Framework for AEC qualifications standard for Automotive “SemiPass” components

SemiPass = Automotive Passive component made with semiconductor fabrication techniques

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Why is a Semiconductor Tier2 making passive components? How to qualify?

Technical situation

- Isolation products allow sensing of EV batteries to safely interact with higher voltage domains using low voltage control electronics.
- Current Generation of Electric batteries is 400 to 800V. Future trend is >1000V DC operation.
- SiCr Thin film Resistors dividers allow connection to the high voltage and provide ppm accuracy over the useful lifetime in an automotive environment.
- Developed for use with Isolation ICs, SiCr resistor dividers are offered as standalone passive products under TI’s RESxxx part number family.

Qualification standards dilemma

- AEC-Q200 is the traditional method for qualifying passives and one used by Supplier quality engineers for passives.
- Passives fabricated using semiconductor processes and package assembly methods such as bond wires that are not comprehended by AEC-Q200. *TI refers to these as “SemiPass” devices to articulate they are different category from traditional passive products. Semipass’s will require different qualification testing similar to AEC-Q100 in many cases.*
- Using the TI’s RES60A-Q1 rated for 1400V DC as a case study, AEC/ JEDEC and other standards such as IEC are reviewed to recommend methods for qualifying SemiPass devices under a hybrid AEC framework.

RES60A-Q1 datasheet.

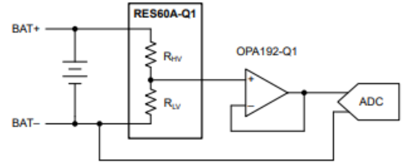
RES60A-Q1 Automotive, 1400V_{DC}, Precision Resistive Divider

1 Features

- AEC-Q200 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C
- High voltage rating:
  - Survives 3+ HiPOT tests at 4000V_{DC} (60s)
  - 1700V_{DC} creepage and clearance support between HVIN and LVIN (IEC-61010 PD 2)
- High dc precision with low shift and drift:
  - Initial ratio matching precision: ±0.1% (max)
  - Low drift: ±1ppm/°C (typ)
  - Accurate ±0.2% across aging and temperature
- Low thermal noise thin-film resistors

2 Applications

- High-voltage bus and battery voltage monitoring
  - HEV/EV battery management system (BMS)
  - HEV/EV DC/DC converter
  - HEV/EV onboard charger (OBC)
  - HEV/EV inverter and motor control
  - ESS – battery management system (BMS)
- Nonisolated, same-ground, always-on dividers
- High common-mode range amplifiers



Typical Schematic

3 Description

The RES60A-Q1 is a matched resistive divider, implemented in thin-film SiCr with Texas Instruments' modern, high-performance, analog wafer process. A high quality SiO_2 insulative layer encapsulates the resistors and enables usage at extremely high voltages, up to 1400V_{DC} for sustained operation or 4000V_{DC} for HiPOT testing (60s). The device has a nominal input resistance of R_{HV} = 12.5MΩ, and is available in several nominal ratios to meet a wide array of system needs.

The RES60A-Q1 series features high ratio matching precision, with the measured ratio of each divider within ±0.1% (max) of the nominal. This precision is maintained over the specified temperature range and aging, with a cumulative drift of only ±0.2% (max). Therefore, the lifetime tolerance of an uncalibrated RES60A-Q1 remains within a ±0.3% (max) envelope.

The RES60A-Q1 is automotive qualified under AEC-Q200 temperature grade 1, with a specified temperature range from –40°C to +125°C. The device is offered in an 8-pin SOIC package, with nominal body size 7.5mm × 5.85mm, and features creepage and clearance distances of at least 8.5mm between the high-voltage and low-voltage pins.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
RES60A-Q1	DWV (SOIC, 8)	5.85mm × 11.5mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and

4 Pin Configuration and Functions

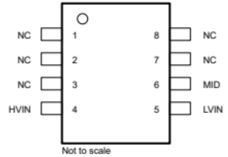


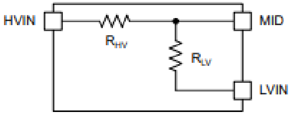
Figure 4-1. DWV Package, 8-Pin SOIC (Top View)

SOIC package

Table 4-1. Pin Functions

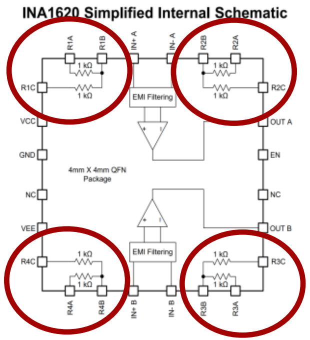
PIN		TYPE	DESCRIPTION
NAME	NO.		
HVIN	4	Input	High-voltage input of divider
LVIN	5	Input	Low-voltage input of divider
MID	6	Output	Center tap of divider
NC	1, 2, 3	—	Noninternally-connected pins on high-voltage side. Solder to the PCB for best board-level reliability. The exposed metal area of these pins must be considered as part of any creepage and clearance calculations.
NC	7, 8	—	Noninternally-connected pins on low-voltage side. Solder to the PCB for best board-level reliability. The exposed metal area of these pins must be considered as part of any creepage and clearance calculations.

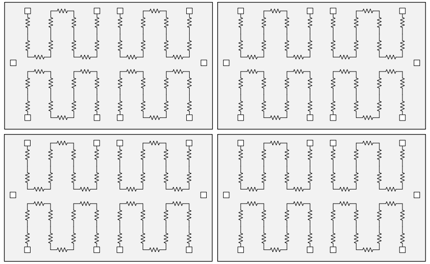
6.2 Functional Block Diagram



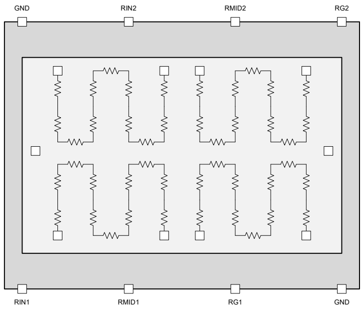
How are RESxxx product built?

- RESxxx products leverages SiCr resistor technology that is in high volume production with TI's INAxxx device families
  - INA1620 was the first to break these resistors out for customer use
- The devices are untrimmed for optimal matching across temperature

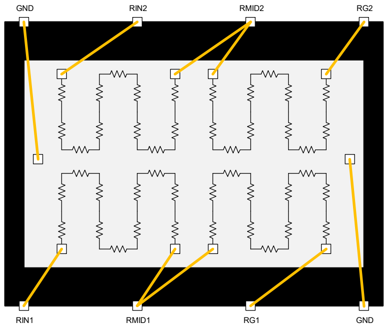




Step 1: Resistive material built up on wafers using same wafer fab as IC. Share similar BEOL flow as IC



Step 2: Wafers cut into die, mounted on leadframe



Step 3: Pins are bonded, encapsulated and separated into individual products before testing.

- **RESxxx Shares with ICs:**
  - ✓ Design rules as IC for isolation.
  - ✓ Wafer fab processing
  - ✓ BEOL PDK
    - EM, TDDB etc.
  - ✓ Bond pads
  - ✓ AT site for automotive packaging in SMT package
  - ✓ BOM : Bond wires, mold compound / die attach

Q200 Qualification

Q200 Table 7 Stress	No.	Reference
Pre- and Post- Stress Electrical Test	1	User Specification
High Temperature Exposure (Storage)	3	MIL-STD-202 Method 108
Temperature Cycling	4	JESD22-A104
Humidity Bias	7	MIL-STD-202 Method 103
High Temperature Operating Life	8	MIL-STD-202 Method 108
External Visual	9	MIL-STD-883 Method 2009
Physical Dimensions	10	JESD22-B100
Terminal Strength (for axial and radial THT components)	11	MIL-STD-202 Method 211
Resistance to Solvents	12	MIL-STD-202 Method 215
Mechanical Shock	13	MIL-STD-202 Method 213
Vibration	14	MIL-STD-202 Method 204
Resistance to Soldering Heat	15	MIL-STD-202 Method 210
ESD	17	AEC-Q200-002
Solderability	18	J-STD-002
Electrical Characterization	19	User Specification.
Flammability	20	UL-94 or IEC 60695-11-5
Board Flex (SMD)	21	AEC-Q200-005
Terminal Strength (SMD)	22	AEC-Q200-006
Flame Retardance	24	AEC-Q200-001

Q100 qualification elements

Q100 STRESS TEST	ABV	TEST#	TEST METHOD
Preconditioning	PC	A1	JEDEC J-STD-020 JESD22-A113
Temperature Humidity Bias or HAST	THB / HAST	A2	JESD22-A101/A110
Autoclave or Unbiased HAST or Temperature Humidity	AC / UHST / TH	A3	JESD22-A102/A118/A101
Temperature Cycle	TC	A4	JESD22-A104
High Temperature Storage Life	HTSL	A6	JESD22-A103
High Temperature Operating Life	HTOL	B1	JESD22-A108
Wire Bond Shear	WBS	C1	AEC Q100-001
Wire Bond Pull Strength	WBP	C2	MIL-STD-883 - 2011
Solderability	SD	C3	J-STD-002
Physical Dimensions	PD	C4	JESD22-B100/B108
Electromigration	EM	D1	
Time Dependent Dielectric Breakdown	TDDB	D2	
Stress Migration	SM	D5	
Pre- and Post-Stress Electrical Test	TEST	E1	Test to spec
ESD - Human Body Model	HBM	E2	AEC Q100-002
ESD - Charged Device Model	CDM	E3	AEC Q100-011
Latch-Up	LU	E4	AEC Q100-004
Electrical Distributions	ED	E5	AEC Q100-009
Characterization	CHAR	E7	AEC Q003
Lead Free	LF	E12	Q005
Process Average Test	PAT	F1	AEC Q001
Statistical Bin/Yield Analysis	SBA	F2	AEC Q002

Failure mechanism-based qualification?

- **AEC-Q100 rev J** : **FAILURE MECHANISM BASED** STRESS TEST QUALIFICATION FOR INTEGRATED CIRCUITS IN AUTOMOTIVE APPLICATIONS
- **AEC-Q200 rev E**: STRESS TEST QUALIFICATION FOR PASSIVE COMPONENTS
- Other AEC-Qxx specifications (Q101, Q104 etc) have "Failure mechanism based.." intent.
- AEC-Q104 provides guidance on identifying potential new and unique failure mechanisms:-

2.2 AEC-Q104 Objective

These tests are capable of stimulating and precipitating semiconductor device and package failures. The objective is to stimulate / precipitate failures in an accelerated manner compared to application conditions. This set of tests should not be used indiscriminately. Each qualification project should be examined for:

a. Any potential new and unique failure mechanisms as determined through a Failure Mode Effects Analysis (FMEA).
b. Any situation where these tests/conditions may induce failures that would not be seen in the application.
c. Any extreme use condition and/or application that could adversely reduce the acceleration and, therefore, lifetime coverage of the stress test.

TI qualification of High voltage thin film resistors

Technology qualification per AEC-Q100 focusing on **durability** and **aging** of thin film resistors. New and unique situations:-

- TDDB of isolation structure.
  - Included robustness to Voltage overstress covering scenarios such as “HiPot” testing by customer.
- Electromigration of resistor circuitry.
- Reliability stressing
  - DC bias with High voltage HTOL including aging study.
  - AC bias engineering study including drift analysis.
  - High temperature storage including aging study.
  - Biased humidity including aging studies
  - Q006 durations for remaining package tests.
- ESD characterization

Q200 and Q100 : Similar but different tests

- Differences in execution in some key tests

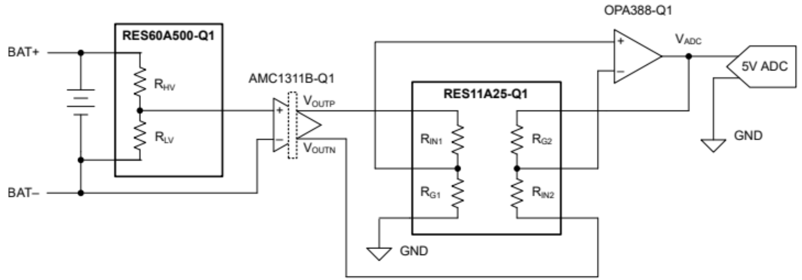
	Q200 table 7	Q100
Temperature grades	No temperature grades - per ambient operating	Grade 0 to grade 3
Preconditioning	• 3x reflow before TC, HB and HTOL. • No moisture soak required.	A1 test Moisture soak + 3x reflow. Before A2 to A5. Not for HTOL.
Temperature Cycling (JESD22-A104)	• -55C/Tmax operating x 1000 cycles • Dwell time- min 15 minutes • Transition time 1 minute max	• -55/150C grade 1 x 1000 cycles. • Dwell time 1 minute • Ramp rate typical 15 °C/minute
Humidity Bias	• MIL-STD-202 Method 103 • THB only • 10% of operating power (for components with • specified operating voltages higher or equal to • 500V, 10% of operating voltage)	• JEDEC JESD22-A104 • THB or BHAST • Vmax.
High Temperature Operating Life	• MIL-STD-202 Method 108 • Intermittent Power for 1000 hours: 90 minutes ON 30 minutes OFF.. • maximum specified operating temperature at 100% rated power	• JEDEC JESD22-A108 • Grade 1 : 125C Ta x 1000 hours. • 100% on and Vmax
ESD	• AEC-Q200-002	• ESD HBM per AEC Q100-002 • ESD CDM per AEC Q100-011

Technical judgement of package reliability

- One key difference for a SemiPass may be the use of bond wires.
- Bond wire have known bond wire fail manufacturing and intrinsic reliability concerns that need to be qualified.
- Packages used have MSL sensitivity ratings.
- Q100 Preconditioning that including moisture soak per MSL rating is recommended to address popcorning/ delamination. This should be performed for remaining group of package studies.
- Per JESD22-A104E, advisories are given about ramp times and dwell times for bond wire units
  - Dwell times are not critical except for interconnect solder fatigue. For bond wire, 1 minute dwell is ok.
  - A thermal shock condition can overstress bond wires and slower ramp times are recommended for IC type of packages.
    - *"Typical ramp rate for this situation is 15 °C/minute or less for any portion of the cycle, with a preferred rate of 10 °C to 14 °C/minute"*
- If copper wire used it should include AEC-Q006 technology studies.

Power on test

- Intermittent power (90 minutes on / 30 minutes off) vs 100% On.
- Both situations were studied for technology qualification and RES60.
- **TI opinion** : 100% on better represents application use condition of connecting to the HV battery.



  - Example : Circuit for battery voltage measurement featuring the RES60A-Q1, RES11A-Q1 and AMC1311B

ESD testing of thin film resistors

- Methods for testing ESD between Q200 and Q100 are different.
- AEC-Q200-002 shares similarities to IEC 61000-4-2 system level ESD testing.
- System level ESD will have higher energy current waveforms. May need additional protection for the higher system level voltage ranges.
- AEC-Q100 HBM / CDM are handling ESD events.
- It is understood that AEC-Q200 will adopt ESD HBM in future revision for the handling situations in factories.

For RES60-Q1:

- Specified AEC-Q200-002 to 4KV level in datasheet.
- Characterized to IEC 61000-4-2 for 4kV.

“HiPot” Testing

- HiPot reference to High Potential testing.
- Used to verify that electrical insulation in an EV battery system can safely withstand voltages above normal operating levels without breaking down.
- HiPot ensures dielectric integrity.
- Technology qualification characterized safe levels of HiPot testing that can be supported.
- HiPot testing varies by OEM and typically 1.5 to 2x rated voltage with soak time up to 1 minute.
- RES60 device supports 3 HiPot exposures to 4000Vdc for 60s.
- HiPot is not called out in AEC-Q200 but critical for such components.

AEC-Q004: Zero Defect approach for RES60A-Q1.

- A SemiPass component will benefit from established practices for semiconductor type of products that called out in AEC-Q004.
- Wafer fab – automotive service package.
- Assembly site – automotive service package.
  - Addition of Bonding wire controls and materials.
- Specific to RES60 in early life screening tests: 100% production test for Voltage OVST of +/- 2700Vdc and applied to the device for 100ms. Parametric tests performed before and after OVST.

Semipass: Recommendations from the case study

1. Apply a failure mechanism-based AEC-Qxxx qualification that reflects the underlying design and manufacturing processes of the SemiPass.
   - Hybrid Q200 / Q100 qualification.
   - Q006 if appropriate.
2. Document guidance for this approach into AEC-Q200
   - Envisaged this will be an addendum to AEC-Q200.
   - Mark Yampolsky (TI) volunteered to document a proposal.
3. Use opportunity to capture specific tests / loads unique to High Voltage EV battery.
   - For example: “HiPot” tests carried out by the battery OEMs.