

Design-Phase prediction of ELFR assurance in automotive ICs using physics-based dielectric reliability modelling

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2026-10-15



Evolution of ELFR prediction at Infineon toward securing a competitive ELFR across all products!

RELATED TO:



Dielectric defects

in

Smart Power^{BCD} Technology

Towards the creation, establishment and optimization of a new methodology

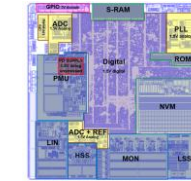
First products development in the new SPT BCD Technology

Best-guess stress concept

Unclear link between **fab** and **field** performance

New technology with **no reference data**

Production ramp-ups with **BI oven testing**



All-in-one die

- ✓ Mixed Signal
- ✓ Memories
- ✓ Logic
- ✓ Power



ELFR study as a learning result

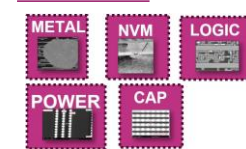
Several years of **learning to succeed**

- ✓ **Design** rules added
- ✓ **FE process** improvements
- ✓ **Test & stress** upgrades

*Simplified Development flow



Dielectric defects



Design for Stress (DfS) methodology

“Stress Guidelines”:

- ✓ A compilation of **ATE*** **High Voltage** stress.
- ✓ Binding doc in product development.

The start of physics-based dielectric reliability modelling.



Ensure the **same competitive ELFR** for all products

H. Lewitschnig,
J. Goncalves, “Design
for Stress”, *IEEE*, 2021



DfS in Infineon development flows

Technology development flow

Product development flow

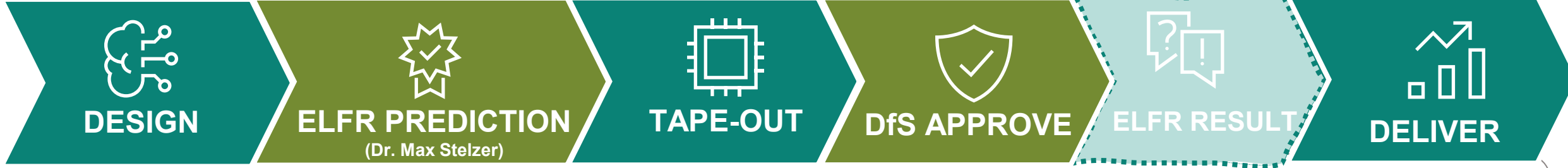
CONSERVATIVE STRESS TIMES

OPTIMIZATION BASED ON FIELD PERFORMANCE

*Automated Test Equipment, e.g., Wafer Test equipment

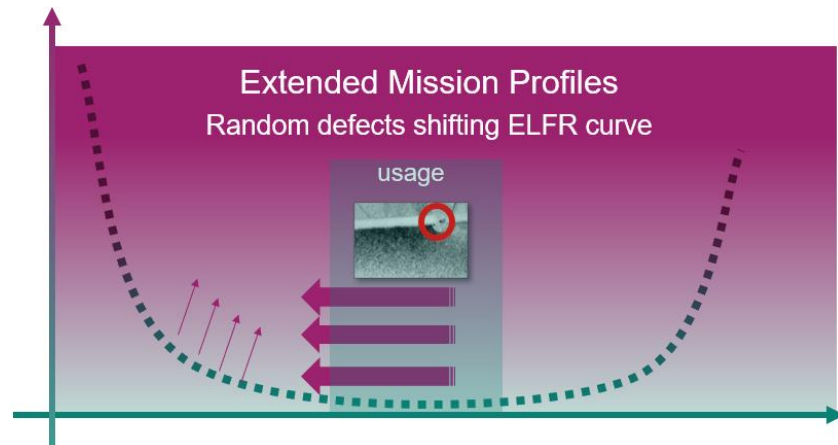
With the DfS methodology, **ELFR assessment** transitions from a learning **result** into an increasingly accurate **prediction** step.

*Simplified Development flow



- 1 An ELFR **prediction** and **approval** gate is integrated into **each product*** development process
- 2 Efficient defect activation and detection during **ATE HV testing**, eliminating the need for a productive BI oven
- 3 Methodology inherently addressed the rapidly evolving **market demands and trends**.

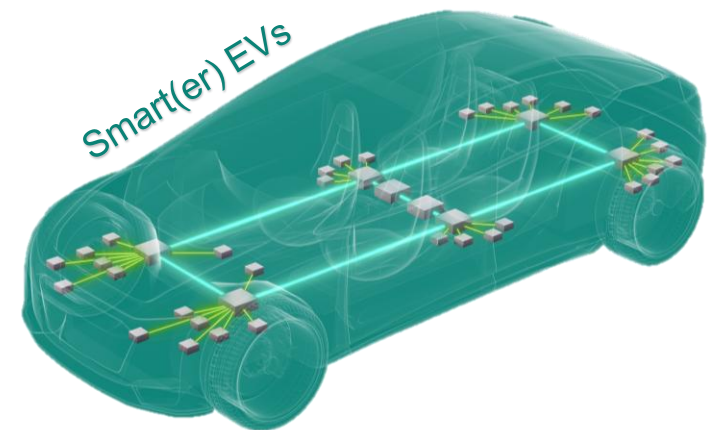
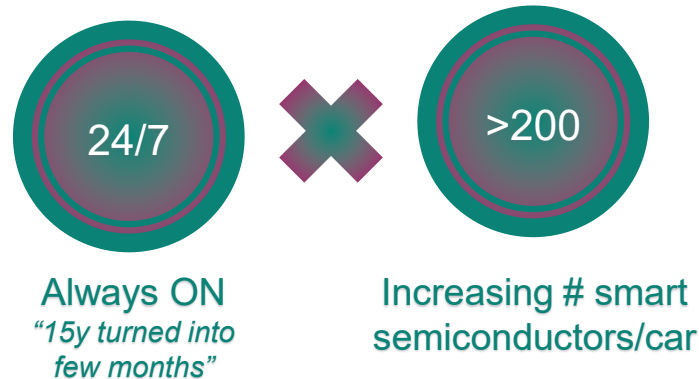
Demanding Market trends



* Smart Power Technologies (SPT)

2026-10-15

Public

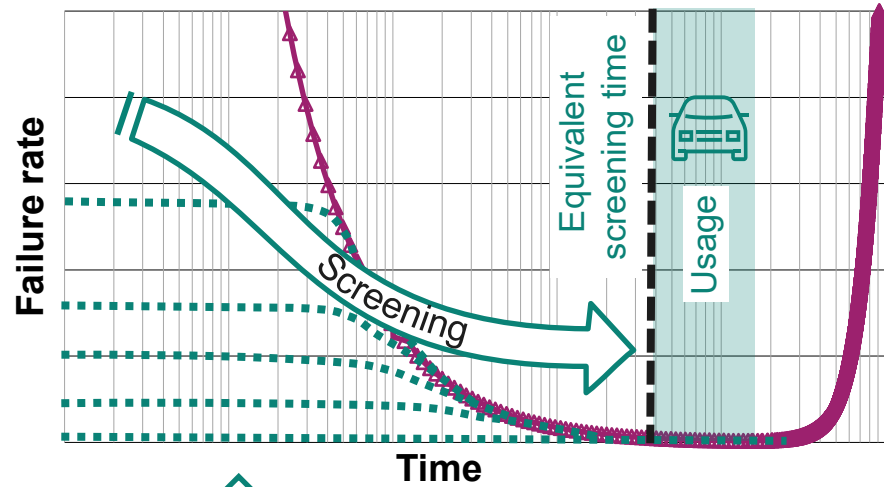


The methodology behind our ELFR prediction

Max Stelzer, PhD, Infineon Technologies AG



Screening reduces early-life failures



Failure rate as a function of time: $h(t) = \frac{f(t)}{R(t)} = \frac{f(t)}{1-F(t)} = \frac{\beta}{\tau} \left(\frac{t}{\tau}\right)^{\beta-1}$
→ after screening: $h(t) = \text{const.} \Rightarrow \beta = 1$

Prevention of early fails in the field



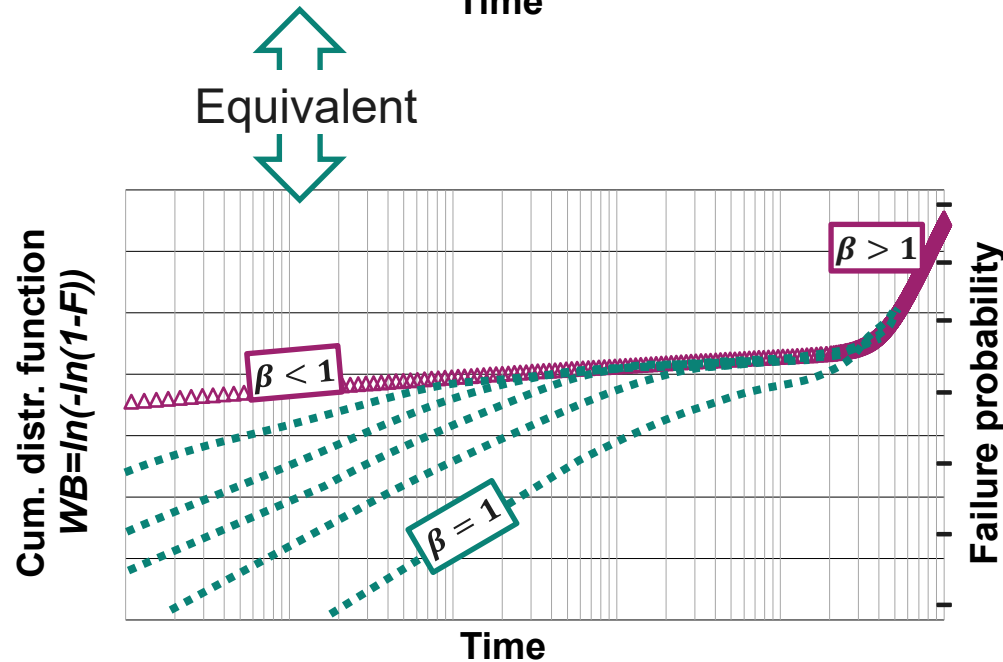
Process optimization and inline inspection to reduce defects



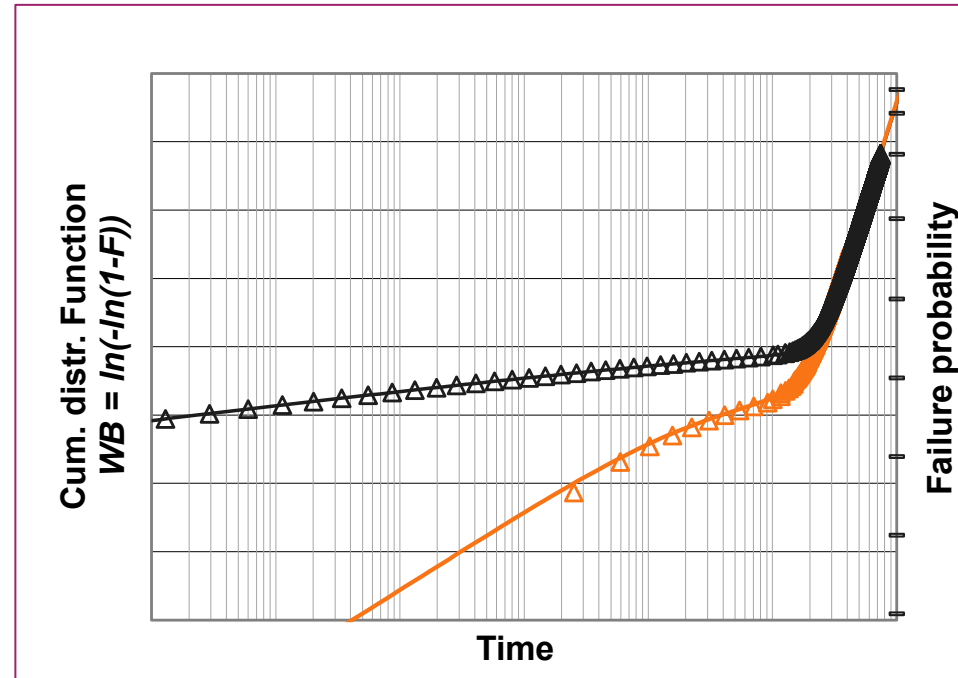
Robust design/layout



Electrical screening by WL burn-in or HV screening
→ Weak devices are detected and scrapped before field use



Key questions for an effective screening strategy



Time?
Voltage?

Which are
the critical
defects?

How to handle
voltage spikes?

What is a “safe”
design?

What is the
expected ELFR?

Less burn-in – more
HV screening?

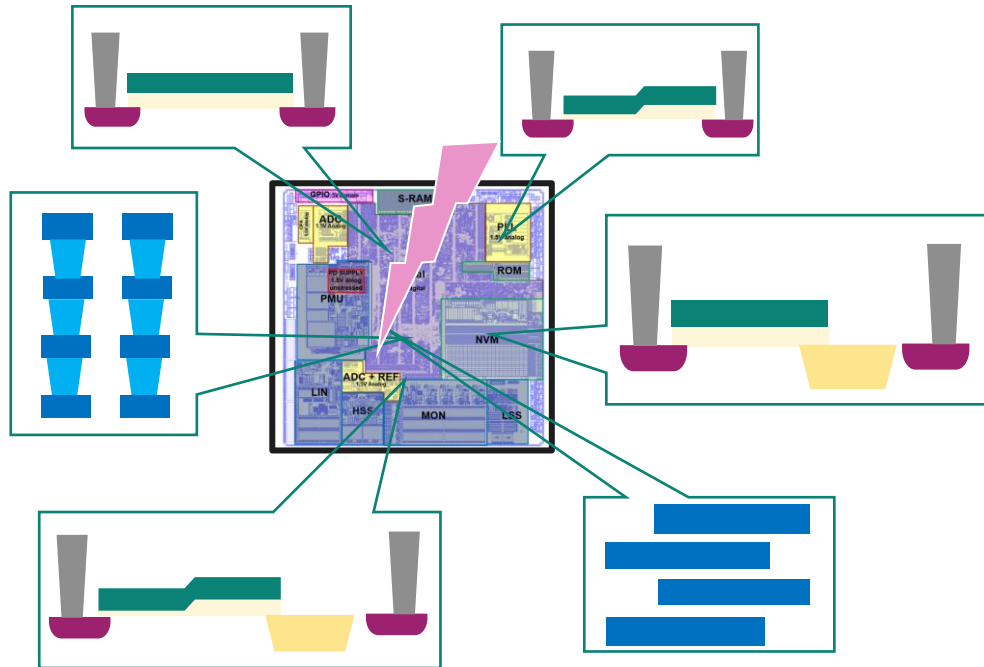
Which failure
probability can be
ensured?

Is the DD-level of
the fab sufficient
for automotive?

Learning from statistics

Zero-defects target for automotive applications

-  Automotive applications require **stricter failure-probability targets**
-  **Diverse product spectrum** for an individual technology → product-specific assessment
-  **Higher voltages** and **multiple** voltage classes compared to CMOS → device fine assessment
-  Power devices introduce **failure modes** not seen in logic technologies



Multiple potential
failure locations within
the device

A generic reliability assessment is not sufficient for automotive power devices

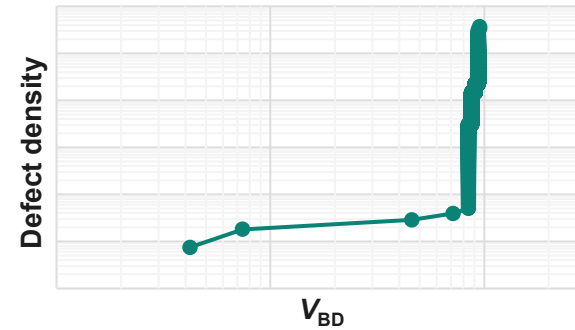
From fab performance to device-specific defect risk

Fab performance

Failure mode

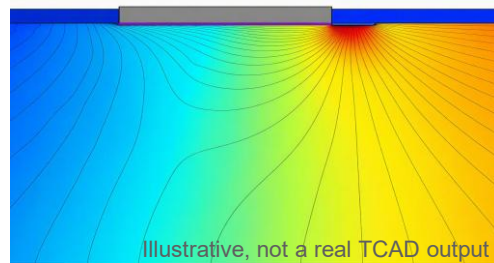


Electrical
defect density

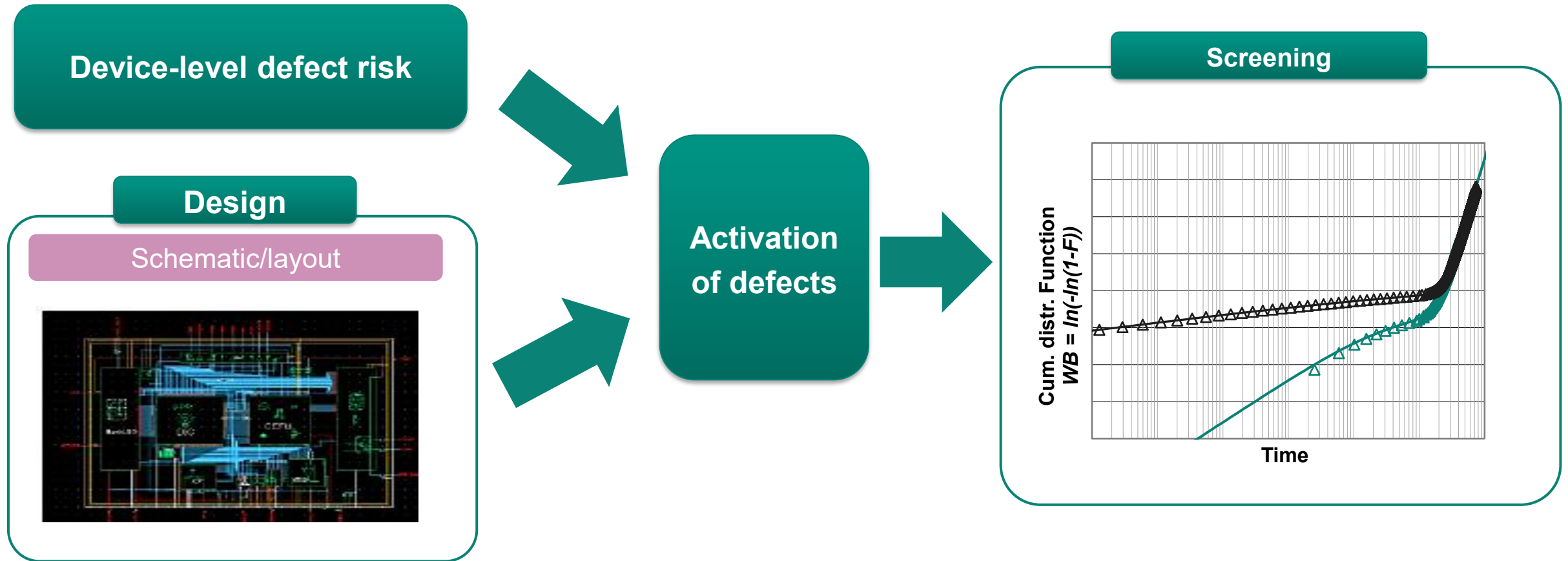


Technology

Device simulation

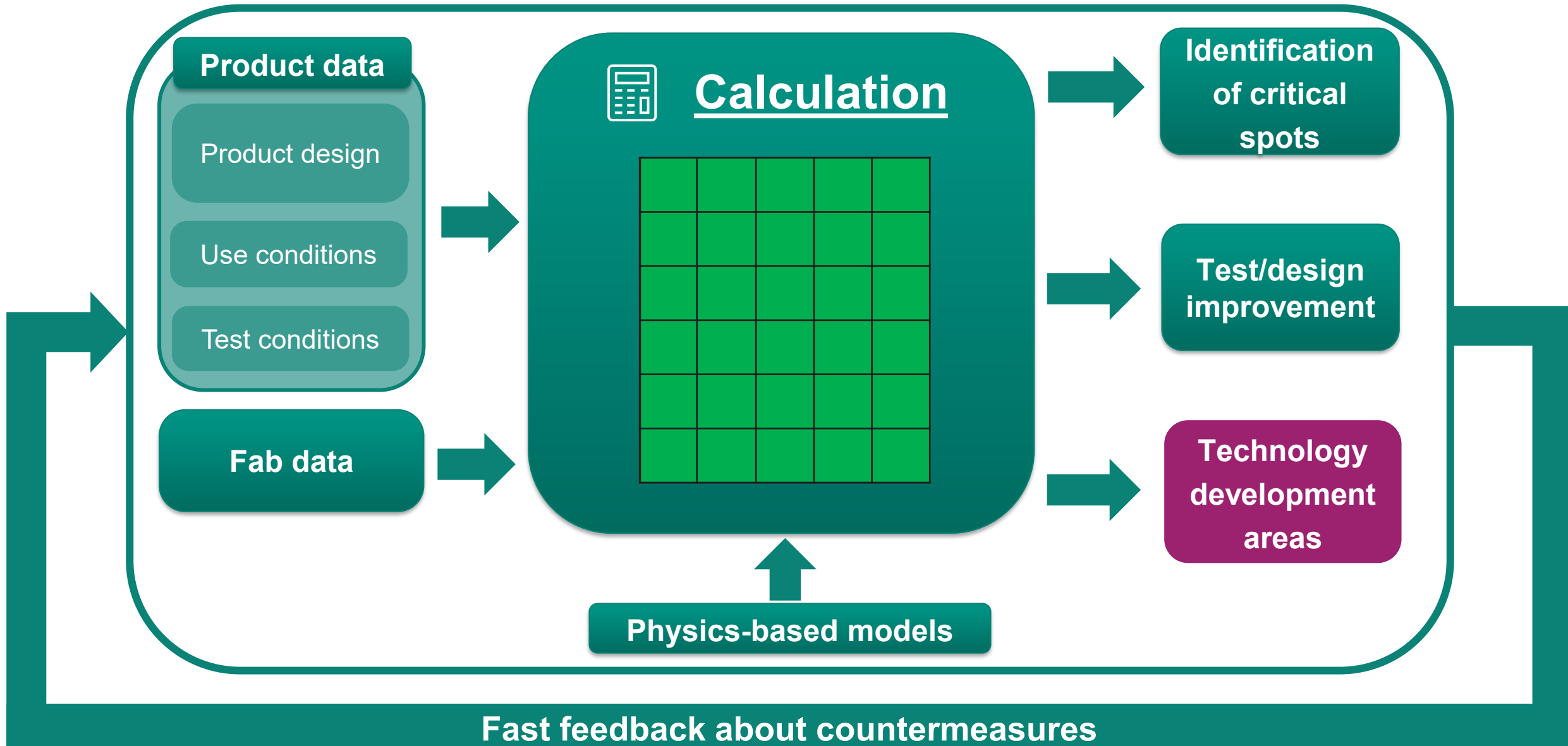


Device-level
defect risk

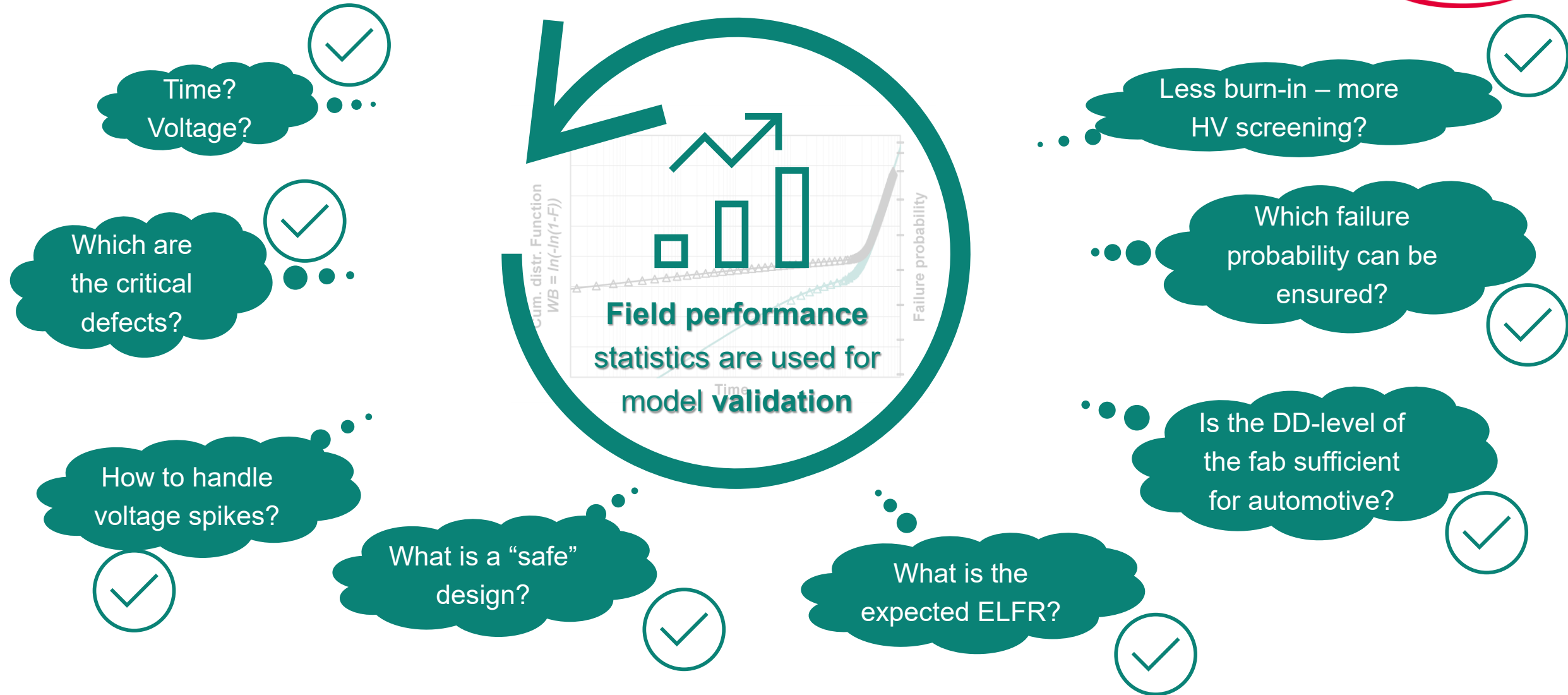


OUTPUT: ELFR PREDICTION

Calculation of product-specific failure risk



Field data can validate and refine ELFR predictions



Find the balance of **quality, performance and cost**

Wrapping-Up...

- ✓ DfS methodology enables an effective acceleration and detection of ELFR dielectric defects across all products
- ✓ Supported by an efficient link between fab data and product info towards an optimized ELFR quantification during design-phase

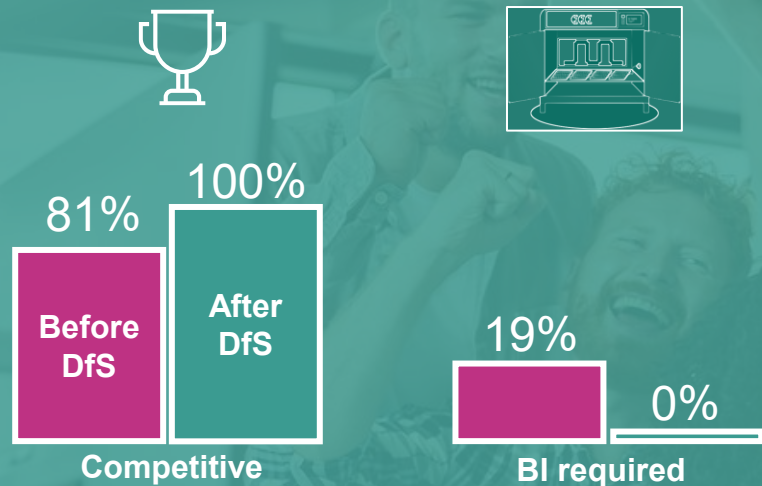
What's left...

- ✓ DfS: A proven success story
- ✓ Ensuring competitive ELFR across all cases



A success story proven by “first time right” ELFR studies and improved competitiveness of products since the introduction of DfS methodology

% of products per ELFR “class”



“First Time Right” ELFR studies

Before DfS



- ! Restart needed
- ! (un)necessary FE proc. change
- ! Test Program changes

After DfS



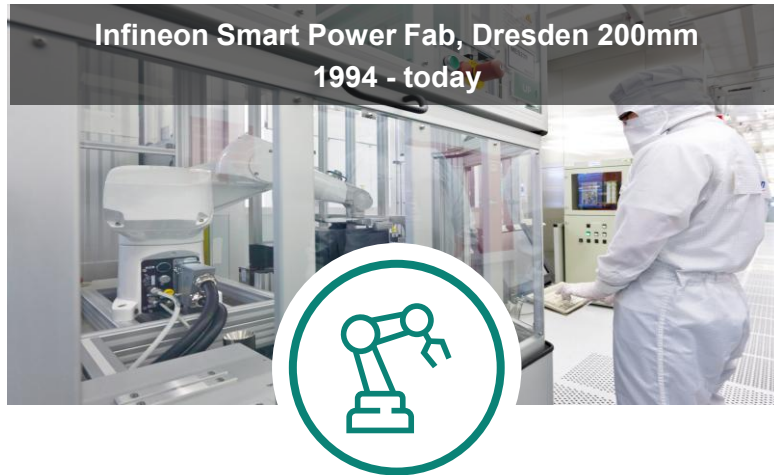
- ✓ No restart needed
- ✓ No FE process changes
- ✓ No Test Program changes



Design for Stress methodology brought a consistent outcome in:

- ✓ Products championing ELFR competitiveness
- ✓ Timely execution and first-time right completion of ELFR studies

A systematic methodology embedded in Infineon's development flows to ensure competitive ELFR performance across all products



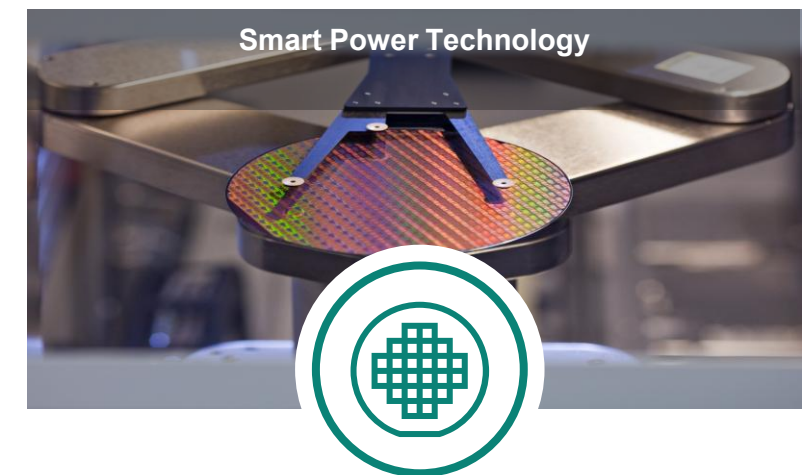
High volume manufacturing site(s)

Ensure the same competitive ELFR for all **new development products**



New manufacturing site(s)

Ensure the same competitive ELFR from the **ramp-up phase onwards**



SPT technologies

Ensure the same competitive ELFR to all **derivative technologies and new devices**



Optimized Design for Stress (DfS) methodology

Ensuring that all products are designed, manufactured and tested at optimum costs towards Zero Defects.

QUESTIONS?

It would be a pleasure to discuss ELFR with you over a 🍺 🥨



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Design for Stress Methodology

We ensure the reliability of your future products!

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Publications:

H. Lewitschnig, J. Goncalves,
"Design for Stress", IEEE, 2021

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