



Functional Safety – Radiation Effects

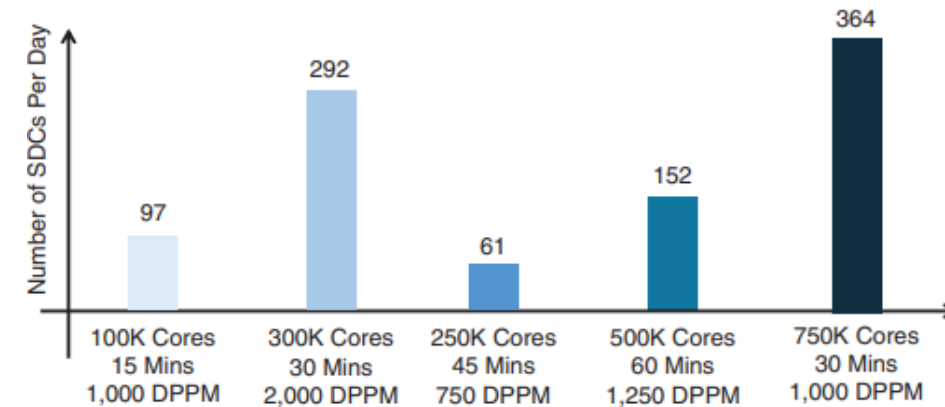
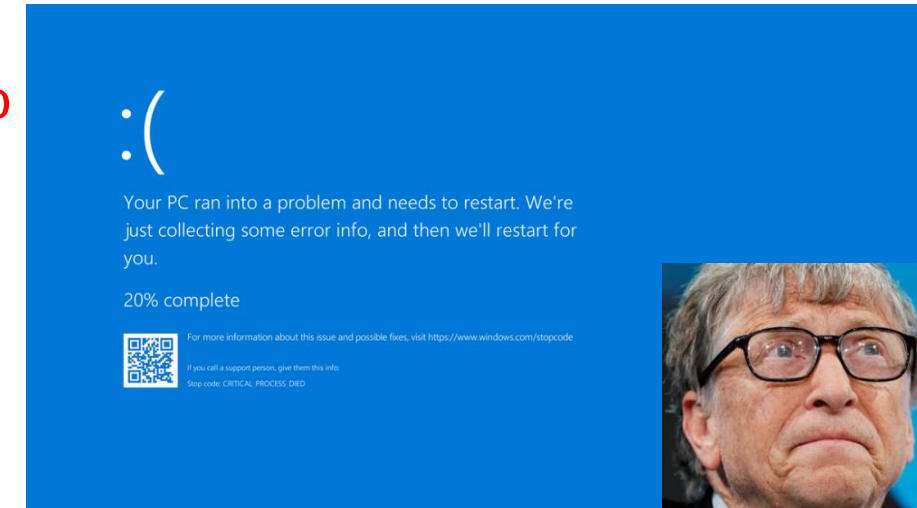
Impact of Radiation Effects on Advanced Process Semiconductors



Soft Error Overview

— Numbers, Numbers, Numbers

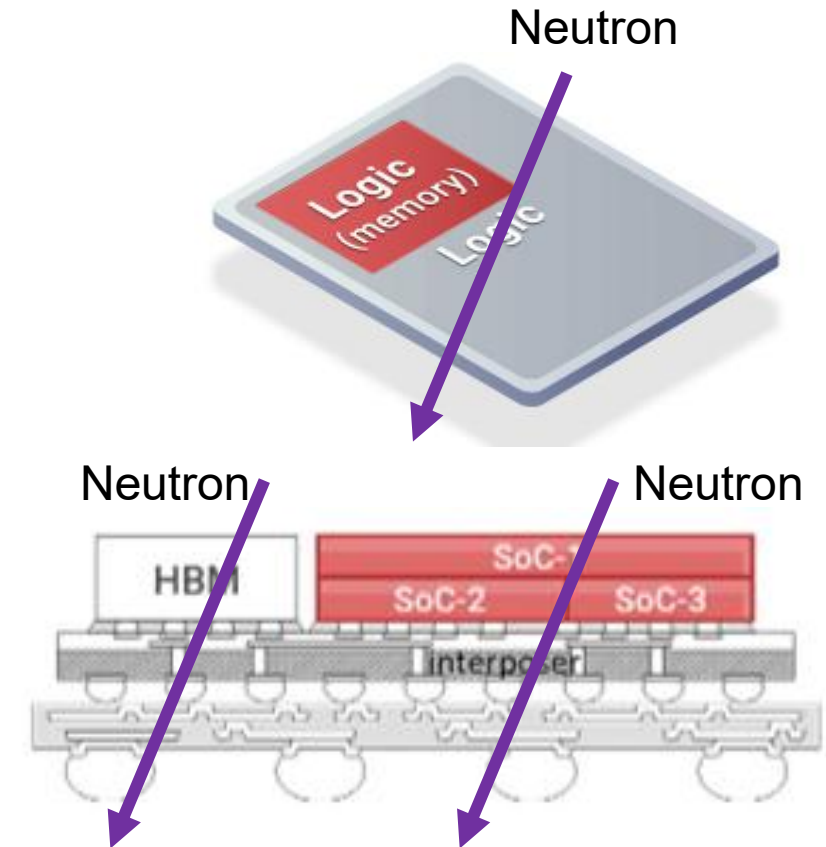
- Permanent Failures Reliability FIT < 20FIT
 - Soft Error Rate: **Known greater than 100 or 1000 per Mb**
- Hostile Universe (Veritasium Video)
 - Server: Google, Sun, EMC
 - HPE Soft Error, Dell Soft Error, OCP Gemini SDC
 - Avionics: 2008 Airbus A330, 2025 6,000 A320 Recall
 - Evoting: Belgium evoting
 - Telecom: HuaweiES3000, CiscoASR9000, ITU-T K.130*
 - Automotive:
 - Standards
 - AEC-Q100 mandate on 1Mb SRAM/DRAM
 - ISO26262 mandates on transient faults
 - **Misconception: SER isn't always transient**
 - Toyota Unintentional Acceleration
 - Imagine recalling 20 years of products
 - Takata airbag , Arc Automotive
 - Taiwan Gogoro Battery Problem
 - Xiao Mi SU7 (Is ADAS immune?)



— Inherent SDC Vulnerable Structure of AI

★ Inherent Vulnerable Structure of AI

- Layered, non-deterministic, and parallelized
 - Errors in (MMA) MAC -> Divergence in gradient descent -> Math contagion that halts training cluster or corrupts inference outputs that evades standard correctness check.
- Advance process node
 - Lower V_{DD} (Q_{CRIT}): More vulnerable to soft errors (less energy needed)
 - Denser volume = worse multiple bits errors = failures of SECDED ECC -> ECC aliasing -> SDC
- Known IC architecture problems
 - MCU/CPU: incorrect output, SEFI
 - MAC: stuck errors
 - HBM: Multiple days unattended runs of training with MBU
 - Etc.



— How Is SDC Manifested in AI Applications?

- ✦ Interrupted job, halted computation, freeze:
 - Possible Causes: SDC in MCU i-cache, program counter, etc.
 - Relatively easy to correct and correct (reset/power cycle)
 - Probability tends to be low
- ✦ Incorrect numerical activations, Hallucinations, Low-quality or garbled reasoning, Invalid or NaN (not a number) token probability, Crashes or failed inference, etc.
 - Possible Causes: SDC in HBM, MMA. Faults in parameters (weights).
 - Hard to detect or identify error location (origin)
 - Higher probability
- ✦ Parameter Vulnerability Factor (AVF version to evaluate AI)

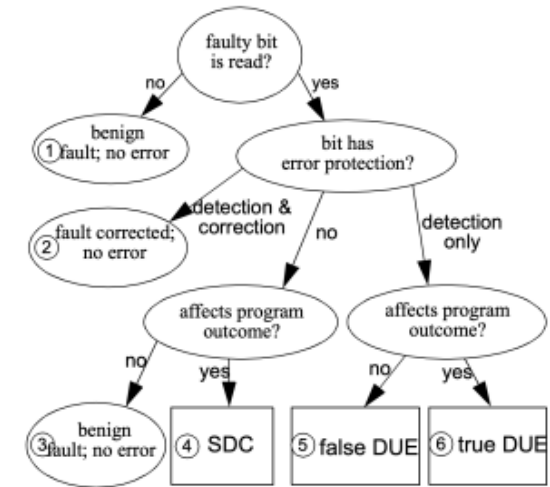


Figure 1: Classification of the possible outcomes of a faulty bit in a microprocessor. SDC = silent data corruption. DUE = detected unrecoverable error [1]

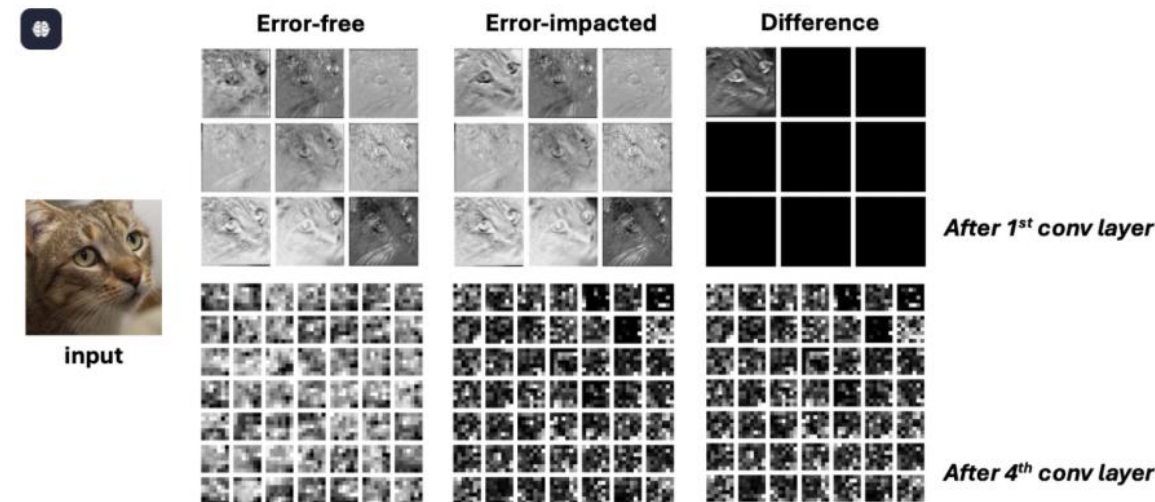


Figure 1: Flipping a random bit of one parameter in the 1st convolution (conv) layer in ResNet-18 drastically alters the model's output.

— Robotics Accidents

- Video: [Unintentional Arm Fling](#)
- News:
 - [Unintentional Arm Control](#)
 - [2023 North Korea Robotic Arm Accident](#)
 - [2023 Tesla Kuka Robotic Arm Accident](#)

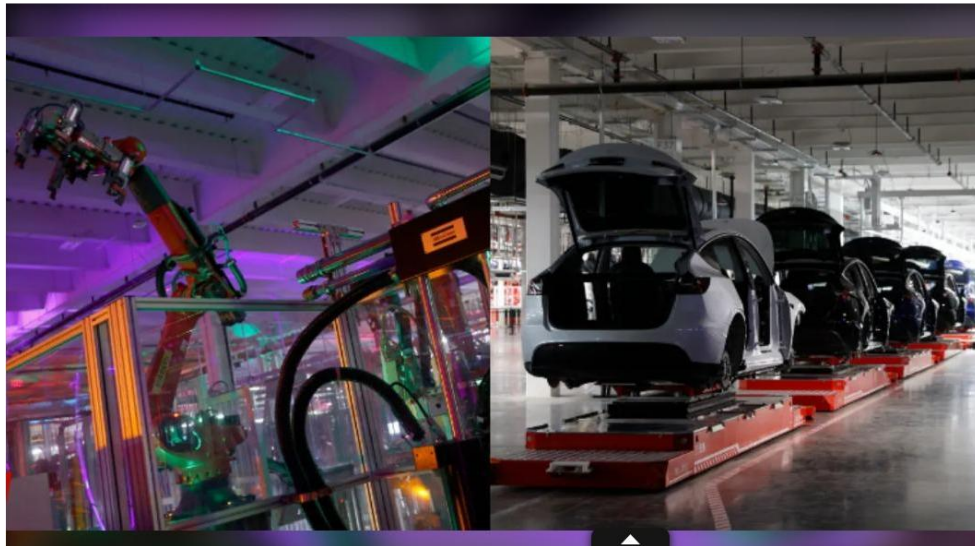
首頁 > 國際

特斯拉爆機器人「插入工程師」爆血 馬斯克甩鍋：非公司製造

編輯 丘力龍 報導

發佈時間：2023/12/28 16:19

最後更新時間：2023/12/28 16:19



疑被機器人誤判是1箱辣椒 南韓工人慘遭活活壓死

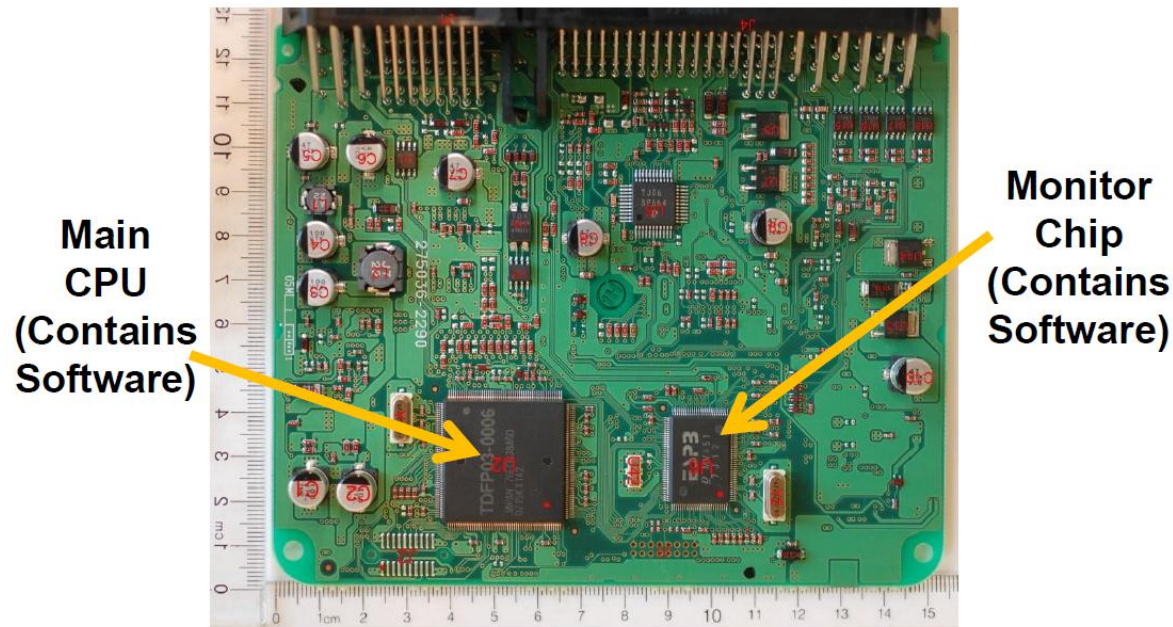


韓國慶尚南道8日晚間發生1起工安意外，1名40歲設備檢修人員不幸被機械手臂當作成箱的辣椒後被送上輸送帶導致面部及胸部被壓碎送醫不治。示意圖，圖與新聞事件無關。（歐新社）

Toyota – ECC – MBU? Interleaved?

Carnegie Mellon

Toyota 2008 ETCS – Two CPUs



http://m.eet.com/media/1201063/Toyota_ECM.jpg

Carnegie Mellon

Did NASA Have Correct & Complete Information?

- The ESP-B2 Monitor Chip has software in it
 - But NASA does not analyze ESP-B2 software in its reports – analysis is limited to Main CPU software.
- NASA credited Error Correcting Codes in RAM for 2005MY:
The Main and Sub-CPU's use two types of memory: non-volatile ROM for software code and volatile Static Ram (SRAM). The SRAM is protected by a single error detect and correct and a double error detect hardware function performed by error detection and correction (EDAC) logic.
[NASA REPORT P. 54]
 - Apparently because Toyota told NASA it had EDAC (ECC)
[Bookout 2013-10-14PM 83:19-84:25]
- Exponent public report claims ECC for Main CPU [p. 201]
 - Only claims SEC, not SECMED
- But, actually no EDAC on RAM for 2005MY vehicle
[Bookout 2013-10-11 AM 55:22-25; 2013-10-14 AM 72:5-73:11; 2013-10-14AM 78:16-79:17]

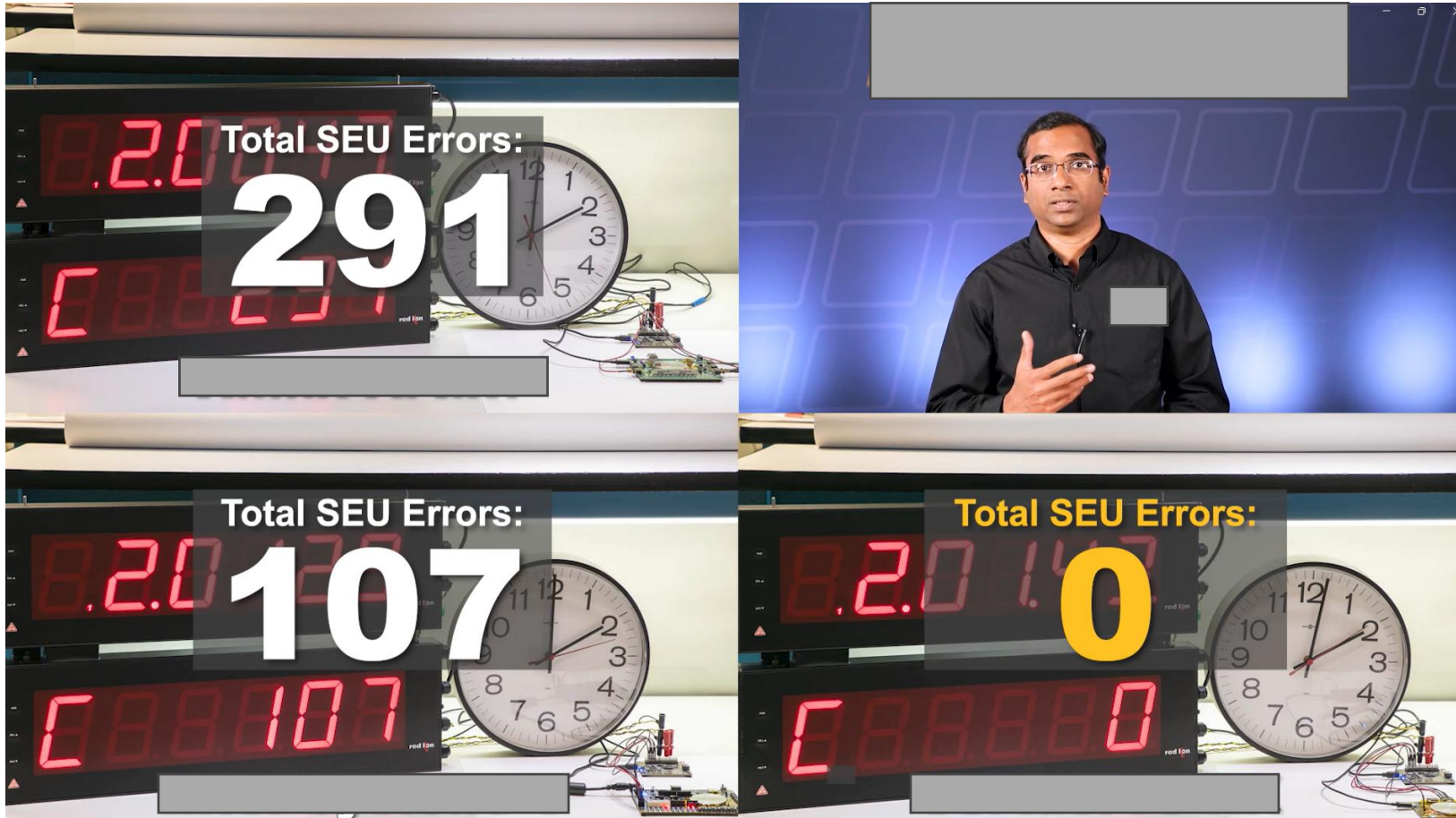
— SER is just FUD, I Can Safely Ignore It

- Tier-1/OEM Customer Types
 - Don't know and don't care about SER
 - Paper work only -> Submit your reports and you're good
 - Guru -> Will catch you if you reports seems out of line~
- SER can be powerful marketing and sales weapon
 - When power, performance, features, price, etc. aren't differentiating factors and your competitors sales rep is smoking hot...
 - Here comes SER to save the say
 - Accelerated results numbers takes 3~6+ months
 - It's probability -> Only your tier-1 accounts will notice it
 - If you don't care, there'll be no R&D or QA requirements
 - The questions isn't if I have the problem, it's how bad
 - When your customer identified it's your problem, it's too late
- If you hit the jackpot...



Marketing FUD

- When competitor tested your part, how would you respond? Can you respond?





AEC-Q SER Requirements

Appendix 6 - Part Design Criteria to Determine Need for SER Testing

■ A6.1 SER Part Design Criteria

Use the following criteria to determine if a part is a candidate for SER Testing:

- a. The part use application will have a significant radiation exposure such as an aviation application or extended service life at higher altitudes.
- b. SER testing is needed for devices with large numbers of SRAM or DRAM cells (> 1 Mbit). For example: Since the SER rates for a 130 nm technology are typically near 1000 FIT/MBIT, a device with only 1,000 SRAM cells will result in an SER contribution of ~1 FIT.

■ A6.2 SER Part Design Factors

Examples of factors that would be expected to affect SER results:

- a. Technology shrink to small L effective.
- b. Package mold/encapsulate material.
- c. Bump material making die to package connections for Flip Chip package applications.
- d. Mitigating factors such as implementation of Error Correcting Code (ECC) and Soft Error Detection (SED).

■ A6.3 New SER Testing

Cases where new SER testing may be required:

- a. Change in basic SRAM/DRAM transistor cell structure (e.g., L_{eff} , well depth and dopant concentration, isolation method)

AEC Q100

Table 2: Qualification Test Methods (continued)

TEST GROUP E – ELECTRICAL VERIFICATION TESTS (CONTINUED)								
STRESS	ABV	#	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
Latch-Up	LU	E4	H, P, B, D, E	3	1	0 Fails	AEC Q100-004	See attached procedure for details on how to perform the test. TEST before and after LU at room and hot temperature.
Electrical Distributions	ED	E5	H, P, B, E	30	3	Where applicable, $C_{PK} > 1.67$	AEC Q100-009 AEC Q003	Supplier and user to mutually agree upon electrical parameters to be measured and accept criteria. TEST at room, hot, and cold temperature.
Fault Grading	FG	E6	---	---	---	AEC Q100-007 unless otherwise specified	AEC Q100-007	For production testing, see Q100-007 for test requirements.
Characterization	CHAR	E7	---	---	---	---	AEC Q003	To be performed on new technologies and part families.
Electromagnetic Compatibility	EMC	E9	---	1	1	---	SAE J1752/3 – Radiated Emissions	See Appendix 5 for guidelines on determining the applicability of this test to the device to be qualified. This test and its accept criteria is performed per agreement between user and supplier on a case-by-case basis.
Short Circuit Characterization	SC	E10	D, G	10	3	0 Fails	AEC Q100-012	Applicable to all smart power devices. This test and statistical evaluation (see Section 4 of Q100-012) shall be performed per agreement between user and supplier on a case-by-case basis.
Soft Error Rate	SER	E11	H, P, D, G	3	1	---	JEDEC Un-accelerated: JESD89-1 or Accelerated: JESD89-2 & JESD89-3	Applicable to devices with memory sizes $\geq 1\text{Mbit}$ SRAM or DRAM based cells. Either test option (un-accelerated or accelerated) can be performed, in accordance to the referenced specifications. This test and its accept criteria is performed per agreement between user and supplier on a case-by-case basis. Final test report shall include detailed test facility location and altitude data.
Lead (Pb) Free	LF	E12	L	See Test Method	See Test Method	See Test Method	AEC Q005	Applicable to ALL Pb-free devices. Note the recommendations for all related solderability, solder heat resistance and whisker requirements.

AEC Q100

Note: A letter or "•" indicates that performance of that stress test should be **considered** for the appropriate process change. Reason for not performing a considered test should be given in the qualification plan or results.

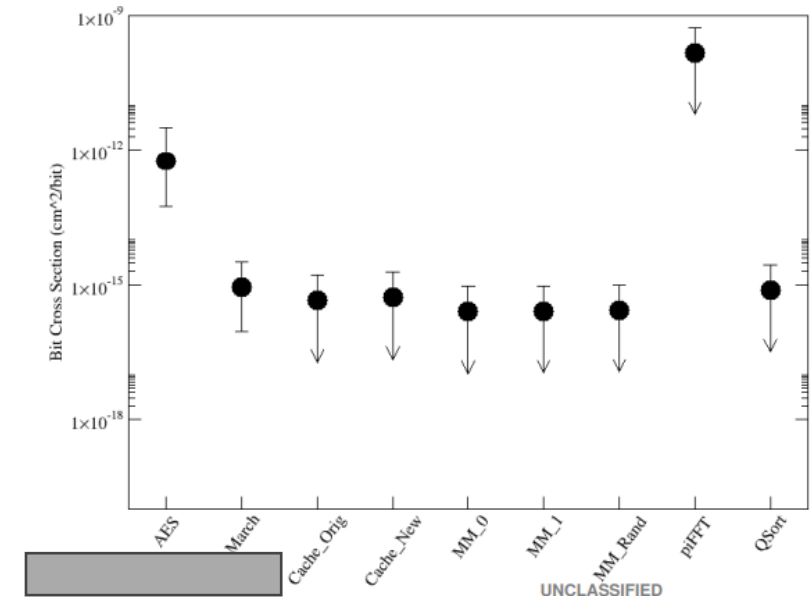
Table 2 Test #	A2	A3	A4	A5	A6	B1	B2	B3	C1	C2	C3	C4	C5	C6	C7	D1	D2	D3	D4	D5	E2	E3	E4	E5	E7	E9	E10	E11	E12	G1- MECH	G4	G5	G6	G7	G8	
Test Abbreviation	THB	AC	TC	PTC	HTSL	HTOL	ELFR	EDR	WBS	WBP	SD	PD	SBS	LI	BST	EM	TDD	HCI	BTI	SM	HBM	CDM	LU	ED	CHAR	EMC	SC	SER	LF	G1- MECH	G4	G5	G6	G7	G8	
DESIGN																																				
Active Element Design		•	•	M		•	•	DJ								D	D	D	D	D	•	•	•	•	•	•	•	•					F			
Circuit Rerouting			A	M																	•	•	•	•	•	•	•									
Wafer Dimension/ Thickness			E	M		•	•		E	E									•		E	E	E	•												
WAFER FAB																																				
Lithography	•		•	M		•	G		•	•										•				•												
Die Shrink	•	•		M		•	•	DJ								•	•	•	•	•	•	•	•	•	•	•	•	•								
Diffusion/Doping				M		•	G												•		•	•	•	•	•	•										
Polysilicon			•	M		•		DJ											•		•	•	•	•	•	•										
Metallization/Via/ Contacts	•	•	•	M		•			•	•						•				•				•	•		•									
Passivation/Oxide/ Interlevel Dielectric	K	K	•	M		•	GN	DJ	K	•							•	•	•	•		•	•	•	•	•										
Backside Operation			•	M		•															M	M	•		•									H		H
FAB Site Transfer	•	•	•	M		•	•	J	•	•						•	•	•	•	•	•	•	•	•											H	
WAFER BUMPING																																				
Redistribution Layer	•	•	•	M	•										•									•												
Under Bump Metal	•	•	•	M	•										•									•												
Bump Material	•	•	•	M	•										•									•												
Bump Site Transfer	•	•	•	M	•										•									•												
ASSEMBLY																																				
Die Overcoat/ Underfill	•	•	•	M	•	•																						•								H
Leadframe Plating	•	•	•	M	•					C	•		•																L						H	
Bump Material/ Metal System	•	•	•	M	•	•						•	•															•	L							
Leadframe Material		•	•	M	•					•	•	•	•	•													•	L	H						H	
Leadframe Dimension		•	•	M							•	•		•															L	H						
Wire Bonding	•	•	•	Q	•				•	•														M												
Die Scribe/ Separate	•	•	•	M																																
Die Preparation/ Clean	•	•		M					•	•																										H
Package Marking											B																									
Die Attach	•	•	•	M		•																			•		•		L	H					H	H
Molding Compound	•	•	•	M	•	•	•				•	•		•														•	L							
Molding Process	•	•	•	M	•	•					•	•		•															L							
Hermetic Sealing		H	H		H							H		H																			H		H	
New Package	•	•	•	M	•	•	•		•	•	•	•	T	•								•	•		•		•							H	H	
Substrate/Interposer	•	•	•	M	•	•			•	•			T																L	H					H	H
Assembly Site Transfer	•	•	•	M		•	•		•	•	•	•	T	•										•					L	H					H	H



AEC-Q Current Limitation

— Same JESD89B test, Significant Different Results

- Tests performed in accordance to JESD89B
 - Same R5 MCU
 - Different Test design programs
 - FFT vs AES vs simple mem writes
 - $\sim 10^5$ difference in FIT
- Comparison of different MCUs
 - 5X different results
 - NSEU FIT (1MB):
 - 1,086 ~ 5,431
 - Parts offer 256KB ~ 4MB options
- SEFI observed! But not required to report
- Only SRAM and DRAM are mentioned
 - See next slide on flash results

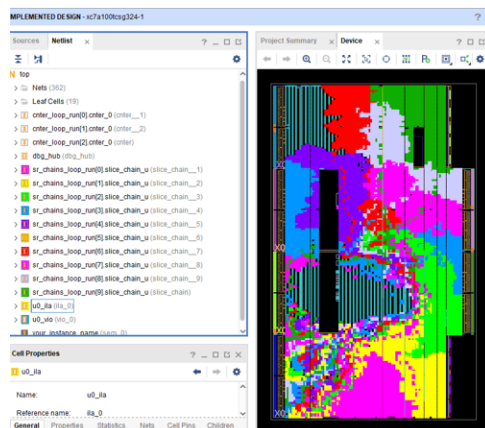
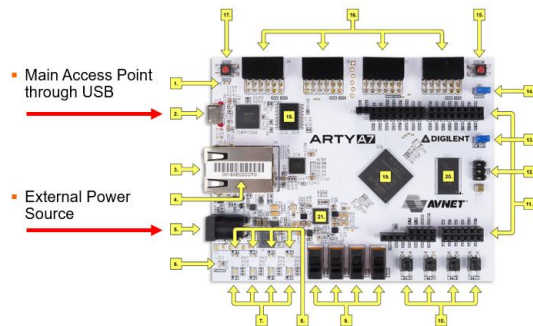
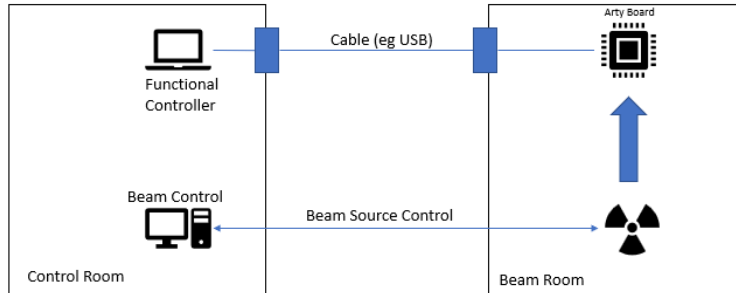


Part	SEU Bit Cross Section
microcontroller	$5 \times 10^{-14} \text{ cm}^2/\text{bit}$
microcontroller	$1 \times 10^{-14} \text{ cm}^2/\text{bit}$
microcontroller	$1 \times 10^{-14} \text{ cm}^2/\text{bit}$
microcontroller	$1 \times 10^{-14} \text{ cm}^2/\text{bit}$

— Memories FIT – Accelerated Test Data on Flash

Manufacturer	Array size	Technology	# of tested devices	Logic level	cross section (cm ²)	cell FIT per Gbit (without ECC)
A	8Gbit	FG NAND, MLC 65nm	14	00	8.53×10^{-19}	11.9
				01	2.31×10^{-18}	32.3
				10	9.61×10^{-19}	13.5
				11	4.14×10^{-21}	0.1
B	8Gbit	FG NAND, MLC 90nm	13	00	3.53×10^{-18}	50.2
				01	3.33×10^{-18}	46.6
				10	3.82×10^{-20}	0.5
				11	4.14×10^{-21}	0.1
B	4Gbit	FG NAND, MLC 65nm	18	00	4.30×10^{-18}	60.2
				01	4.45×10^{-18}	62.2
				10	3.55×10^{-20}	0.5
				11	0	0.0
B	4Gbit	FG NAND, SLC 65nm	13	00	1.91×10^{-21}	0.0
C	8Gbit	FG NAND, MLC 70nm	4	00	1.12×10^{-17}	157.5
				01	7.94×10^{-18}	111.2
				10	9.94×10^{-20}	1.4
				11	0	0.0
D	512Mbit	Nitride trapping NAND 90nm	8	0	7.21×10^{-19}	10.1

— SRAM is Weaker than ASICs?



2 FT2232H Block Diagram

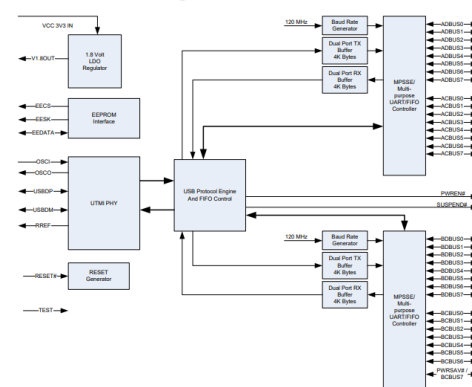


Figure 2.1 FT2232H Block Diagram

- Arty Board tested at NARI
 - 7A100T: ~183,637,824* transistors
 - FT2232: ~ 2,000,000** transistors
- Failure modes
 - 7A100T: All failures can be recovered and mitigated via design
 - FT2232: SEFI observed. Require power cycling
- It's not the technology, it's if you have done something about it!

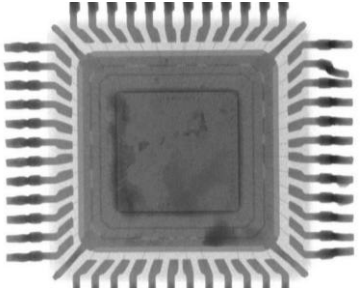
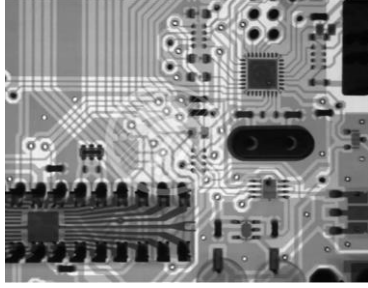
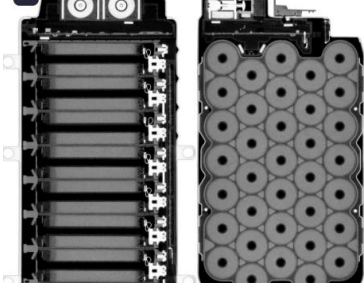
— Process Variation

- ★ Accelerated test prediction
 - JESD89B (Neutron & Alpha)
 - AMD (Xilinx) UG116
- ★ Environmental prediction
 - Rossetta Test
- ★ In 1998, SEU ~20% of all “could-not-duplicate” errors
- ★ Intel/Cisco/TI/Xilinx, etc. all have dedicated team performing tests



Tech Node	Product Family	LANSCE Neutron Cross-Section per Bit ²		FIT/Mb (Thermal Neutrons)		FIT/Mb (Alpha Particle) ³		FIT/Mb ⁴ (Real-Time Soft Error Rate Per Event) ^{5,7}	
		CRAM	Error	CRAM	Error ⁴	CRAM	Error ⁵	CRAM	Error ⁶
90 nm	Virtex 4	1.55 x 10 ⁻¹⁴	±18%					263	±11%
90 nm	Spartan 3	2.40 x 10 ⁻¹⁴	±18%					190	-50% +80%
90 nm	Spartan 3E, Spartan 3A	1.31 x 10 ⁻¹⁴	±18%					104	-80% +90%
65 nm	Virtex 5	6.70 x 10 ⁻¹⁵	±18%					165	-13% +15%
45 nm	Spartan 6	1.00 x 10 ⁻¹⁴	±18%	21	-11% +13%	88 Foil	-50% +100%	177	-10% +11%
40 nm	Virtex 6	1.26 x 10 ⁻¹⁴	±18%	0.7	-11% +13%	7 Cave	-45% +97%	105	-10% +11%
28 nm	Artix 7, Spartan 7, and Zynq 7000	6.99 x 10 ⁻¹⁵	±18%	29	-10% +10%	50 Foil	-34% +56%	74 28nm	-8% +9%
28 nm	Kintex 7 and Virtex 7	5.69 x 10 ⁻¹⁵	±18%	1.1	-15% +18%	50	-34% +56%	40	-17% +21%
20 nm	UltraScale	2.55 x 10 ⁻¹⁵	±18%	0.5	-13% +16%	9	-64% +374%	32	-10% +12%
16 nm	UltraScale+	2.67 x 10 ⁻¹⁶	±18%	0.35	-16% +20%	0.1	-20% +20%	5	-15% +18%
7 nm	Versal	2.6 x 10 ⁻¹⁷	±20%	0.1	±50%	0.1 Cave	±50%	0.33	-51% +129%

X-Ray Induced TID Not Considered – AI Assisted

					
Prod. Tier	<u>Tier-2 (Semiconductor)</u>	<u>Tier-1 (ECU/Module)</u>	Tier-1 (EV Power)	<u>OEM (Assembly)</u>	<u>OEM (Final Veh.)</u>
Scan Purpose	• Die-attach • wire bond • packaging integrity	• PCB assembly • BGA solder joints • housing	• IGBT/SiC voiding in heavy copper modules	• Battery cell alignment • Structural welds	• Logistics check • missing parts • "End of Line"
Inspection Type	High-res 2D / Micro-CT	Automated 3D (AXI)	High-Energy 3D CT	Inline CT / 2D	Drive-through X-ray
Expected Dose (per scan)	1 – 10 rad	10 – 200 rad	200 – 500 rad	50 – 300 rad	< 0.001 rad
Equivalent in krad	0.001 – 0.01 krad	0.01 – 0.2 krad	0.2 – 0.5 krad	0.05 – 0.3 krad	< 0.000001 krad

— Known TID Effects on Semiconductors

- Degradation of IC
 - Shifting threshold & increased leakage
 - Ex. Memory may suffer alter retention margins or latent reliability impacts
 - Tail bits fall out of spec driven device failure
 - Refresh time of tail bits may degrade beyond data sheet spec due to charge leakage
 - Thermal annealing can lead to “some” recovery – but not total recovery
- Known failure at low TID
 - DRAM* at 120 rad (0.12Gy)
 - HBM anyone?
 - Is **0.55% (5,500 PPM)** acceptable for your customer?

Vendor	Technology Platform	Failure Rate	
		120 Rad	480 Rad
A	0.18	<0.01%	0.6%
B	0.13	0.55%	7.8%
C1	0.13	<0.01%	<0.01%
C2	0.11	<0.01%	3.6%
D	0.13	0.13%	2.8%
E	0.13	<0.01%	<0.01%
F	0.09	<0.01%	<0.01%

Device / Cell Type	Primary Radiation-Induced Failure Mode
SRAM / DRAM	Increased standby supply current, data retention failure
Flash Memory	Charge loss in floating gate, erase/write timing degradation
Analog / Mixed Signal	Offset voltage shift, degraded signal-to-noise ratio, "ghosting"
High-Voltage Power	Decreased breakdown voltage, increased leakage
Advanced FinFET	Parasitic lateral conduction, subthreshold leakage



Steps to Take

Actions for Consideration - SER

- Updating Appendix and Table information
 - Limit alpha material problem to packaging
 - Remove JESD89-2A – Refer to UG116 Foil vs Cave numbers
 - Packaging to provide Alpha emissivity report is sufficient
 - Remove >1Mb SRAM and DRAM note and allow tier-1/suppliers to work out necessity
 - Flash, regular FF, MAC already proven to be significant contributors.
- Addendum/Appendix on metrics/test programs/failures
 - Accelerated NSEU test for general purpose IC
 - Recommend standardized test program and pattern (MCU, AI, memory)
 - SER need to include failure information, especially SEFI

— Actions for Consideration - TID

- Item to be added to AEC-Q100
- Test Standard
 - JESD22-B121
- Process to track the accumulated dosage and data hand-over
 - Starting from foundry, track and analyze.
 - Validate dose tracking from machine vs part
- Minimize effect
 - Reduce exposure and/or adjust X-ray parameter
 - Publish recommended guidelines
 - 100 rad (0.1Gy)
 - Ex. NXP AN13412, Renesas TID_QER_2310-009
 - Avoid known vulnerability
 - Reduced shielding: Memory-on-package, Thin package, direct-die
 - Known technique
 - Reduce dose: Integrated heat spreader, thick substrate



Questions?

Wei.Tseng@sgs.com

+886 0974-054-649

www.sgs.com/

