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AUTOMOTIVE ZERO DEFECTS FRAMEWORK

CASEBOOK EXAMPLES

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TABLE OF CONTENTS

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AUTOMOTIVE ZERO DEFECTS FRAMEWORK - CASEBOOK EXAMPLES

1. SCOPE

This document is a general guide with examples of the most commonly used methods and practices in the automotive industry in use today to work toward zero defect products. It is a companion to and relies upon AEC – Q004 to provide specific interpretations of the various tools used to develop and maintain a "zero defect" process. This document is by no means an exhaustive reference of examples.

1.1 Purpose

The purpose of this Casebook of Examples is to provide initial guidance on the use of each tool described in the main document and give practical examples for illustration if applicable.

2. STRUCTURE OF INDIVIDUAL TOOL EXAMPLES

The numbering of the subsections is identical to those of the main AEC-Q004 document. For ease of use, each tool example is explained by a consistently applied structure of 4 subsections:

1. Background: Introduction to the topic from a practical perspective is given
2. Example(s): Where possible, real-life example(s) or illustration(s) is/are provided
3. Benefits: High-level overview of benefits for the user is given
4. References: List of publicly accessible references for further study is provided

2.1 Acronyms

Table 2 provides an overview of all acronyms used in this document

Table 2: list of Acronyms

Acronym	Description	Acronym	Description
AEC	Automotive Electronics Council	KEP	Key Electrical device and process Parameters
AIAG	Automotive Industry Action Group	MCM	Multi-Chip Module
AM	Acoustical Microscopy	MEMS	Micro-ElectroMechanical System
ANOVA	ANalysis Of VAriance	MSA	Measurement System Analysis
APQP	Advanced Product Quality Planning	MTP	Multiple Time Programmable
ASIC	Application Specific Integrated Circuit	NAND	Not-And Gate
ASSP	Application Specific Standard Product	NBTI	Negative Bias Temperature Instability
ATE	Automated Test Equipment	NIST	National Institute of Standards and Technology
ATPG	Automatic Test Pattern Generation	NNR	Near Neighborhood Residuals
BEOL	Back End Of Line, latter portion of IC fabrication consisting of interconnections through metallization layers.	NVRAM	Non-Volatile Random-Access Memory
BIST	Built In Self-Test	OCAP	Out-Of-Control Action Plan
BKM	Best Known Method	OEM	Original Equipment Manufacturer
BMY	Below Minimum Yield	OTP	One Time Programmable
BTS	Bias Temperature Stress	PAT	Part Average Test
CAA	Critical Area Analysis	PBTI	Positive Bias Temperature Instability
CDF	Cumulative Distribution Function	PC	PreConditioning
CMOS	Complementary Metal-Oxide-Semiconductor	PCB	Printed Circuit Board
CMP	Chemical & Mechanical Polishing	PCI	Process Change Information
CPU	Central Processing Unit	PCM	Process Control Monitor
DFA	Design For Analysis	PCN	Process Change Note/Notification

Table 2: list of Acronyms (continued)

Acronym	Description	Acronym	Description
DFM	Design For Manufacturability	PDK	Process Design Kit
DFMEA	Design Failure Mode & Effects Analysis	PFMEA	Process Failure Mode & Effects Analysis
DFR	Design For Reliability	PID	Plasma Induced Charging
DFT	Design For Test	PMOS	P-channel Metal-Oxide-Semiconductor
DOE	Design Of Experiment	POC	Power On Clear
DPAT	Dynamic Part Average Testing	PoF	Physics of Failure
DUT	Device Under Test	POR	Power On Reset
ECU	Electronic Control Unit	PPAP	Production Part Approval Process
EEPROM	Electrically Erasable Programmable Read Only Memory	PPB	Parts Per Billion
EIPD	Electrically Induced Physical Damage	PVT	Process Voltage Temperature
EM	ElectroMigration	QFN	Quad Flat No lead
EV	Electric Vehicle	QFP	Quad Flat Package
FA	Failure Analysis	QM	Quality Management
FEOL	Front-End-Of-Line (FEOL): Beginning of wafer processing in the Fab that makes the transistors, capacitors and resistors.	RAM	Random Access Memory
FIB	Focused Ion Beam	Ringo	Ring oscillator
FMEA	Failure Mode & Effects Analysis	RF	Radio Frequency
fWLR	fast Wafer Level Reliability	ROM	Read-Only Memory
FTA	Fault Tree Analysis	SBA	Statistical Bin Analysis
GDBC	Good Die in Bad Cluster	SBL	Statistical Bin Limit
GDBN	Good Die Bad Neighborhood	SHOVE	SHort OVervoltage Elevation
GR&R	Gage Repeatability & Reproducibility	SPAT	Static Part Average Testing
HTOL	High Temperature Operating Life	SPC	Statistical Process Control
HTSL	High Temperature Storage Life	SYL	Statistical Yield Limit
HV(ST)	High Voltage (Stress Test)	TDDB	Time Dependent Dielectric Breakdown
IATF	International Automotive Task Force	TC	Temperature Cycling
IC	Integrated Circuit	THB	Temperature Humidity Bias
IDDQ	IDD Quiescent current	TMP	Temperature Mission Profile
IEEE	Institute Of Electrical and Electronics Engineers	TPMS	Tire Pressure Measurement System
ILD	Inter-Level Dielectric	TTF	Time To Failure
IMC	Inter-Metallic Compound	ULPY	Unit Level Predictive Yield
IMD	Intra-Metal Dielectric	VDA	Verband Der Automobilindustrie
IN	Information Note	VLVT	Very Low Voltage Testing
IQC	Incoming Quality Control	WLR	Wafer Level Reliability
IRC	Internal RC (Resistor Capacitor)	ZD	Zero Defect
ISSQ	ISS Quiescent current	ZVEI	Zentralverband Elektrotechnik- und Elektronikindustrie
JEDEC	Joint Electron Device Engineering Council		

3. PRODUCT DESIGN

3.1 Design Failure Mode and Effect Analysis (DFMEA)

3.1.1 Background

The activity of defining a DFMEA is complementary to the process of designing a product. FMEA is focusing on what potentially could go wrong in a product. A failure mode is the way in which an element fails to perform its intended function (permanently or temporarily). Potential non-intended side effects should also be identified and rated. A team of subject matter experts is needed to identify all risks, causes and effects. Before starting the DFMEA activity, the scope, a description of the process, and its specifications are needed.

3.1.2 Example(s)

The example in Fig. 3.1.2-1 only shows the results of the functional analysis, failure analysis, and risk analysis. The preparation and the improvement actions are not given.

	Structure Analysis (STEP2)			Function Analysis (STEP3)		
No./ID.	**1. Next Higher Level**	**2. Focus Element**	**3. Next Lower Level or Characteristic Type**	**1. Next Higher Level Function and Requirement**	**2. Function of Focus Element and Product Characteristic**	**3. Next Lower Level Function and Requirement or Characteristic**
Band Gap						
X	SoC	Bandgap	Bandgap reference voltage	Power management	Voltage reference	Bandgap accuracy

1

	Failure Analysis (STEP4)				Risk Analysis (STEP5)						
No./ID.	**1. Failure Effects (FE) to the Next Higher Level Element and/or Vehicle EndUser**	**Severity (S) of FE**	**2. Failure Mode (FM) of the Focus Element**	**3. Failure Cause (FC) of the Next Lower Element or Characteristic**	**Current Prevention Control (PC) of FC**	**Occurrence (O) of FC**	**Current Detection Controls (DC) of FC or FM**	**Detection (D) of FC/FM**	**DFMEA AP**	**Special Characteristic / Classification**	**Filter code (Optional)**
X	ldo/DCDC regulators output voltage accuracy degraded, potentially out of specification	7	Deviation at low temperature, larger spread at Cold Temp	Silicon results are not matching simulations. Multiple hypothesis not fully demonstrated today: - Parasitic MOSFET in subthreshold region is not modeled in wafer technology - Poor modeling of BIPOLAR close to saturation region	- New optimized and less sensitive design with better matching of current mirror Vds - Improve simulation models	7	Check ATE data	2	**H**		

2

3

	Optimization (STEP6)											
No./ID.	**DFMEA Preventive Action**	**DFMEA Detection Action**	**Responsible Person's Name**	**Target Completion Date**	**Status of Action**	**Action Taken with Evidence**	**Completion Date**	**[S] Severity**	**[O] Occurrence**	**[D] Detection**	**DFMEA AP**	**Remarks**
X	Re design of BandGap with improved matching	Check ATE data with new design at Tri-temp (R,H,C)	xyz	yy/mm/dd	In Progress	tbd	tbd	tbd	tbd	tnd	tbd	

4

Figure 3.1.2-1: part of DFMEA for specific circuit block; planning & preparation (STEP 1) and results documentation (STEP 7) are not shown.

3.1.3 Benefits

1. Users are protected against failing parts due to design flaws.
2. Root causes of potential failures are identified and can be solved.
3. Effects of potential failures can be detected more effectively and acted upon.
4. Priority setting of risks to work on first.

3.1.4 References

[3.1.4.1] https://www.aiag.org/ search for “AIAG & VDA FMEA Handbook”

3.2 Redundancy

3.2.1 Background

With respect to zero defect, redundancy is a tool to overcome certain limitations in manufacturability or reliability of single base elements of a technology. This might be a single device on an IC or a specific part of the BEOL structure. In most cases, this becomes relevant if the product is of high complexity and the base element is used in the product many million times. Especially when the failure of one of these base elements may lead directly to a functional failure on product level, this may result in product level failure rate or yield loss in the percentage range. An appropriate countermeasure in that case is to include spare basic structural elements at critical position to compensate for potential manufacturing defects causing yield loss or an early wear out failure causing a field failure.

3.2.2 Example(s)

a. A common example for yield improvement by redundancy is the insertion of redundant vias. There is an unneglectable risk of not completely filled vias which leads to yield loss and might also be cause for latent defects. Redundant vias reduce the risk of a single via failure by the square of the single via failure probability (e.g., if a single via fails with a probability of $1{:}10^{9}$ the double via structure fails with a probability of $1{:}10^{9\times2}=1{:}10^{18}$). Depending on the complexity of the product, this might move the yield loss from the percentage range to the ppm range or below.

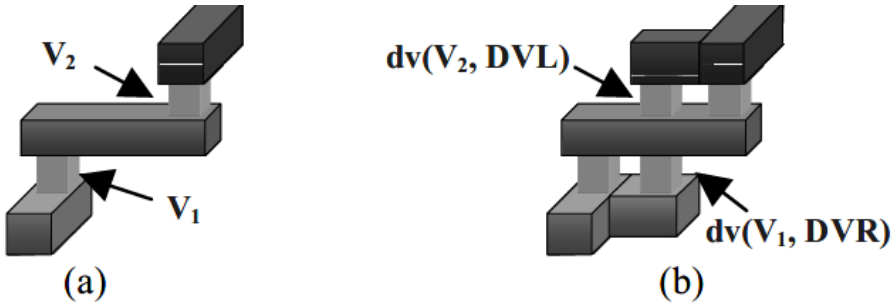


Figure 3.2.2-1: single via structure (a) vs. double via structure (b) in the metal routing of an integrated circuit [3.2.4.1]

b. Modern NAND Flash Devices suffer from even sub-PPB failure rates of single cells with respect to the whole device reliability and yield performance. Redundancy and replacement of bad cells or typically blocks containing one or more bad cells is a common practice. This is done before delivery as well as during operation once the memory controller identifies a block failing during read or write operation. The block is then replaced by a spare block by changing the address table.

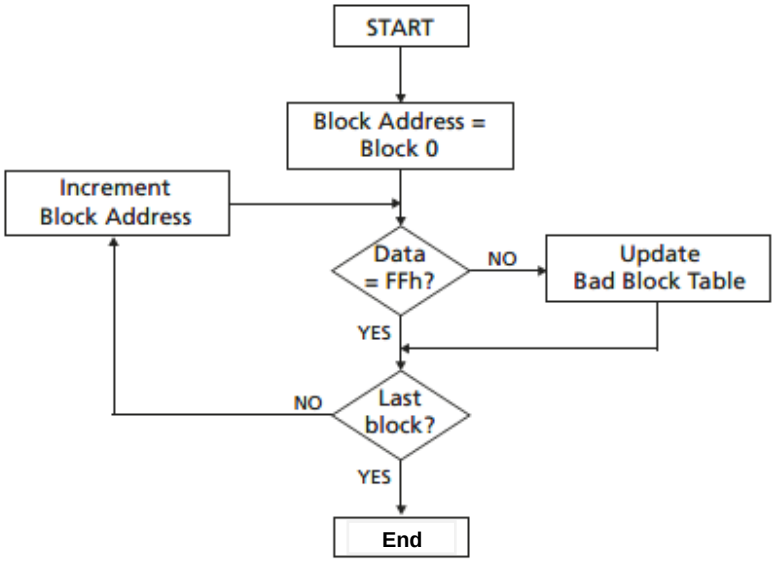


Figure 3.2.2-2: NAND Flash bad block management flow chart [3.2.4.2]

3.2.3 Benefits

Redundancy on base element level of complex integrated circuits may lead to decreasing yield loss and field failure rates on product level by orders of magnitude. The additional die area is a trade-off for increased reliability and yield performance. Therefore, the decision for using a certain level of redundancy needs to be strongly correlated to the product complexity.

3.2.4 References

[3.2.4.1] Kuang-Yao Lee, Ting-Chi Wang, “Post-Routing Redundant Via Insertion for Yield/Reliability Improvement”, Asia and South Pacific Conference on Design Automation, 3C-1, 2006.
[3.2.4.2] Micron Technical Note TN-29-59 “Bad Block Management in NAND Flash Memory”, https://www.micron.com/; search for “TN-29-59”.

3.3 Built-In Self Test (BIST)

3.3.1 Background

This section is mainly related to IC being qualified under AEC-Q100 (IC) and AEC-Q104 (MCM). BIST serves two purposes:

a. Reduce escape of defects by improving test coverage. BIST can help to test (internal) blocks and functions of IC that are very difficult to test from outside.

b. Provide run-time test coverage (especially when used in mission critical or safety related applications). In this use-case, it must be ensured that all parts of the IC are working as designed/intended at runtime or startup.

When BIST is implemented, effective electrical failure analysis might be compromised if no precautions are taken. Therefore, it is recommended to implement an option to bypass BIST in a special characterization test mode.

3.3.2 Example(s)

There is no generic “best practice” or mandatory implementation as the zero-defect guideline applies to many different component types. For complex ICs or multi-die modules, possible BIST examples are:

- Self-test of internal references and signals (supply voltage, internally generated voltages, and oscillators).
- Power-On reset (POR) or Power-on-clear (POC) functionality verification.
- LBIST (Logic BIST) targets logic modules like processor/CPU, watchdog or interrupts.
- MBIST (Memory BIST) was developed specifically for memory modules like ROM, RAM or nonvolatile memories like OTP, MTP, EEPROM or Flash. Here several algorithms can be run to verify memory functionality or test for memory faults.
- Self-test of analogue or mixed-signal blocks (e.g., signal chain verification with known stimulus and verification of expected response).
- Depending on device complexity (e.g., a processor) even boundary scan can be implemented as BIST.
- A loopback test (feedback transmit signal into receive path and confirm data is identical) could be done on transceiver devices.

3.3.3 Benefits

For the user, the application of runtime BIST could also cover runtime test requirements (e.g., functional safety requirements according to ISO26262). To test intended functionality additional on-chip hardware might be required. For application / customer specific IC developments, user and supplier should agree on the required coverage of individual BIST for ATE testing, device startup and device runtime at the beginning of a new project.

3.3.4 References

No public reference found.

3.4 Design for Test (DFT)

3.4.1 Background

The main purpose of DFT is to ensure the effectiveness of test coverage during ATE in mass production. The field of DFT was and is the subject of intense research as the complexity of ICs and applications is growing. It must be highlighted that DFT is not a single measure, test or method. It is always a combination of tests & methods (see examples in section 3.4.2).

3.4.2 Example(s)

The list of examples provided here can only scratch the surface of the topic:

- Scan-chain design implementation to enable ATPG (automated test pattern generation) test (see AEC-Q100-007 for details).
- Implement BIST (see Section 3.3).
- Boundary scan implementation according to IEEE 1149.1.
- Enable HV stress testing. This could be achieved by either bypassing on-chip regulators or changing voltage settings as needed for an effective stress.
- Availability of internal signal on outside pins by switching pin functionality in test mode (Figure 3.4.2-1).

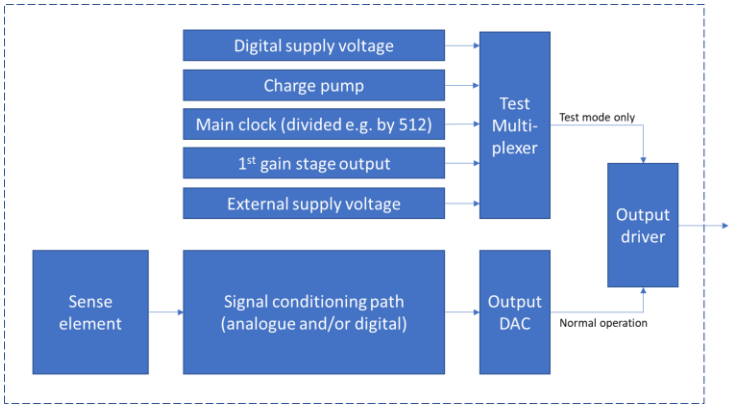


Figure 3.4.2-1: internal test multiplexer example

3.4.3 Benefits

The main benefit of implementing DFT measures is a more effective test coverage during mass production testing, which in turn can support a trend to zero-defect quality. However, there might be secondary benefits such as:

- support of the failure analysis process as internal blocks and nodes can be measured individually (overlap with chapter 3.5).

These benefits need to be weighed against additional development time/cost and silicon area.

3.4.4 References

[3.4.4.1] https://www.ieee.org/; search for ”IEEE 1149.1”.
[3.4.4.2] http://www.aecouncil.com/; search for “Q100-007”.

3.5 Design for Analysis (DFA)

3.5.1 Background

Failure analysis (FA) aims at finding the physical root cause of a device failure. For complex IC many blocks and signals are only available internally to the IC. To enable in-depth failure analysis process, access must be provided to measure these internal signals in various blocks. DFA is not a single design measure or implementation. To obtain good analysis access, it will most likely be a combination of measures and implementation (depending on IC complexity).

3.5.2 Example(s)

Some best practice examples are:

- Add test pads for internal supplies of ICs.
- Include internal signal in test multiplexers made available in test mode (Figure 3.5.2-1).
- Implement externally triggerable BIST routines (selective, allow looping).
- Route relevant signals (at least partially) in top metal layers so they are accessible to FIB (e.g., for placing FIB pads).
- Implement special (internal) registers and functions in digital IC for advanced testing.
- Add orientation marks in large, repetitive structures like RAM, ROM or EEPROM/NVRAM.

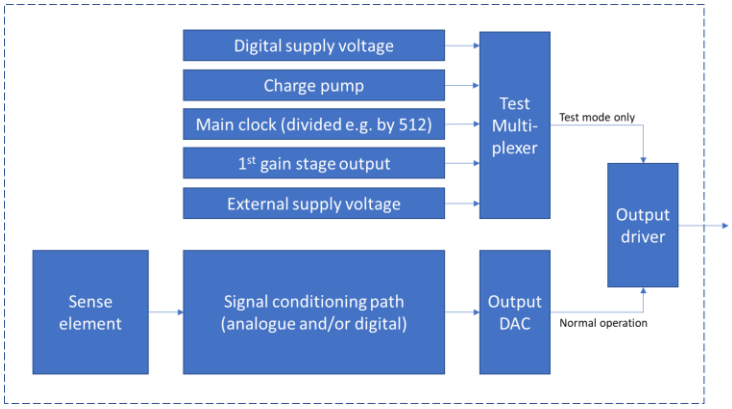


Figure 3.5.2-1: internal test multiplexer example.

3.5.3 Benefits

The benefit of implementing DFA measures is access to internal blocks for failure analysis. When the root cause of systematic and field failures is identified, proper measures can be implemented to attain zero defects. This benefit needs to be weighed against die-size restrictions for optimal pricing.

3.5.4 References

No public reference found.

3.6 Design for Manufacturability (DFM)

3.6.1 PART 1: Product Perspective

3.6.1.1 Background (Part 1)

Design For Manufacturability (DFM) is best practice actions taken during the product design phase, to ensure the product can be predictively manufactured and defect free. To design products to be more compatible with the process and equipment requires a good understanding of process windows and the integration of lessons learned from scrap or poor reliability. The mitigation strategies from lessons learned, which should be documented into the process design rules, and where possible coded into the design rule checking and simulation software or alternatively added to the PFMEA document (see section 4.1). Though DFM for IC manufacturing largely applies to fab processing, the Assembly and Test operations also deserve DFM consideration.

3.6.1.2 Example(s) (Part 1)

a) Parametric defect avoidance is achieved by accurate modeling of the process and IC layout parasitic due to interconnect series resistance and parallel line capacitance. The layout parasitic can be geometrically extracted from the layout and included back into the product simulation, and if needed the design or layout can be modified to compensate.
b) Critical Area Analysis (CAA) looks at IC layout to determine if there are areas sensitive to random particles. Where metal interconnects have long min-space parallel runs, spacing out the interconnects may provide better immunity to small defects. CAA should also look for areas where the vias or contacts are widely spaced or isolated. Increasing the density of vias or contacts in these areas or adding redundancy can reduce the occurrence of small, partial, or open vias or contacts, as well as a reduction in the parasitic series resistance which may be inadequately modeled in the isolated cases.

c) Antenna effect rules identify poly gates connected to large areas of metals and are intended to control the ratio of metal to gate area for reducing plasma charging effects during the metal etching process. A large metal to gate ratio can generate charge accumulation and damage to the gate oxide, sometimes manifesting as latent defects in the gate oxide.

d) Where space allows, design should not draw physical features at the minimum size. For example, a poly resistor drawn at minimum width, will have worse matching and greater variability than the same value resistor drawn at 2-4x minimum width. Increasing minimum feature size also applies to minimum metal/poly enclosure rules of contacts and vias; if the enclosure of a via or contact can be increased by even a small amount, the product will be more tolerant to layer-to-layer overlay mismatch, avoiding interconnect shorting or opens which may also cause latent failures.

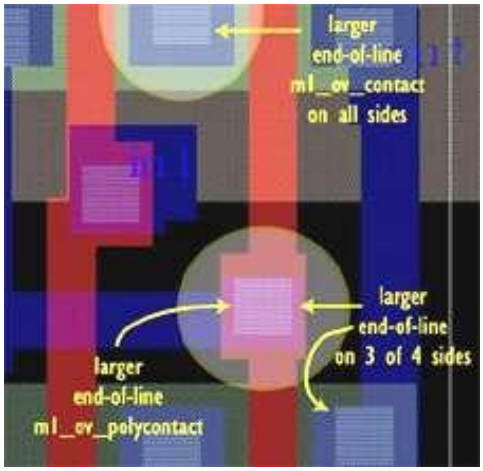


Figure 3.6.1-1: increased contact and via enclosure [3.6.4.1]

e) Pattern density gradient is especially important with processes using Chemical & Mechanical Polishing (CMP) for planarization but also has value with non-CMP processes. Identify high density areas next to low density areas and try to balance shapes to reach a homogeneous density. A dummy pattern fill can help balance the density gradient but can have detrimental process charging effects from the floating metal or poly patterns.

f) DFM examples for production test and assembly are rules for bond pad placement for providing probe needle clearance during wafer probe and proper clearances for wire bonding operations in assembly.

3.6.1.3 Benefits (Part 1)

DFM helps to avoid ‘Product to Process’ mismatch, which causes systematic yield loses and can lead to the delivery of marginal product to the customer. Incorporation of lessons learned from previous products into the DFM rules results in follow on products that are more compatible with the manufacturing environment, improving yield and reliability.

3.6.1.4 References (Part 1)

[3.6.4.1] P. De Dood, "Impact of DFM and RET on Standard-Cell Design Methodology," Proc. Electronic Design Processes Workshop, IEEE CS Press, 2003, pp. 62-69

3.6.2 PART 2: Process Perspective

3.6.2.1 Background (Part 2)

In Manufacturing Operations, DFM is error proofing the manufacturing flow, and installing mechanisms for detection of abnormal events. For error proofing, a key concept is Poka-Yoke or “Mistake Proofing”. The Poka-Yoke concept was formalized by Shigeo Shingo and introduced into manufacturing on the Toyota manufacturing line in the 1960’s. Poka-Yoke can be implemented at any point in the manufacturing process where a human error or equipment event may create opportunity for defective products to escape to the user. Opportunities for Poka-Yoke can be found by utilizing the PFMEA to identify operation steps where mistakes can have low detection or high severity, or by fanout of ‘Prevent Reoccurrence’ measures during the 7D step of an 8D for a customer return (see Section 8.1)

A second key element for DFM with Manufacturing Operations is the concept of 6S, which helps to eliminate misprocessing by keeping work areas uncluttered, orderly, and with a clear path for components and work in progress to flow. The 6S principles are a series of activities originally developed by Toyota as part of Lean manufacturing systems to help minimize waste, which contributes to errors and defects at the workplace. These principles are Sort, Set in Order, Shine, Standardize, Sustain, and Safety. Each step builds on the previous one to help achieve improved productivity and efficiency, while avoiding mixing material or missed steps in the operation.

Figure 3.6.2-1: 6S Concept [3.6.8.1]

3.6.2.2 Example(s) (Part 2)

Poka-Yoke:

a) Non-interchangeable or keyed connectors for ATE test hardware for preventing swapping of test sites (Figure 3.6.2-2).

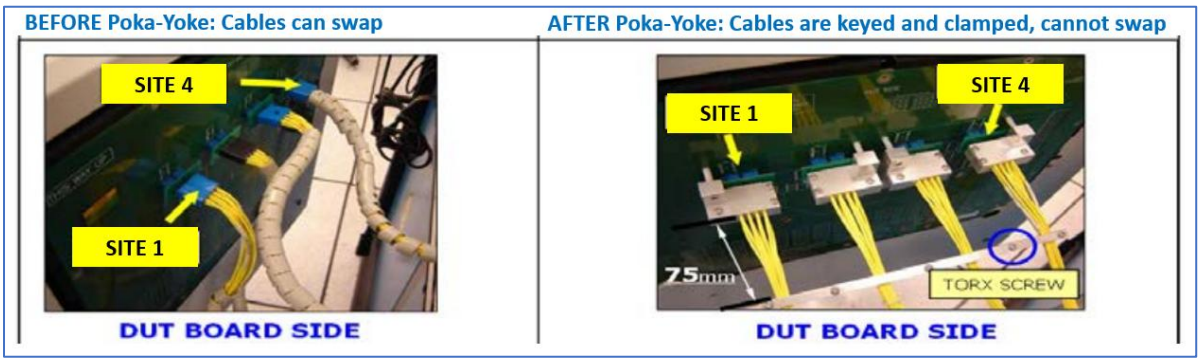


Figure 3.6.2-2: non-interchangeable or keyed connectors

b) Mechanical or electrical detection of a stuck unit in an ATE test socket, for preventing following units into the socket from piggybacking on the stuck unit and being binned as good but are untested.

3.6.2.3 Benefits (Part 2)

Mistake proofing and a clean orderly workspace will prevent mistakes and mis-processing from occurring or provide detection of the occurrence. Where possible a full automation approach should be applied to decrease 'Occurrence' or the 'Detection' score to the minimum in the PFMEA Action Priority Number (see Section 4.1).

3.6.2.4 References (Part 2)

[3.6.8.1] Shigeo Shingo, "Zero Quality Control: Source Inspection and the Poka-Yoke System"

3.7 Design for Reliability (DFR)

Design for Reliability (DFR) summarizes the efforts within the development process to design products that do not noticeably degrade and/or wear out during the projected service life of the OEM product while used as specified.

3.7.1 Background

DFR requires a systematic design approach that considers real-world usage expectations, constraints, loads, and the accurate application of Physics-of-Failure (PoF). It also necessitates a thorough understanding of process reliability and variation characteristics. An overly optimistic design approach may fail to prevent wear-out failures at the OEM level, especially towards the end of the product's service life. This section on DFR will:

- Demonstrate, through an example, how to utilize the combined knowledge and information from the Mission Profile to design or assess a product (or feature) and prevent the development of intrinsic failure mechanisms due to wear-out during the product's service life.
- Exclude discussions on extrinsic process and processing failure mechanisms, which are covered in other sections in this Case Book related to Design for Manufacturability (DFM), Design for Test (DFT) and Test Screen methodologies.

For many conventional automotive use cases, the application of inherited automotive design rules with sufficient design margins typically results in reliable products throughout the vehicle's service life. This has been proven with the AEC-Q10x qualification approach. However, for new automotive applications with extended stress and lifetime requirements, it is advisable to perform a Mission Profile-aware numeric assessment of the design rules, at least to the critical elements. This assumes that the supplier is aware of the Mission Profile or can make experience-based assumptions about it.

This approach enables the assessor to generate numeric predictions for the evolution of the selected parameters regarding the materials/processes intended for the future product when exposed to the stresses as described in the Mission Profile. The results allow for drawing upfront conclusions about capability, feasibility, weakness, and margins of the materials, processes, and design rules for creating a reliable product.

If the designed product is used according to its datasheet, it will perform without failure or noticeable degradation under real-world conditions meeting the specified functionality, reliability, and other requirements set by the designing and producing organization assuming the manufacturing process achieves the intended failure rates.

3.7.2 Example(s)

This case study aims to demonstrate the principles of Design for Reliability (DFR) by focusing on the design of a critical conductor line within a chip's interconnect system, taking into account the reliability requirements derived from the stress budget of the Temperature Mission Profile (TMP). The primary failure mechanism considered is Electromigration (EM), and the analysis is performed numerically using Black's Equation [3.7.2-1].

The objective of this example is to encourage open discussion throughout the supply chain, from suppliers to the Original Equipment Manufacturer (OEM). The goal is to collaboratively identify and develop the most feasible and optimal trade-off solutions for all parties involved and finally obtain a reliable solution for the end customer. The numbers used in this example are arbitrary and intended solely for illustrative purposes
The calculation is based on Black's Equation, where the current density (J) is replaced by the current (I) flowing through the conductor's cross-section, which is defined by its width (w) and thickness (th).

The equation is given by:

$$t_{TF} = A_o \times \left(\frac{I}{w \ x \ th}\right)^{-n} \times e^{Ea/kT} \qquad \text{(Eq. 3.7.2-1)}$$

where:
t_{TF} time to failure
k Boltzmann's constant (8.61733 x 10^{-5} eV)
T temperature in K
A_o material constant, depending on the assessed technology, failure: criteria, level, threshold
n material constant
E_a activation energy in eV; specific for the chosen technology / conductor system
I current flowing through the conductor
w width of the conductor
th thickness of the conductor

The assessed use case represents a TMP shown in the Table 3.7.2-1.

Table 3.7.2-1: Temperature Mission Profile (TMP)

Duty cycle in Active Mode %t(i)	Use Case Duration t(i)	Ambient Temperature T_a	Junction Temperature $T_j=T_a+\Delta T$ (ΔT: 35°C)	Acceleration Factor (for E_a=0.7eV)	Accelerated Duration (for T_j=185°C)
7%	1000 h	-40 °C	-5 °C	2.9E+05	0 h
10%	1500 h	25 °C	60 °C	7.7E+02	2 h
33%	5000 h	80 °C	115 °C	2.4E+01	204 h
47%	7000 h	120 °C	155 °C	3.5E+00	2021 h
3%	500 h	150 °C	185 °C	1.0 E+00	500 h
Total: 100%	Total: 15000 h		$T_{j\text{-}eff}$ = 145°C [1]		Total: 2727 h [2]

Notes:
Given the TMP in Table 3.7.2-1, one can calculate the ([1*]) effective junction temperature ($T_{j\text{-}eff}$ of 145°C) and the ([2*]) accelerated duration ($t_{acc\text{-}use}$ of 1500h) for the use case duration of 1500h. The TMP provides the duty cycle, ambient temperature, and junction temperature for different use cases.

Calculation of Effective Junction Temperature and Accelerated Duration
using the collected data during technology qualification:

T_{ref} Reference temperature: 185 °C
J_{max} Maximum current density at T_{ref}: 25 mA/um^2, with
w_{min} 0.14 um minimum allowed metal line, for
th 0.25 um conductor line thickness, specific to the arbitrarily defined technology
E_a activation energy: 0.7 eV
t_{budget} guaranteed time budget at T_{ref} and J_{max}: 2000 h

The total accelerated duration ($t_{acc\text{-}use}$) is calculated as 2727 hours, which is larger than the guaranteed time budget (t_{budget}) of 2000 hours. This indicates that the current design does not have sufficient robustness margin regarding EM:

$t_{budget} < t_{acc\text{-}use}$ (Eq. 3.7.2-2)

Design for Reliability (DFR) Options
to prevent EM during the projected service life

1. Scaling up the conductor line's width
   Increasing the width (w) of the conductor line reduces the current density, which can mitigate EM. However, this may lead to an increase in chip size.

2. Reducing Current Through the Metal Trace
   Decreasing the current (I) flowing through the conductor can reduce EM. This may require adjustments to the chip's parameters or behavior, necessitating agreement with users and the OEM.

3. Alternative Technology Options
   - Conductor Line Thickness: Increasing the thickness (th) of the conductor line can reduce current density.
   - Higher Activation Energy: Selecting a conductor material with a higher activation energy (E_a) can improve immunity against EM.
4. Improving the Cooling to reduce the Junction Temperature
   - At Semiconductor Manufacturer: Use a package with lower thermal resistance.
   - At Tier1: Implement an ECU construction with dedicated cooling concepts, such as passive/convection or active cooling systems.
   - At OEM: Position the ECU in a location with better cooling and less exposure to high temperatures, such as attaching it to a thermal drain on the vehicle chassis.
5. Reducing Temperature Stress/Duration
   Adjust the mission profile to reduce the duration of high-temperature exposure.

6. Service and Replacement Concept:
   If no other solutions are feasible, a practical service and replacement strategy for the affected ECUs/chips should be considered.

Conclusion
This example demonstrates the Design for Reliability (DFR) approach for a critical metal trace in a chip, focusing on preventing electromigration within a numerically defined environment, known as the Mission Profile. It serves as a foundation for discussions with stakeholders across the supply chain, highlighting potential options to explore if the initial approach proves impractical for ensuring the reliability of critical components. By embracing slight and feasible modifications, often cost-neutral for partners within the overall engineering system, a viable and reliable solution for existing technology can be identified, effectively mitigating the risk of electromigration for the considered metal trace.

In summary, understanding and mitigating the influencing factors of relevant stressors associated with a particular failure mechanism, combined with close collaboration across the supply chain, can lead to the best solution. The ultimate goal is to achieve the most feasible, reliable, robust, and efficient outcome.

This case study aims to serve as a practical example to foster collaboration and innovation in design for reliability, particularly in chip design, by considering the reliability requirements based on the real-world environment in which a chip will operate reliably throughout the entire projected service life of the OEM's product.

3.7.3 Benefits

- Prevent wear out failures in the field.
- Root causes of potential failures are identified and can be solved.
- Effects of potential failures can be detected more effectively and acted upon.
- Priority setting of risks to work on first.

3.7.4 References

[3.7.4.1] https://www.jedec.org; search for “JEP001”, “JEP122”
[3.7.4.2] https://www.zvei.org/; search for “Mission Profile”, “Robustness”

3.8 Simulation and Modeling

3.8.1 PART 1: Die Design

3.8.1.1 Background (Part 1)

Standard product qualification methodology is time consuming (mission profile dependent, where typically 1000 h HTOL is performed) and would be difficult to evaluate e.g., impact of process corners. Reliability simulation is therefore an indispensable tool to be deployed at early design phase as well as new product development phase. Reliability simulation can identify weak spots in the design or in parts of the design with respect to operational conditions and/or to product-to-product variation, because much more conditions and process fluctuations can be evaluated. It can also provide an invaluable information (circuit level detail) for failure analysis.

3.8.1.2 Example(s) (Part 1)

An example how this has helped to debug a HTOL fail using reliability simulation is described in this subsection (see Figure 3.8.2-1):

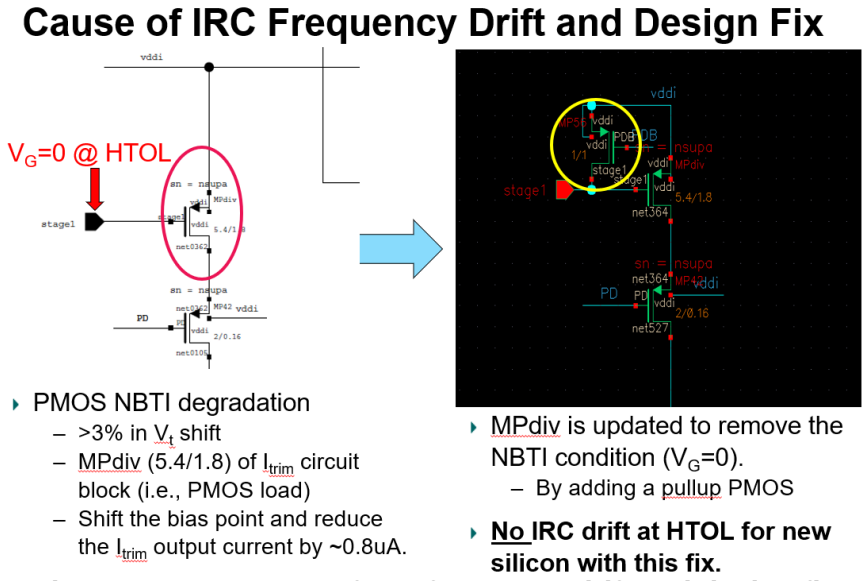


Figure 3.8.2-1: cause of IRC frequency drift and design fix

- A CMOS product’s IRC (Internal RC clock) has experienced a systematic ~ -1 MHz frequency degradation after 168 h HTOL at 150 °C (for 100% of HTOL samples).
- Reliability Simulation was able to produce similar frequency degradation, i.e., ~ -2 MHz at 150 °C for 168 h stress (note that initial NBTI model implementation did not include recovery effect that may account for the larger frequency degradation than what was observed).
- Reliability Simulation identified the root cause of the problem, i.e., I_{trim} current was reduced by ~0.8 µA due to PMOS NBTI degradation. This was caused by a GO1 PMOS transistor (in the I_{trim} block) which shows “degradation” in V_t (+3.4%).
- After the design fix, the new silicon has passed HTOL qualification: no frequency degradation.

3.8.1.3 Benefits (Part 1)

The above example illustrates a couple of clear benefits:

- Guarantee circuit reliability at design stage, before taping out.
  - "Design Rule based Design" may not be totally adequate or too restrictive), e.g., "keep below x Volts, and you'll be safe"
  - Performance and reliability trade-off (e.g., overdrive)
- Clear lifetime estimation in field reliability.
- A more efficient and effective qualification program.
  - Reduce delay due to "preventable" failures
  - Assess extreme mission profile (high temperature & overdrive) efficiently
- Design optimization by balancing application requirements and reliability margin.
- Root cause failure analysis.
  - Help to propose design solution

3.8.1.4 References (Part 1)

No public reference found.

3.8.2 PART 2: Package Design

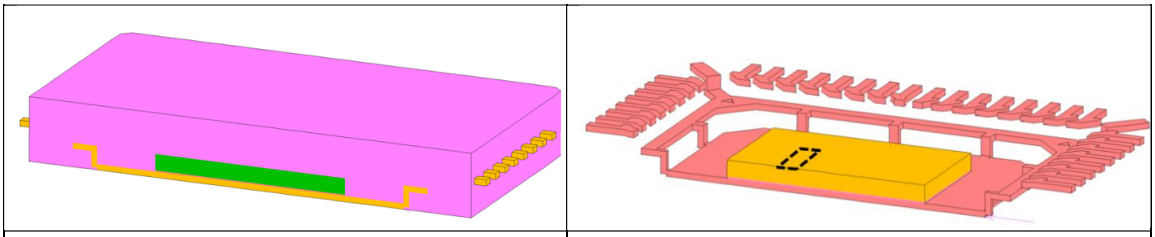
3.8.2.1 Background (Part 2)

The increased complexity and requirements in combination with the shorter time to market reduces the time available for physical prototyping of microelectronic systems. Building several iterations of the same product is not always an option. A validated simulation model can be used to quickly evaluate several designs or materials available and will thus reduce the required number of physical prototypes. From the simulation results the most promising options can be picked for physical prototyping. The physical prototype can be used to reaffirm that the model is correct and serve as physical evidence. Furthermore, simulation can be used to investigate the robustness of a given design by evaluating small changes in materials, load or geometry. The changes originate from batch-to-batch differences and normal spread in manufacturing. If the small changes result in significant differences in performance a non-robust optimum was found, and the design might need a revision. However, a model is only of merit if it is generated under appropriate assumptions and the results can be experimentally validated.

3.8.2.2 Example(s) (Part 2)

To reach high precision of high performance mixed-signal IC's trimming on wafer level or package level is commonly employed. Trimming is needed due to slight dimensional differences caused by process variation and small differences in mechanical stress between the products after packaging. The package, however, induces stress on the devices [3.8.8.1]. The piezo-electric effect, responsible for causing changes in electrical parameters due to mechanical stress has been studied extensively [3.8.8.2/3/4]. This stress typically does not lead to mechanical damage in the IC but can cause shifts in its electrical properties [3.8.8.5]. The amount of shift is dependent on the calibration point of the device during its manufacturing, the type of calibration used, the package construction and the type of environment the product is used in.

This example studies a method to decouple the effects of time-temperature dependent stress state caused by organic materials in the IC package. Typical processes after product manufacturing, such as solder reflow, will influence the package materials and will therefore cause a change in the mechanical stress state. In this example, all explored solutions involve a stacked die construction using die attach film. The circuit without stacked die as stress buffer is used as reference for the baseline electrical shifts. Key areas of investigation are the top die geometrical properties and its placement. A half symmetry finite element model is created for the QFP packaged with the die centered inside, see Figure 3.8.6-1.



a. half symmetry model of the 64-lead LQFP package with exposed pad used in this study	b. model with the epoxy mold compound hidden, the area of electrical interest is indicated with the dashed lines

Figure 3.8.6-1: HLQFP64 finite element baseline model without stacked die stress buffer

The model uses viscoelastic material data for the epoxy mold compound. The model is subjected to three reflow cycles. Results after the three reflow cycles are compared to results prior to the three reflow cycles yielding a certain drift in parameters. This drift could for example occur after the part is mounted on a PCB. The response of interest from the model in Figure 3.8.6-1 is the impact of the mechanical construction and its deformation over time and temperature on the electrical performance. For this a coupling between stress and electrical performance is needed. The general formula for piezo resistivity:

$$\Delta R/R=\pi_L \cdot \sigma_{xx}+\pi_T \cdot \sigma_{yy}+\pi_{out} \cdot \sigma_{zz},$$

is well known and many studies report coefficients [3.8.8.6]. Here σ_{xx}, σ_{yy} and σ_{zz} are the three stress components, and π_L denotes the longitudinal, π_T the transverse and π_{out} the out-of-plane piezo resistive coefficients, where the device is designed in the xy-plane and that current is flowing in the x-direction. The stacked die under investigation and the three parameters available for optimization are indicated by the arrows in Figure 3.8.6-2.

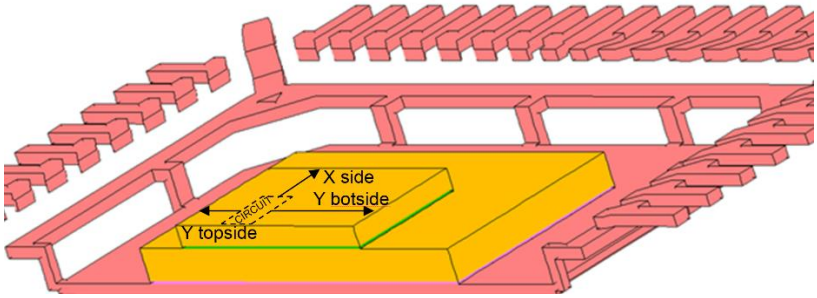


Figure 3.8.6-2: modified model (epoxy mold compound hidden) with the stacked die applied. Three parameters for optimization are defined initially

The goal of the evaluation is to find a stacked die that is effective with the smallest size possible. To reach this a Latin Hypercube numerical experiment is used containing 50 points including the nominal point. From the results a response surface is constructed after which an optimization step is used to find an optimum. This optimization step takes the expected device performance into consideration but also weighs in the cost of the stress buffer die where a larger die leads to higher cost. From the results of the simulations, four cases are selected for manufacturing: 1) Control without stress buffer 2) Largest top die possible 3) Optimum top die size 4) Minimum top die size

In case of the largest die some changes are made such that enough clearance is created between the wire bonds and the top die. The smallest top die possible is slightly increased in size to account for placement tolerances. Experimental results indicate that the best results are obtained with the optimum die and largest die but at a lower magnitude than predicted by the model. The smallest stacked die and control legs behave the worst.

3.8.2.3 Benefits (Part 2)

First, simulation models generate results faster than physical test. The second advantage is the freedom of design and material choice. Simulation can consider many different materials, without considering physical availability or other real-life limitations such as chemical compatibility. Besides, simulations allow for evaluation of many different designs while in reality the tooling costs would typically not allow for this.

3.8.2.4 References (Part 2)

[3.8.8.1] W.D. van Driel et al, “On chip-package stress interaction” Microelectronics Reliability, 48, 2008, pp 1268-1272.

[3.8.8.2] Y. Sun, S.E. Thompson and T. Nishida, Strain Effect in Semiconductors, Springer (2010).

[3.8.8.3] R. van Dalen, H.P. Tuinhout et al, “A methodology to predict the impact of Wafer Level Chip Scale Package stress on high-precision circuits” 2015 IEEE International Electron Devices Meeting (IEDM), Washington, DC, 2015.

[3.8.8.4] J.C. Suhling et al, “Application of stress sensing test chips to area array packaging” EuroSimE 2009 - 10th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems, Delft, 2009.

[3.8.8.5] O. Slattery et al, “Methods of analyzing thermomechanical stress in plastic packages for integrated circuits,” J. Mat. Proc. Tech, Vol 54(1-4), October 1995, pp 199-204.

[3.8.8.6] P.J. French and A.G.R. Evans, "Piezoresistance in polysilicon and its applications to strain gauges”, Solid-State Electronics Vol. 32, No. 1, 1989, pp. I-10.

3.9 Characterization

3.9.1 Background

Characterization comprises different test methods. Below are some examples where characterization can be used. The goal of this section is to show common interpretations of the term so user and supplier can make clear agreements.

3.9.2 Example(s)

Possible understanding of the term “characterization”:

- ATE (automated test equipment) packaged part testing.
- ATE Wafer level testing / probing, includes corner/matrix lots in wafer fab (with the aim to confirm data sheet compliance over PVT (process, voltage, temperature).
- Bench level electrical testing.
- Special tests (depending on application, e.g., high precision ambient temperature application in oil bath, bend/indent testing on packaged components, ultra-high frequency testing, time domain reflectometry).
- Destructive testing (e.g., burst pressure testing for MEMS pressure sensor dies).
- Wafer fab release (process) testing (current, voltage, capacitance, resistance, TDDB, EM, etc. according to JP001A).
- Assembly process testing (wire bond pull, wire bond shear, PC, TC, etc.).
- Process corner lot testing allowing test over PVT (process, voltage, temperature).

Depending on the delivery type of the final product (e.g., packaged part, bare die, flip chip) the characterization plan needs to be set up to enable testing of all datasheet and supplier internally needed parameters. For user-specific products this might be done jointly (depending on supplier/user agreements). Data output (examples):

- Capability reports (assuming gaussian distribution).

- Datasheet parameter limits (before product release).
- Distribution plots.
- Shmoo plots or other correlation plots.
- Safe operating area.
- Specification compliance matrix. Completion of the compliance matrix is commonly achieved using a mix of different data sources (e.g., bench testing, wafer probe data and packaged part test data).

3.9.3 Benefits

Both user and supplier gain extensive knowledge on the device to be released for mass production and the production processes. This allows for example to define test parameters more accurately, trim production processes and (together with qualification results) a prediction of field quality performance.

3.9.4 References

[3.9.4.1] http://www.aecouncil.com/; search for “Q003” (focus on IC)
[3.9.4.2] http://www.aecouncil.com/; search for “Q100-009” (IC only)
[3.9.4.3] https://www.jedec.org/; search for “Characterization” (IC only)

4. MANUFACTURING

4.1 Process Failure Mode and Effect Analysis (PFMEA)

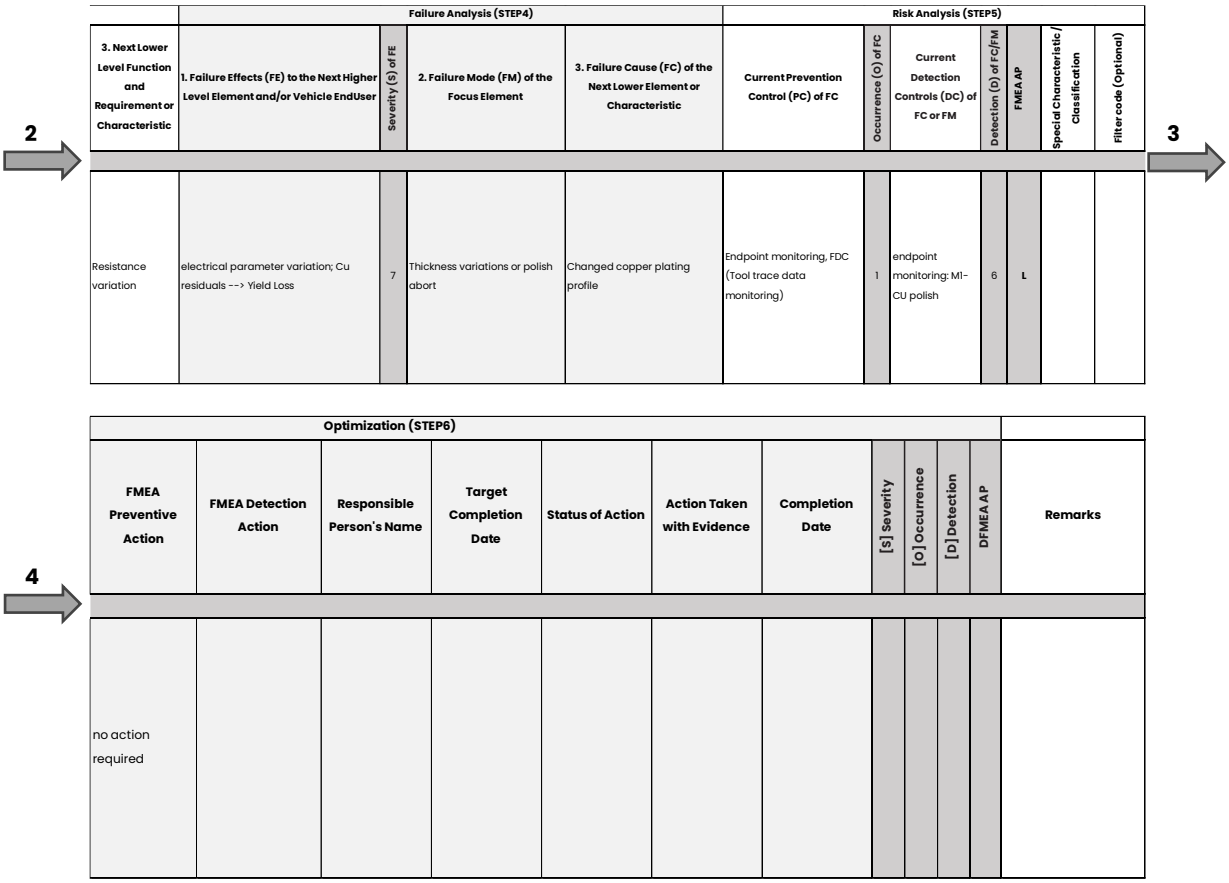
4.1.1 Background

The activity of defining a PFMEA is complementary to the process of designing a process. PFMEA is focusing on what potentially could go wrong in a process or a process step. A failure mode is identified when a function is not performing at all as intended by design or not preforming properly (too much, too little, non-uniform, not consistent, etc.). Potential non-intended side effects should also be identified and rated. A team of subject matter experts is needed to identify all risks, causes and effects. Before starting the PFMEA activity the scope, a description of the process and its specifications are needed.

4.1.2 Example(s)

The example in Fig. 4.1.2-1 only shows the results of the functional analysis, failure analysis, and risk analysis. The preparation and the improvement actions are not given.

	Structure Analysis (STEP2)			Function Analysis (STEP3)		
No./ID.	1. Next Higher Level	2. Focus Element	3. Next Lower Level or Characteristic Type	1. Next Higher Level Function and Requirement	2. Function of Focus Element and Product Characteristic	3. Next Lower Level Function and Requirement or Characteristic
BEOL						
x	M1-Cu Polish	Chemical mechanical polishing of Copper/ Barrier/ ILD to ensure isolation of not connected structures and get metal resistance on target	Thickness variations or polish abort	Yield Loss	Product Yield	Resistance variation



	Failure Analysis (STEP4)				Risk Analysis (STEP5)						
3. Next Lower Level Function and Requirement or Characteristic	1. Failure Effects (FE) to the Next Higher Level Element and/or Vehicle EndUser	Severity (S) of FE	2. Failure Mode (FM) of the Focus Element	3. Failure Cause (FC) of the Next Lower Element or Characteristic	Current Prevention Control (PC) of FC	Occurrence (O) of FC	Current Detection Controls (DC) of FC or FM	Detection (D) of FC/FM	FMEA AP	Special Characteristic / Classification	Filter code (Optional)
Resistance variation	electrical parameter variation; Cu residuals --> Yield Loss	7	Thickness variations or polish abort	Changed copper plating profile	Endpoint monitoring, FDC (Tool trace data monitoring)	1	endpoint monitoring: M1-CU polish	6	L		

Optimization (STEP6)											
FMEA Preventive Action	FMEA Detection Action	Responsible Person's Name	Target Completion Date	Status of Action	Action Taken with Evidence	Completion Date	[S] Severity	[O] Occurrence	[D] Detection	DFMEA AP	Remarks
no action required											

Figure 4.1.2-1: part of PFMEA for Chemical-Mechanical Polishing (CMP); planning & preparation (STEP 1) and results Documentation (STEP 7)

4.1.3 Benefits

- Users are protected against failing parts due to process design flaws.
- Root causes of potential failures are identified and can be solved.
- Effects of potential failures can be detected more effectively and acted upon.
- Priority setting of risks to work on first.

4.1.4 References

[4.1.4.1] https://www.aiag.org/ search for “AIAG & VDA FMEA Handbook”

4.2 Statistical Analysis of Variance

4.2.1 Background

Data of a continuous variable normally shows variation. In many cases the observed variation can be attributed to multiple contributors (factors). Statistical Analysis of Variance can be used to quantify the respective contribution. The data should be structured according to the factors. ANOVA can be applied to production data and data from experiments

4.2.2 Example(s)

In a wafer fab three tools are available to deposit a metal layer. Wafers are processed in batches of 25 wafers. The layer thickness is measured on 5 positions on every wafer. The total observed variation in

layer thickness can be split into tool-to-tool variation, batch-to-batch variation within tool, wafer-to-wafer variation within batch and position-to-position variation within wafer. The tool-to-tool variation and the position-to-position variation are regarded as fixed. Batch-to-batch variation and wafer-to-wafer variation are normally regarded as random, until proven otherwise. The measurement variation is discarded.

Some sample output from statistical software is given below. Four factors are taken into the model: Tool, Batch, Wafer and Position. Tool and position are regarded as fixed factors and batch and wafer as random factors.

Table 4.2.2-1: Tests of Fixed Effects

Term	DF Num	DF Den	F-Value	P-Value
Tool	2.00	37100.0	214.34	0.000
Position	4.00	37100.0	0.00	1.000

Table 4.2.2-2: Variance Components

Source	Var	% of Total	SE Var	Z-Value	P-Value
Batch	10.366860	33.89%	4.912402	2.110345	0.017
Wafer	0.006804	0.02%	0.040995	0.165961	0.434
Error	20.218892	66.09%	0.469446	43.069711	0.000
Total	30.592555				

Position and Wafer are not statistically significant (p-value > 0.05) and are removed from the model. Output for the updated model.

Table 4.2.2-3: Variance Components

Source	Var Comp.	% of Total	StDev
Tool	0.676	2.05	0.822
Batch	27.879	84.52	5.280
Error	4.430	13.43	2.105
Total	32.985		5.743

In this case the tool-to-tool is significant, but quite small. It accounts for 2.05% of the observed variation. The batch-to-batch variation accounts for 84.52% of the variation. The rest variation is 13.43%. The rest variation is the variation that is not explained by the model. The boxplot underneath visualizes this.

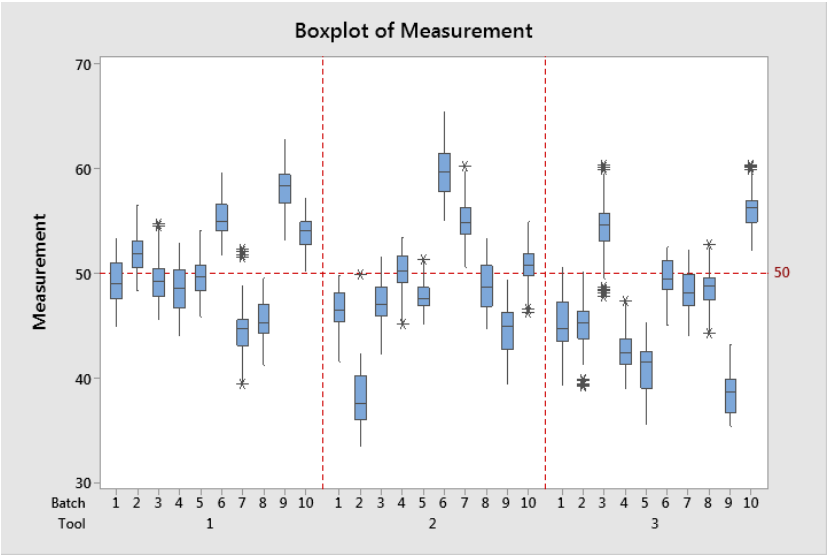


Figure 4.2.2-1: box plot based on example data and analysis describe in this section

4.2.3 Benefits

Analysis of Variance (ANOVA) gives profound insight into the nature of the variation that is observed and its contributors. Knowledge of this can be used for characterization and release, but also for improvement of process capability. MSA uses ANOVA to quantify the repeatability and reproducibility.

4.2.4 References

[4.2.4.1] https://www.aiag.org/ search for “Measurement Systems Analysis”
[4.2.4.2] https://www.nist.gov/

4.3 Control Plan

4.3.1 Background

The Control Plan is a consistent plan to control a manufacturing process. Once FMEAs are defined for the overall process flow and for the sequential process steps and/or the equipment, a Control Plan outlines how the most important characteristics will be monitored, measured and controlled. Included are frequency of performing measurements, the sample and sample size. The Control Plan includes a reaction strategy whenever the measurements indicate an out-of-control situation. The reaction strategy can involve adjusting the process but also can involve the dispositioning of products.

4.3.2 Example(s)

The example is derived from a Semiconductor packaging line or assembly line. The assembly process involves sequential process steps. For each step, the important characteristics, specifications, measurement aspects and sample characteristics are detailed. The measurements and the sample should be selected such that they signal most sensitively any deviation from targeted or common behavior. In case a deviation is signaled, reference to the reaction plan is given. See the table in Figure 4.3.2-1 below.

Part Name/Description		Control Plan ID:	Organization/Plant		Organization Code		Date (Orig.)		Date (Rev.)	
BGA-123		Plan-BGA-123	Assy 1		AT1		1/1/2020		1/1/2023	
Process Step Number	Process Name / Description	Machine, Device, Method	Characteristics		Methods					Reaction Plan
			Product	Process	Specification	Evaluation Technique	Sample Size	Frequency	Control Method	
Incoming QA	Incoming QA Control Plan				Qual Doc 1					
1	Die Prepartion	Naked Eye		Documentation	Spec 1	Visual	100%	All AO	Hold lot for any deviation	a) Hold affected lot engineer disposition b) Assembly General OCAP (OCAP G1)
2/3/4/5/6/7	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx
8	Laser Groove	High Power Scope (100X min)	Laser Kerf Placement		Spec 3	Measurement	3 Rows per Channel per Wafer	1st wafer for every wafer lot	see Shop Floor System	a) Hold affected lot engineer disposition b) Assembly General OCAP (OCAP G1)
		High Power Scope (100X min)	Visual Defects		Spec 3	Visual	a) 10 units/location, 9 locations for 12inch wafer, 5 locations for 8inch wafer	Every wafer lot or after machine setup	a) Lot on Hold and Yield Summary Sheet b) Shop Floor Control system	a) Hold affected lot engineer disposition b) Assembly General OCAP (OCAP G1)
		Tool LG1		Film Remains	Spec 3	Auto machine monitor	1 Point	Every lot	See Shop Floor System	a) Hold affected lot engineer disposition b) Assembly General OCAP (OCAP G1)
		Tool LG1		Laser Groove Power (Efficiency)	Spec 3	Auto machine monitor	Every wafer	Continuous monitoring	Machine auto trigger / stop	a) Machine auto stop & hold for engineer verification. b) BGA Assembly General OCAP (OCAP BG1)
9/10/11/12/13/14	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx
15	Die Bond	Low Power Scope (15X minimum)	Visual Defects		Spec 2 Spec 3 Spec 4	Visual	Min. 3 strips / magazine	Every magazine	a) Lot on Hold and Yield Summary Sheet b) Shop Floor Control system	a) BGA Die Wetting OCAP (OCAP YX1) b) BGA Epoxy On Die OCAP (OCAP YX2) c) BGA Die Placement OCAP (OCAP YX3) d) BGA Die Epoxy Void at Mold X-ray OCAP (OCAP YX4)
		Non-contact tool	Epoxy Bond-Line Thickness & Die Tilt		Spec 2 Spec 3 Spec 4	Measurement	3 units (At 4 corners) (From setup strip)	Every recipe change or start of shift	See Shop Floor System	BGA Bondline Thickness OCAP (OCAP YY1)
		Non-contact tool	Die Placement		Spec 2 Spec 3 Spec 4	Measurement	2 units (From setup strip - applicable for package type 1) 3 units (From setup strip - applicable for package type 2)	Every recipe change or start of shift	See Shop Floor System	BGA Die Placement OCAP (OCAP YX3)
		Low Power Scope (15X minimum)	Expoxy Fillet Height		Spec 2 Spec 3 Spec 4	Visual	1 strip (applicable for package type 1) 2 strips (aplicable for package type 2)	Every device change	See Shop Floor System	BGA Assembly General OCAP (OCAP BG1)
		X-ray	Die-Attach Voids		Spec 4 Spec 5	Visual	1 molded shot / press (Beginning lot)	Every lot	See Shop Floor System	a) BGA Assembly X-ray Inspection OCAP (OCAP ZX1) b) BGA Assembly Molding Process OCAP (OCAP ZX2) c) Hold for Engineer disposition d) BGA Assembly General OCAP (OCAP BG1)
16/17/-/35	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx

Figure 4.3.2-1: example of a process control plan in assembly

4.3.3 Benefits

Some of the benefits are:

- Structured documentation and recording of control monitors, methods of measurement, and test plans.
- Reduction of defects.
- Containment of excursions with standard reaction strategy.
- Continuous improvement.

4.3.4 References

[4.3.4.1] https://www.aiag.org/ search for “Control Plan”

4.4 Statistical Process Control

4.4.1 Background

Statistical Process Control is an approach to control the quality of production processes. Processes show variation which can be divided into variation due to common sources and variation due to special causes. The SPC control chart is used to monitor variation due to both. In the SPC control chart, a process characteristic is plotted. The process characteristic that best reveals a deviating response should be selected. This can be a single measurement or a statistic, like an average or a standard deviation. Control limits in the SPC control chart are calculated using historical data of this characteristic and are set to quite extreme values of the distribution of this characteristic as described in [4.4.4.2], e.g., to the 3σ limits. The probability of the characteristic to fall beyond these limits is small when only variation due to common sources is present. If it does, there is likely variation due to a special cause. The next step is to act according to a pre-defined plan, the Out-of-Control Action Plan (OCAP), with the purpose to eliminate the source of special variation.

4.4.2 Example(s)

General set-up of an SPC loop is shown in Figure 4.4.2-1 below.

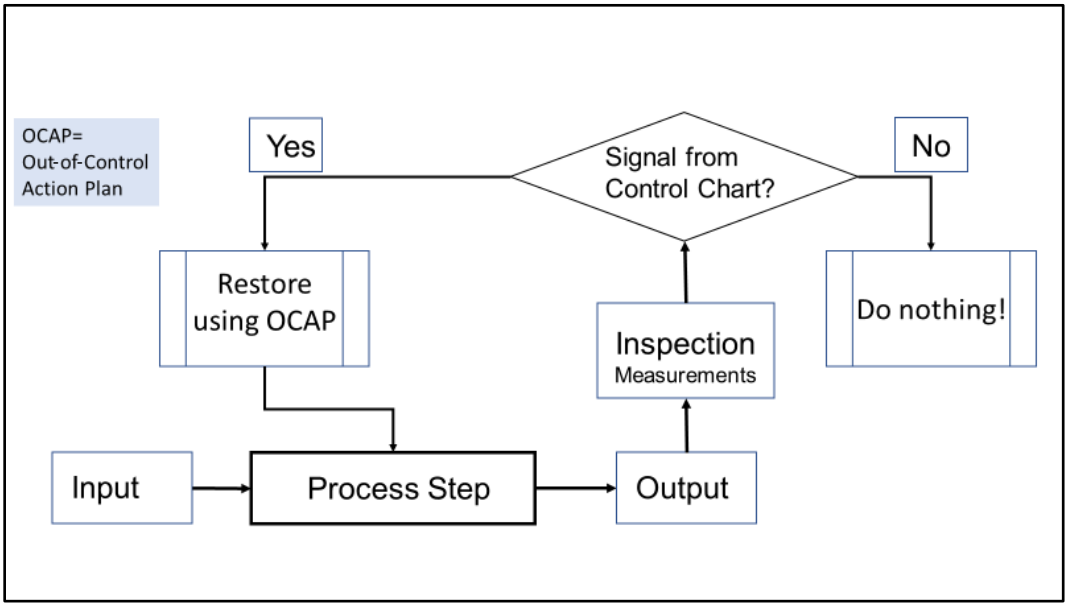


Figure 4.4.2-1: SPC control loop

The process step is the deposition of a metal layer on a batch of wafers. The average and the standard deviation are plotted in a Shewhart chart. When the average moves outside the limits, the OCAP is executed. An example OCAP is as follows:

- If the average is too low, then check RF generator.
- If the RF generator needs adjustment, calibrate this unit and perform a validation run.
- If the average of the validation run is within the limits, then release the equipment.
- If the average is not within the limits, then block the equipment and ask for assistance from engineering.

Only a small part of the OCAP is given.

4.4.3 Benefits

- SPC limits process variation to its natural boundaries. This will reduce the number of defects.
- SPC makes the quality of the sequence of production steps more consistent and more predictable.
- SPC gives clear guidance when to intervene in a production process and when not and how to act effectively and efficiently. This makes the production more person independent and will increase the capacity.

4.4.4 References

[4.4.4.1] https://www.aiag.org/ search for “Statistical Process Control”
[4.4.4.2] http://www.aecouncil.com/; search for “Q002”

4.5 Lot Acceptance Gates

4.5.1 Background

The production process of semiconductor devices consists of many sequential steps. The process control plan defines whether an inspection or a measurement shall be performed to check the quality of the respective process step or of a chain of process steps. These inspections can act as a gate: a decision point to release the material and to continue further processing or to stop, partially stop or rework the material - see Figure 4.5.2-1 below. At those gates criteria for collected data, are applied to to determine conformance of the work in progress or finished product. Cases of non-conformance require a disposition. Rework is only possible at gates after some process steps based on careful evaluation. For various gates the guidelines from the sections Screens (see Section 0), Part Average Testing (see Section 5.1) or Statistical Bin Yield Analysis (see Section 5.2) might be applicable.

4.5.2 Example(s)

Examples of *data collection* for a wafer fab process, are inline defectivity inspection, inline measurement, electrical measurements on test structures and Wafer sort. Examples for the assembly process, are visual inspection after wafer sawing (singulation), inline bond pull test and check of co-planarity of the leads.
Typical *gates for a wafer fab production process* are final wafer electrical (parametric) test at the end of the process on test structures (wafer acceptance criteria) or functional test on dies (wafer sort) and for assembly outgoing visual inspection.
At the end of the wafer fab production process on multiple positions of the wafers various dedicated test structure are placed next to the dies. The dies are intended to be processed further and to be delivered to users. The test structure is sometimes called the Process Control Monitor (PCM). These structures are designed to characterize the basic elements of the electrical circuit on the die, like transistors, capacitors and resistors. Multiple parameters are measured and for most parameters’ specification limits are set. Based on the number of readings outside the specification a wafer or a complete wafer batch can be scrapped.

Final Test of finished devices is considered to be the *final gate* to test the fitness for use of every single device.

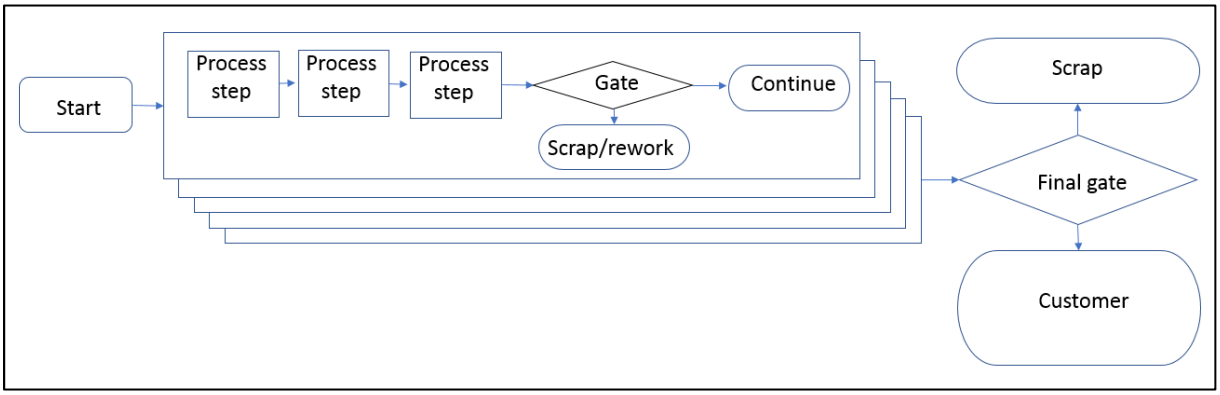


Figure 4.5.2-1: flow chart consisting of various acceptance gates

This criterion is normally set per parameter. A small portion of the specification table could look like the next example in Table 4.5.2-1 below:

Table 4.5.2-1: example of a specification table

Parameter	Wafer level	Batch level
Vth	Scrap wafer if more than 2 readings are below 3V.	Scrap batch if more than 5 wafers don't pass on this parameter.
Ebd	Scrap wafer if any reading is below 12V.	Scrap batch if more than 3 wafers don't pass on this parameter.
Rds_on	Scrap wafer if more than 5 readings are above 60.	Not applicable.

4.5.3 Benefits

- Substandard parts or lots are screened and not delivered to users.
- Signals from every gate are opportunities to correct or improve the process.
- The data from the gates can be used as quality indicators.
- It can be economical to scrap parts as soon as possible to avoid further processing of substandard material.

4.5.4 References

[4.5.4.1] http://www.aecouncil.com/; search for "Q004"and "acceptance gate"

4.6 Audits (Management System, Manufacturing Process and Product)

4.6.1 Background

The degree of excellence of a (quality) management system, a manufacturing or a development process can be determined during a review by an external party. External in that manner means outside of the process or system owning organization but can be from the same company. Also possible is a review by a user or a 3rd party which confirms a certain degree of excellence of the reviewed process or management system. Audits are reviews performed by designated auditors that determine the degree of compliance of a management system, manufacturing, or process, to certain standards. There are 3 types of audits:

a) Internal audit - conducted by auditors within a company.

b) User audit - conducted by auditors from external users.
c) Certification audit - conducted by 3rd party auditors to verify a company's compliance against a specific standard.

An audit is always an interruption of the regular flow of an organization. Therefore, it is important to keep the balance between the chance of improvement after an audit and the disturbance caused by it. Unnecessary high number of audits can lead to a reduced performance.

4.6.2 Example(s)

a) Internal audit: an internal audit is typically part of the quality management system. It is used to regularly check and optimize the processes. It is also often used upfront a following user or certification audit to check if the organization is ready to achieve a certain audit result.

b) User audit: users may perform an audit to release a manufacturing site for delivery of products or after a process change or after an excursion. In the automotive industry the VDA 6.3 standard is a commonly used base for process audits. Another trigger for a user audit could be the release of a new supplier by auditing one of the development or manufacturing sites as representative example.

c) Certification audit: an audit to achieve an IATF 16949 certification for the quality management system of a site is a typical example for a certification audit. An external auditing party (which is itself qualified to do this certification audit) is challenging the QM system with respect to the requirements of the standard. If the results are on a required level, it officially certifies the compliance to the standard (see Figure 4.6.2-1).

Figure 4.6.2-1: IATF 16949 certificate issued after a successful certification audit

4.6.3 Benefits

Generally, a review by an external party which is not involved directly in an organization delivers feedback from a different view angle and can help to uncover weaknesses or confirm efficiency measures in place. Furthermore, standard based audits help to make the degree of excellence of very different processes and management systems comparable. This helps to quickly agree between user and supplier on a level which is good enough to achieve a desired level of quality.

4.6.4 References

[4.6.4.1] IATF 16949 (Weblink: https://www.iatfglobaloversight.org/)
[4.6.4.2] VDA 6.3 (Weblink: https://www.vda.de/en)

5. TEST

5.1 Part Average Testing (PAT)

5.1.1 Background

Part Average Testing (PAT) is an industry standard that uses statistics to calculate static or dynamic test limits to identify individual parts that have characteristics that are outside the typical distribution for the particular test being performed. These PAT limits can be calculated statically as static test limits (known commonly as SPAT), where they are set up once and only changed when there is a change in the process, or they can be calculated on a recurring or dynamic basis (known commonly as DPAT) where they are usually calculated for each lot/wafer.

5.1.2 Example(s)

There will always be some amount of process variation that will affect the performance of a part for a particular test. These variations can cause a part to be outside the test values for the majority of parts but still be within the specification. For example, a common parameter subjected to PAT in IC production the IDDQ current of logic blocks or devices, which typically has a very reproducible characteristic. The figure below is an excerpt from AEC-Q001.

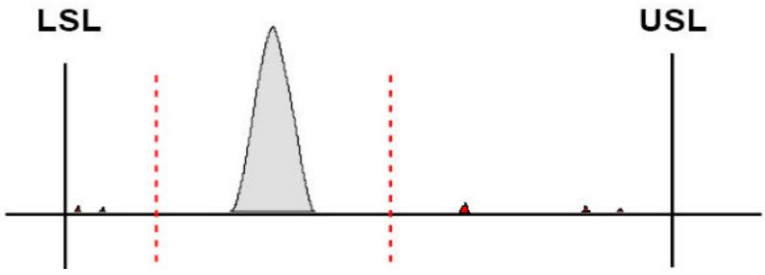


Figure 5.1.2-1: example distribution for PAT

The figure above shows the main distribution is very well placed within the specification limits. By calculating the robust mean and standard deviation, PAT limits indicated by the dashed red lines can be implemented. All parts with a higher (or lower) than expected IDDQ reading are rejected because they pose a higher risk to fail in the field compared to parts from the main distribution.

5.1.3 Benefits

The primary benefit of implementing this tool is to prevent marginal devices from escaping to a user. In addition, by examining these marginal units, we can better understand the process variations that cause

these outliers and can implement actions to reduce/eliminate the outliers and thereby increase the test yield.

5.1.4 References

[5.1.4.1] http://www.aecouncil.com/; search for “AEC-Q001”

5.2 Statistical Bin Yield Analysis

5.2.1 Background

Statistical yield limits (SYL) focus on the yield per lot, sublot or wafer. Statistical bin limits (SBL) focus on outliers in the reject bin pareto. Lots violating the upper or lower yield or bin levels require special actions to be taken (e.g., quarantine or engineering review)

5.2.2 Example(s)

Let’s say we need to calculate SYL on a wafer fab process for a steering diode. We have data from 12 single wafer lots available from production start. The data was confirmed to fit a normal distribution curve. The data set used to determine the statistical bin limits is the following:

Table 5.2.2-1: example of a yield data set

Lot	1	2	3	4	5	6	7	8	9	10	11	12
Yield	97.1	96	96	96.8	99	95.2	97	97.1	97.7	98.1	96.3	98

Step 1: Determination of the mean of the distribution = 97.03
Step 2: Determination of the standard deviation (sigma) = 1.03
Step 3: Calculation of SYL1 and SYL2 values using the following formulas

- SYL1 = Mean – 3 sigma = 97.03 - (3 x 1.03) = 93.83
- SYL2 = Mean - 4 sigma = 97.03 - (4 x 1.03) = 92.76

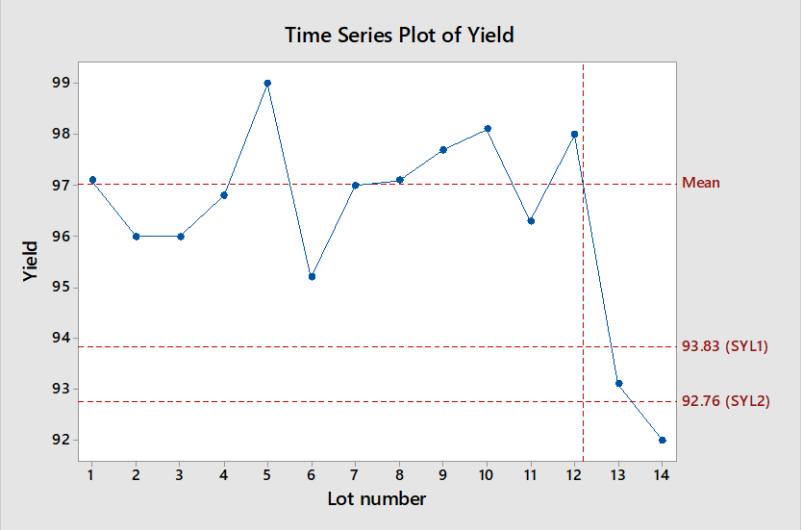


Figure 5.2.2-1: SYL calculation example

These limits are applied to lot 13 and 14:

- Lot #13 has a yield between SYL1 and SYL2. According to AEC-Q002 this requires engineering review.
- Lot #14 violates SYL2 and requires action and may be quarantined.

For SBL1 and SBL2, the logic is the opposite: if the rejects for a specific reject bin class (e.g., reverse leakage current) exceed three or four sigma from the historical mean SBL1 is considered the warning limit and SBL2 is considered the limit requiring action.

5.2.3 Benefits

The primary benefit is the detection and removal of lots (wafer, die or assembled) that exhibit unusually low yield or unusually high bin failure rates. Typically, if these lots were allowed to pass through to the user, it is highly likely that the lots would exhibit some type of quality and/or reliability concern.

5.2.4 References

[5.2.4.1] http://www.aecouncil.com/; search for “AEC-Q002”

5.3 Data Collection, Storage and Retrieval

5.3.1 Background

For automotive products, there is an obligation to store development and production data. IATF 16949 requirement can serve as the baseline, but the user and supplier can also agree on additional or more specific requirements (captured in quality frameworks) if needed.

5.3.2 Example(s)

Examples falling under “data collection” are:

- PDK (process design kit), design libraries and databases.
- Wafer process documentation.
- Product characterization data (pre-production).
- PPAP record.
- Wafer production data (product related, device data).
- Packaged part production data (product related, device data).
- Production data (maintenance/calibration logs, training records).
- Process change notifications.

Data storage / retrieval considerations are:

- Cloud or server storage.
- Backup approach.
- Agreement on storage duration / retrieval time.

5.3.3 Benefits

The benefit of data collection and storage is the proof of compliance and traceability along the supply chain for the product lifecycle. Another key benefit of proper data storage is that these data may be key for failure root cause analysis from field returns which may occur months or even years after production of the material. These root cause findings drive process improvements and cross learning for future defect reduction.

5.3.4 References

[5.3.4.1] https://www.iatfglobaloversight.org/; search for “Records”

5.4 Screens

5.4.1 Background

The main purpose of test screens is to filter out abnormal devices (e.g., distribution outliers) to protect the user from receiving marginal device / product. Usually, the approach is tightening the limits to add a guard band compared to the product specification. Additional stresses and or statistical methods for data evaluation now allow for separation of good and potentially bad products. These screens are widely used to support Zero Defect concepts.

Two categories of test screening exist.

- Active Screening: active means adding stress (not overstressing) to trigger weakness in the device during test. This means revealing defects inside the devices. These devices may pass test without active screening but fail in the field.
- Passive Screening: passive methods do not add additional stress but use data analysis to identify outlier or maverick lot.

It is also possible to combine both methods to trigger defects in active screening and detect them with passive screening methods.

Typical methods are described in the paragraph below.

5.4.2 Examples

Measurement or stress methods (active)

- SHOVE (Short Overvoltage Elevation)
- HVST (High Voltage Stress test)
- VLVT (Very low voltage testing)
- IDDQ (Supply current quiescent)
- ISSQ (Ground current quiescent)
- Burn-In

Methods for data analysis (passive) to identify outliers or maverick lots

- PAT (part average testing) [5.4.4-1]
    - DPAT (Dynamic part average testing)
    - SPAT (Static part average testing)
- SBA (Statistical bin analysis)
- NNR (Near Neighborhood residuals)
- GDBN (Good die bad neighborhood)
- GDBC (Good die in bad cluster)
- ULPY (Unit level predictive yield)
- BMY (below minimum yield)
- SPC (Statistical process control) over bin classification

Testing at temperature extremes (min/max operating)

5.4.3 Benefits

The main benefit of production screens is the detection of outliers that might fail prematurely in the field. However, implementation of additional testing or automated data analysis will incur costs in the supply chain. It is recommended that the choice of methods is aligned between user and supplier.

5.4.4 References

[5.4.4.1] http://www.aecouncil.com/; search for “PAT”

6. APPLICATION AND CAPABILITY

6.1 Industry Standards

6.1.1 Background

The evidence of reliability and quality for a certain product is a major step during release for delivery to a user. The process to provide this data needs to be efficient and accurate at the same time. A commonly accepted procedure and goal with a solid technical background is supporting both targets. And the huge variety of industry standards, especially those on reliability and quality, provides a solution to achieve these targets.

6.1.2 Example(s)

Qualification test plan setup for product qualification can be derived by a case-by-case assessment on knowledge base. This can lead to a tailored and lean qualification plan addressing all needs. The drawback is a need for high technical knowledge to do so. Furthermore, the communication along the supply chain is difficult as the complete assessment needs to be made transparent. A standard based qualification helps to overcome this drawback. The content is well defined, the assessment can be based on a standard process on the user side and the expectations on the pass criteria are clear from the beginning. A qualification test plan based on AEC-Q100 as reliability test standard for automotive ICs is shown in Figure 6.1.2-1 below. In case user requires a reliability capability assessment for an intended application, a mission profile is the starting base for a knowledge-based qualification (refer to section 6.2).

Appendix Template 4A: AEC-Q100 Qualification Test Plan

Q100J QUALIFICATION TEST PLAN						
USER COMPANY:			DATE:			
USER P/N:			TRACKING NUMBER:			
USER SPEC #:			USER COMPONENT ENGINEER:			
SUPPLIER COMPANY:			SUPPLIER MANUFACTURING SITES:			
SUPPLIER P/N:			PPAP SUBMISSION DATE:			
SUPPLIER FAMILY TYPE:			REASON FOR QUALIFICATION:			
STRESS TEST	**ABV**	**TEST#**	**TEST METHOD**	**Test Conditions/S.S. per Lot/# Lots (identify temp, RH, & bias)**	**REQUIREMENTS S.S**	**# LOTS**	**RESULTS Fails/S.S./# lots**
Preconditioning	PC	A1	JEDEC J-STD-020 JESD22-A113	Peak Reflow Temp. = Preconditioning used =	Min. MSL = 3		MSL =
Temperature Humidity Bias or HAST	THB / HAST	A2	JESD22-A101/A110		77	3	
Autoclave or Unbiased HAST or Temperature Humidity	AC / UHST / TH	A3	JESD22-A102/A118/A101		77	3	
Temperature Cycle	TC	A4	JESD22-A104		77	3	
Power Temperature Cycling	PTC	A5	JESD22-A105		45	1	
High Temperature Storage Life	HTSL	A6	JESD22-A103		45	1	
High Temperature Operating Life	HTOL	B1	JESD22-A108		77	3	
Early Life Failure Rate	ELFR	B2	AEC Q100-008		800	3	
NVM Endurance, Data Retention, & Operational Life	EDR	B3	AEC Q100-005		77	3	
Wire Bond Shear	WBS	C1	AEC Q100-001		5	1	
Wire Bond Pull Strength	WBP	C2	MIL-STD-883 - 2011		5	1	
Solderability	SD	C3	J-STD-002		15	1	
Physical Dimensions	PD	C4	JESD22-B100/B108		10	3	
Solder Ball Shear	SBS	C5	AEC Q100-010		10	3	
Lead Integrity	LI	C6	JESD22-B105		5	1	
Bump Shear	BST	C7	JESD22-B117	20 bumps/pillars from 5 devices	5	1	
Electromigration	EM	D1					
Time Dependent Dielectric Breakdown	TDDB	D2					
Hot Carrier Injection	HCI	D3					
Bias Temperature Instability	BTI	D4					
Stress Migration	SM	D5					
Pre- and Post-Stress Electrical Test	TEST	E1	Test to spec				
ESD - Human Body Model	HBM	E2	AEC Q100-002		See Test Method		
ESD - Charged Device Model	CDM	E3	AEC Q100-011		See Test Method		
Latch-Up	LU	E4	AEC Q100-004		3	1	
Electrical Distributions	ED	E5	AEC Q100-009		30	3	
Fault Grading	FG	E6	AEC-Q100-007				
Characterization	CHAR	E7	AEC Q003				
Electromagnetic Compatibility	EMC	E9	SAE J1752/3		1	1	
Short Circuit Characterization	SC	E10	AEC Q100-012		10	3	
Soft Error Rate	SER	E11	JESD89-1, -2, -3		3	1	
Lead Free	LF	E12	Q005				
Process Average Test	PAT	F1	AEC Q001				
Statistical Bin/Yield Analysis	SBA	F2	AEC Q002				
Hermetic Package Tests	MECH	G1-4	Series		15	1	
Package Drop	DROP	G5			5	1	
Lid Torque	LT	G6	MIL-STD-883 - 2024		5	1	
Die Shear Strength	DS	G7	MIL-STD-883 - 2019		5	1	
Internal Water Vapor	IWV	G8	MIL-STD-883 - 1018		5	1	
Supplier:				Approved by: (User Engineer)			

Figure 6.1.2-1: standardized qualification test plan [6.1.4.1]

6.1.3 Benefits

There are three main benefits in using standards in the field of reliability and quality:

- Primary Zero Defects (ZD) related: Reliability and quality standards ensure a defined baseline level in reliability independent from the knowledge of the user.
- Additional but not related: (1) Standards enable efficient user communication during product release, (2) Reliability and quality standards define the most understanding of requirements and practices.

6.1.4 References

[6.1.4.1] http://www.aecouncil.com/; search for “Q100”

6.2 Environmental Stress Testing

6.2.1 Background

To prove the suitability for automotive use and to identify potential reliability issues before releasing a component to automotive mass production, stress tests need to be executed and passed.

6.2.2 Example(s)

Failure mechanism / stress test-based qualification
This is the “classical” approach with fixed environmental conditions and fixed test durations, based on automotive grade. The use of mission profiles is not mandatory. See references [6.2.4.1] and [6.2.4.2] for details.

Mission profile-based qualification
This approach defines environmental conditions and test durations based on the mission profile used for the development of the device to be qualified. Especially for specific applications (e.g., TPMS with high – and untypical for normal semiconductors - vibration or shock load), it may be beneficial to derive tests and conditions from the mission / usage profile as these could not be covered by standard stress-test based qualification.

Another example of specific applications are semiconductors used in electric vehicles (EV). These are e.g., exposed to very high voltages and/or very long lifetime. There is a grey / overlap zone with robustness validation for this approach. See references [6.2.4.3] and [6.2.4.4] for details and description of the application of the method.

For both methods, knowledge of the reliability models and acceleration factors are needed for the tests executed. Possible sources are literature or end-of-life testing. A practical example: Assume a mission profile of 15000 hours of powered operation for an automotive grade zero component, distributed over temperatures like shown in Table 6.2.2-1 below.

Table 6.2.2-1: example of a Mission Profile (MP) based qualification

Ambient Temperature [°C]	Time [hours]	Acceleration factor wrt 150°C and 0.7eV	Accelerated hours wrt 150°C and 0.7eV
-40	1000	0.00	0
25	1500	0.00	0
80	5000	0.02	112
120	7000	0.23	1618
150	500	1.00	500
SUM:	15000	n.a.	2230

An HTOL test as required by AEC-Q100 for an ASIC (t = 1000 hours at T_{amb} = 150°C) would not be sufficient to cover the qualification needs.
To cover such a mission profile, user and supplier should consider running a qualification for a duration longer than required by AEC-Q100, e.g., about 2000 h of HTOL in the example above. If this extension is beyond any reasonable duration, other methods than standardized testing should be considered.
User and supplier should consider running a qualification for a longer period (several 1000 hours) than required by AEC-Q100.

6.2.3 Benefits

Systematic reliability issues can be identified ahead of time – before components are used in the field.

6.2.4 References

[6.2.4.1] http://www.aecouncil.com/; search for “Q100” (IC), “Q101” (Discrete Semiconductors), “Q102” (Optoelectronics), “Q103” (MEMS), “Q104” (MCM), “Q200” (Passive components)
[6.2.4.2] https://www.jedec.org/; search for “JESD22”, “JESD94”, “JEP150”
[6.4.4.3] https://www.zvei.org/; search for “Mission Profile”, “Robustness”
[6.4.4.4] https://www.sae.org/; search for “J1879”, “J1211”

6.3 Stress-Strength Analysis

6.3.1 Background

The probability of withstanding a specific stress level can be used to assess the integrity of a functional element, such as an interface or bulk material, against a specific type of stressor. By linking the stress level, the device under stress can withstand to its reliability performance, this method can be used to conclude on the probability of failure without performing a test to fail.

6.3.2 Example(s)

Destructive wire bond integrity testing (wire bond pull or wire bond shear testing) is a typical stress-strength analysis method. The stress (pull or shear force) is increased upon a level which leads to failure of the functional element (the wire and its interfaces to pad or to lead frame). The analysis of the resulting data (force at failure and failure mode) gives feedback on the wire bond process quality. This can also be performed after stress testing to analyze the degree of degradation introduced by the environmental stress (see Section 6.2).

By plotting the data as cumulative distribution function (CDF), even a comparatively low sample size can be used to conclude on the strength of the border region of the distribution. A minimum stress level at a defined probability may be set as a pass criterion to ensure process and therefore product robustness. Figure 6.3.2-1 shows wire bond pull data plotted as CDF at 0 hour (black) and after stress (red). The shift of the distribution indicates the degradation caused by the stress. Knowledge of the degradation mechanism and its acceleration factor can be used to define the necessary strength at 0 hour to fulfill a certain reliability requirement.

6.3.3 Benefits

Typically, methods based on stress-to-fail principles deliver a faster feedback than methods based on time-to-fail principles. Therefore stress-strength analysis can be used as an early indicator for reliability performance during process and product development, qualification and production. Furthermore, it gives a direct indication of the robustness margin of the product.

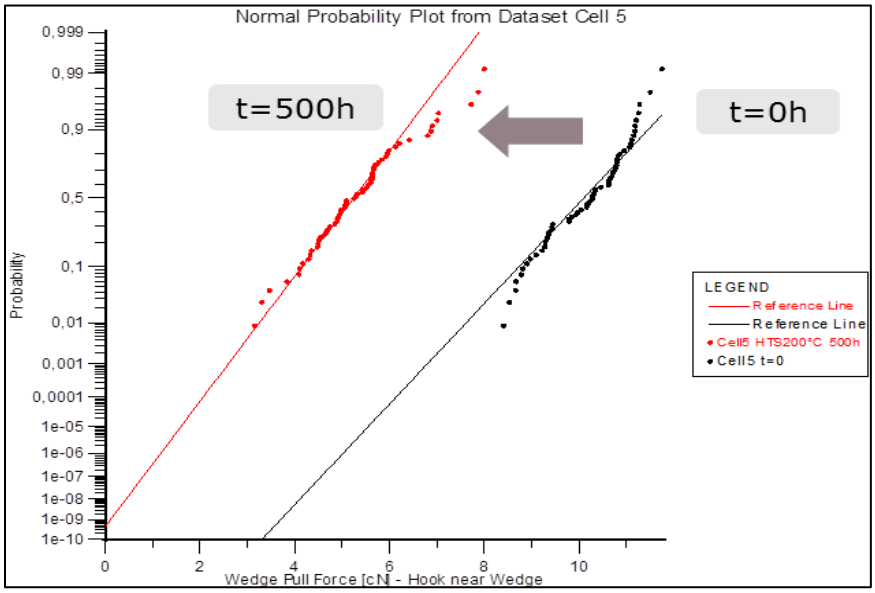


Figure 6.3.2-1: wedge pull data as CDF at 0 h and after 500 h high temperature stress

6.3.4 References

No public reference found.

6.4 Systems Engineering

6.4.1 Background

Automotive systems are growing in complexity (driving assistance systems, autonomous driving, and vehicle electrification). The difficulty to capture interaction paths between new components and the system they are intended to work in is increasing. Classical work- or development flows like the waterfall flow cannot capture all the requirements of a complex system, and the tests needed to verify that all requirements have been met. Defined early at the concept stage and evolving throughout the development, component specifications and verification plans must ensure that user requirements will be met.

6.4.2 Example(s)

Products with Functional Safety Requirements have standards defined that incorporate systems engineering, and mandate that records be kept of the completed validation for every defined system and component requirement (Reference: ISO 26262 [6.4.4.6]). A typical diagram of the Systems Engineering V-Model is shown in Figure 6.4.2-1.

The System Engineering V-Model is a fundamental principle of Systems Engineering, in the form of a conceptual diagram which shows:

- The various sets of information which are necessary for system development.
- The relative relationships between the sets of information.

It is intended to aid with the understanding of requirements, specifications and the various tests which are necessary to develop complex system products; and provide the validation proof that the requirements have been met. Other examples (not discussed in detail) are the boundary diagram or the onion diagram.

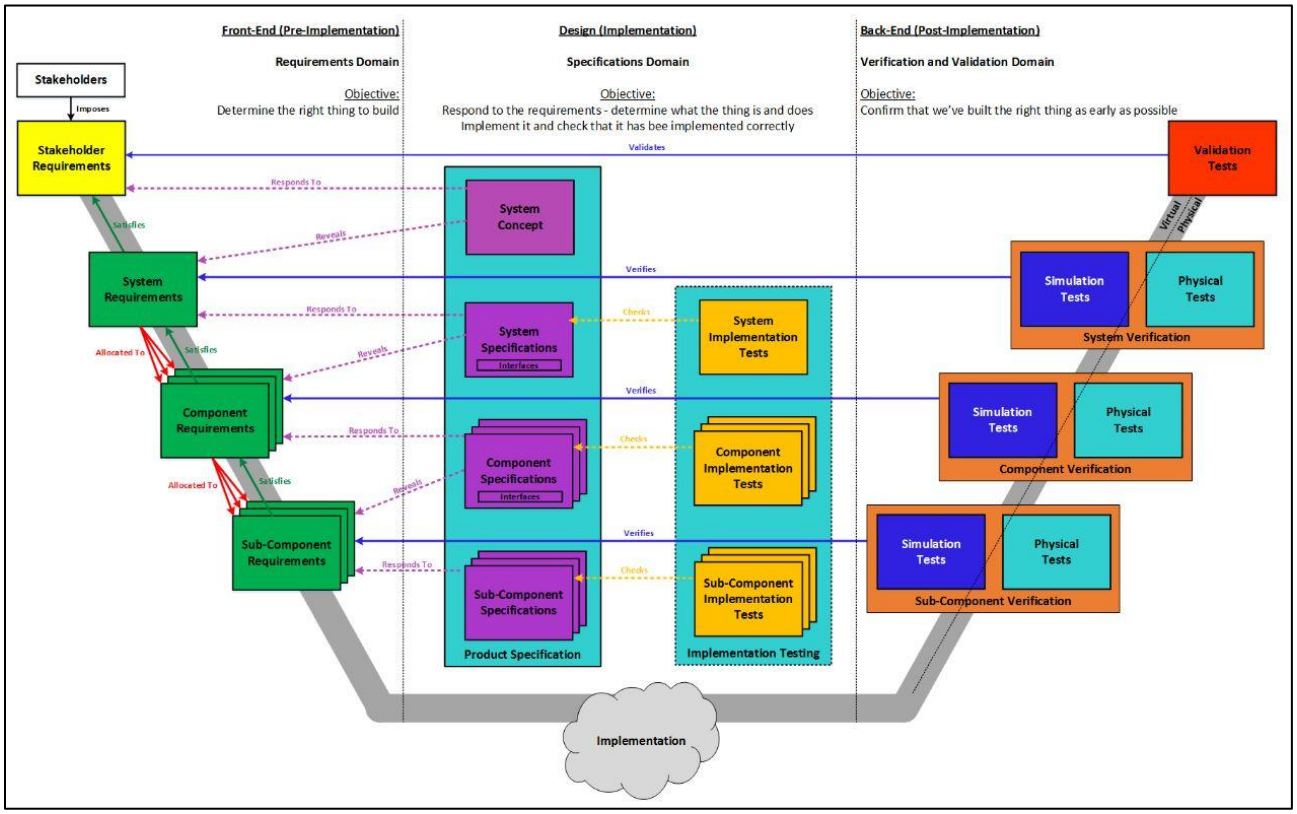


Figure 6.4.2-1: V-model example for systems engineering

6.4.3 Benefits

In a joint development between user and supplier, the application of systems engineering methods enhances mutual understanding of the system and its interaction with the component that is being developed/integrated. To this end, close interaction and cooperation between the key stakeholders (user and supplier) is mandatory for the requirements and necessary features of the system to be clearly defined. The benefits include effective use of critical resources, ways to manage complexity and change, and a structured approach to achieve desired results. Outcomes of systems engineering are clear manufacturing plans, enhanced test coverage, and complete characterization, verification, and validation.

6.4.4 References

[6.4.4.1] Generic search: There are multiple sources for the search term “MBSE” or “Model-Based Systems Engineering”, a synonymously used term is “model-driven systems engineering”

[6.4.4.2] https://www.omgsysml.org/
search term: “Survey of Model-Based Systems Engineering Methodologies (MBSE) Rev B”

[6.4.4.3] http://www.automotivespice.com/
search term: “Automotive SPICE® Process Assessment Model (PAM)”

[6.4.4.4] INCOSE Systems Engineering Handbook,

[6.4.4.5] MITRE Systems Engineering Guide (SEG)

[6.4.4.6] ISO26262 Road vehicles – Functional safety

6.5 Product Derating

6.5.1 Background

Many times, the environment in which a device is applied does not exactly match the use conditions specified by the component manufacturer. When this happens, the user must consult the manufacturer to determine what operating conditions the component in question can be used in and still function as intended. This practice is referred to as "derating" a component and usually refers to modifying the operating parameters of the device to suit the usage conditions that will be seen in the application.

There are a couple of different use cases where this process is employed. They are:

- derating for reliability (long term life)
- derating for functionality (local event causing maximum to be exceeded for short time)

In both cases, the operating environment must be understood. In effect, the junction temperature of the component is being managed. It is not in the scope of this document to provide detailed instructions on how to derate a component.

6.5.2 Example(s)

In the graph below, one can see the relationship of temperature to power dissipation derating and the effect it has on the junction temperature. The goal is to ensure that the junction temperature is not exceeded. So, as an example, one can see where Pd begins to roll off at approximately 85°C. To maintain and not exceed the Tj maximum shown in the graph, from that point on, power dissipation in the application must be controlled to not have the Tj exceed its rated maximum. If the user knows that the component will be operating regularly in this range, then thermal management becomes critical.

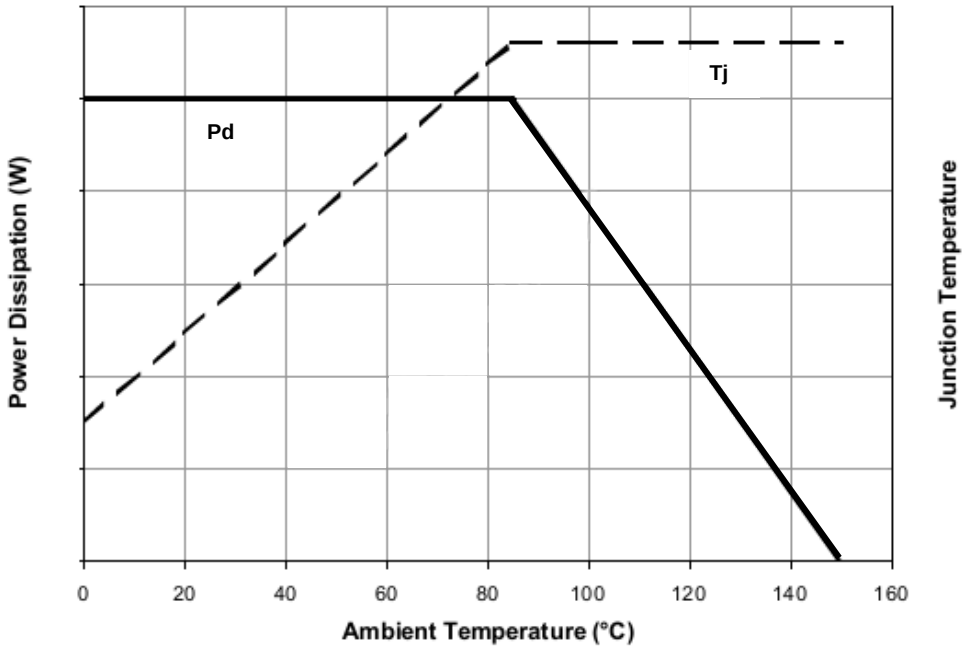


Figure 6.5.2-1: junction temperature versus power dissipation

6.5.3 Benefits

By following recommended guidelines for component operating parameter derating during the design phase, the user can ensure that the component will have adequate stress margins in the application operation, resulting in longer component life and higher system reliability.

6.5.4 Reference

[6.5.4.1] https://www.jedec.org/; search for “JEP149”

7. CONTINUOUS IMPROVEMENT METHODS

7.1 Wafer Level Process Monitoring

7.1.1 Background

A wafer process reliability qualification is performed at the end of the implementation of a new process node. Usually, test structures are stressed on a test chip and data assessed for multiple wafers per lot and on a number of lots with respect to reliability risks. Those reliability risks are defined in an FMEA at the beginning of a technology development project. With a “PASS” from the process reliability qualification a mass production of products can start.

During production Key Electrical device and process Parameters (KEP) are measured on product wafers (generally not related to reliability). Those parameters are used to scrap product wafers because of an expected bad circuit performance. However, reliability stress investigations are performed as “Quarterly Monitoring” on test chips (non-product wafers). Quarterly Monitoring is time consuming (like a process qualification) and in case of the detection of severe reliability deviations during Quarterly Monitoring it is impossible to hold back product wafers, which might have been affected. A lot of affected wafers can already be in the field. This means, reaction time is much too long for Quarterly Monitoring. Some companies include some reliability risks in the KEP with appropriate short stresses. Then the reaction time for the detection of reliability deviations is appropriate since the affected wafers are still in the fab area.
Consequently, it is proposed to perform reliability stresses on a regular daily or weekly basis depending on the number of wafer starts per week. This methodology is called “fast Wafer Level Reliability Monitoring” (fWLR), refer to [7.1.4.1, 7.1.4.2]. It is able to detect reliability relevant process changes/ fluctuations after a successful process reliability qualification. Ideally, fWLR Monitoring can be implemented during technology development in parallel to the process reliability qualification as illustrated in Figure 7.1.1-1. Test structures have special requirements when placed in the scribe line because of the area restrictions. Also, the highly accelerated stresses demand a layout which can tolerate high currents/high voltages and require low series resistances. Stress methods are preferred which take seconds in order to keep measurement time in a cost-effective time frame. High temperature stresses might not be performed with a hot chuck but with local heating of the device under stress. An optimum set up would include an automated data analysis and the display of experimental results in control charts with key reliability limits. Automation requires error-free raw data which can be guaranteed by sophisticated filter methods. It is proposed for the fWLR development phase that a correlation is done between fWLR data and data from process qualification [7.1.4.1].

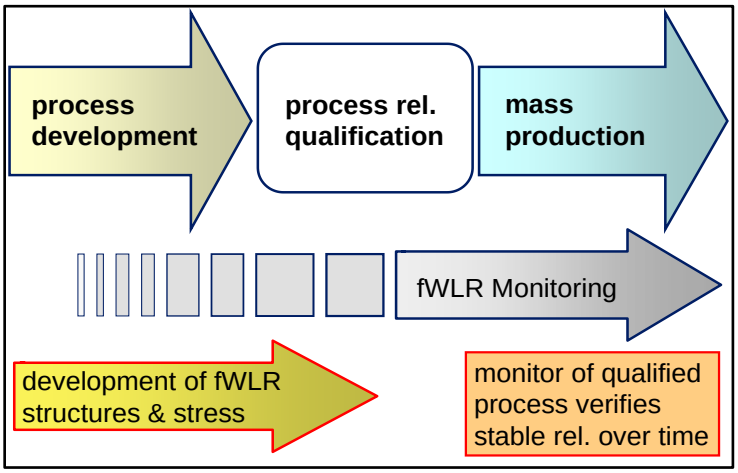


Figure 7.1.1-1: implementation of fWLR monitoring

Generally, all fWLR stresses should detect any relevant deviation in reliability parameters before or after stress. But not all fWLR stresses are quantitative and can be used for a prediction of lifetimes. However, in case of a detected deviation, it is possible to perform additional (longer/ advanced) stresses on the fWLR test structures for the extrapolation of the degradation to use conditions. It is possible that violations of any specification for reliability parameters can trigger an Out-of-Control Action Plan (OCAP), illustrated in the right box of Figure 7.1.2-1. Depending on the severity of the violation various measures can be executed such as, lot on hold, blocking tool equipment, releasing/shipping the lot, or scrapping maverick wafers.

7.1.2 Example(s)

Standard fWLR Monitoring can be executed in a flow as shown in the left box of the Figure 7.1.2-1. The resulting data can be automatically included in a control card which can illustrate the stability of the reliability over time.

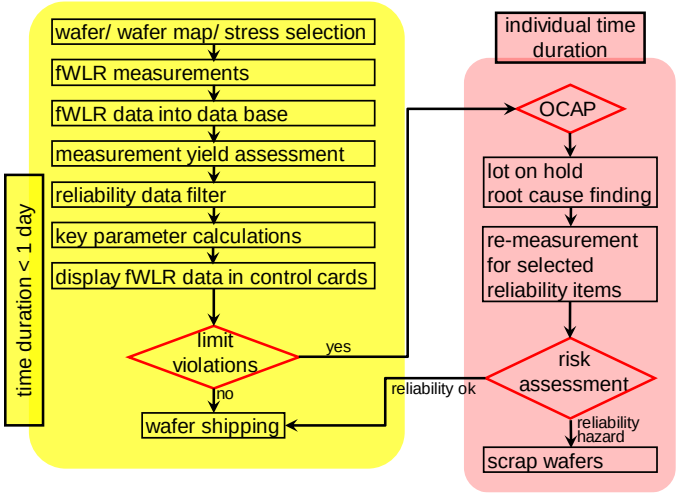


Figure 7.1.2-1: example of Implementation of fWLR monitoring

In terms of a selection of reliability stresses, an fWLR toolbox is proposed to pick any process risk dependent, appropriate stress and measurement sequence, as illustrated in Figure 7.1.2-2. The fWLR stresses are not limited to these in Figure 7.1.2-2.

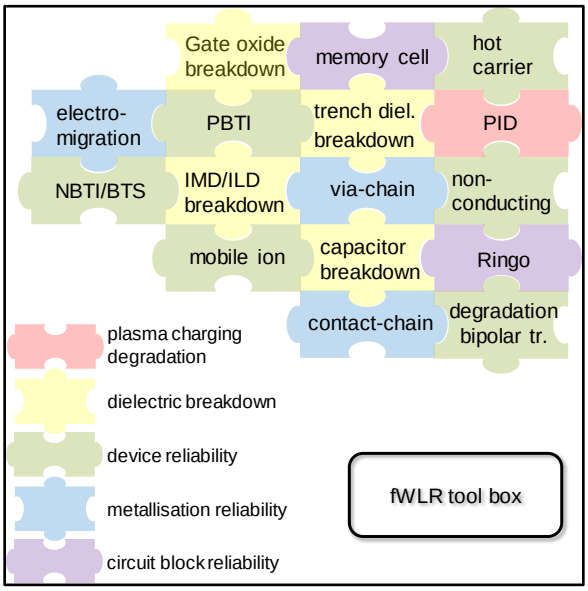


Figure 7.1.2-2: toolbox of fWLR monitoring

This paragraph describes briefly the fWLR stress time and the sampling from good practice and experience (not binding for implementation). Stress times per wafer can reach 2h depending on the number and type of covered reliability risks. With a large sample size (e.g., 10 wafers per lot) fWLR Monitoring would take approximately 24h from picking the lot until the control cards signal a green light for shipping. With respect to an fWLR sampling, for some failure mechanisms (e.g., dielectric breakdown), Plasma Induced Damage (PID) large sample sizes per wafer (e.g., 30 DUTs per 12-inch wafer) are preferred. On the other hand, electromigration, hot carrier or Bias Temperature Stress (BTS) can be stressed on less structures per wafer (e.g., 7 DUT per 12-inch wafer). Sampling of wafers per lot and DUTs per wafer depends also on process maturity and detected reliability weaknesses.

A practical example of a control card is shown in the Figure 7.1.2-3, refer to [7.1.4.3]. The threshold voltage drift of a PID test structure is plotted wafer fine. Clearly, the deviating data sets can be identified fast and a correlation between fWLR data and the processing tools allows for identification of the malfunctioning equipment. Note that the color coding in Figure 7.1.2-3 represents different processing chambers. It can be clearly seen that nearly all the highflyers in threshold voltage drift belong to one chamber.

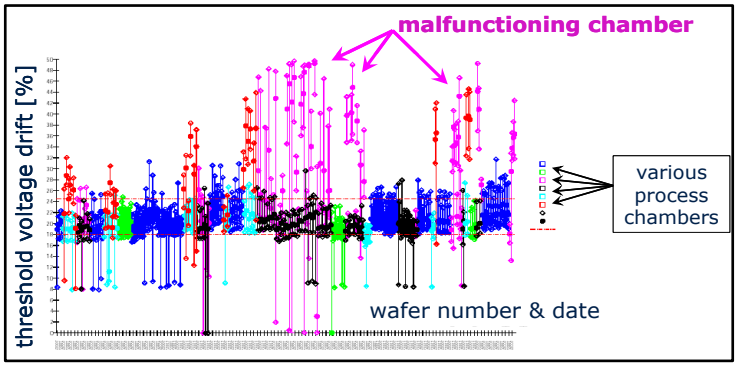


Figure 7.1.2-3: fWLR-example: control card of the drift of threshold voltage after PID stress, refer to [7.1.4.3]

7.1.3 Benefits

fWLR Monitoring offers the unique advantage over Quarterly Monitoring on a test chip and/ or long term packaged product stress, by the fact that the reaction time in case of a violation of reliability specifications is short enough to keep the affected wafers/lots on hold and introduce additional measures / stress measurements on the fWLR test structures which can be used to estimate device reliability lifetimes. From the decision of the OCAP the affected wafers can be shipped or scrapped. This methodology clearly increases product reliability and quality. The example of Figure 7.1.2-3 demonstrates the detection of an event in a process tool which leads to blocking the relevant process chamber. Fully automated fWLR Monitoring gives the advantage of detecting the reliability outliers in time before the wafer material leaves the wafer process fabrication area. fWLR Monitoring with its unique dedicated test structures and reliability stresses can, in a lot of cases, directly verify design rules, which are reliability related. Methods of fWLR can be the measurements which will highlight a processing problem that may affect reliability capability of products, before performing a long term packaged reliability stress for e.g., 1000h.

Further on, fWLR Monitoring methodology can be employed for a very fast assessment of process split investigations. Also, fWLR Monitoring can be used as an initial check of wafer material, which is intended for the process qualification. In case fWLR Monitoring detects reliability violations, the time-consuming qualification measurements on wafer level or package level will not be started and saves time and resources.

7.1.4 References

[7.1.4.1] A. Martin, A. Mitchell, M. Traving, S. Wegner, A. Norman-Elvenich, H. Mayr, H. Nielen, “A fast Wafer Level Reliability (fWLR) Monitoring concept as a continuous reliability indicator for wafer mass production”, IEEE IEDM, pp.175-178, 2020.

[7.1.4.2] A. Martin, R.-P. Vollertsen, A. Mitchell, M. Traving, D. Beckmeier, H. Nielen, "Fast wafer level reliability monitoring as a tool to achieve automotive quality for a wafer process", Microelectronics Reliability, vol.64, pp.2-12, 2016.

[7.1.4.3] A. Martin, C. Bukethal, K.-H. Rydén “Fast Wafer Level Reliability Monitoring: quantification of Plasma Induced Damage detected on productive hardware“, IEEE TDMR, vol.9, no.2, pp.135-144, 2009.

7.2 Process and Product Improvements

7.2.1 Background

If a change is needed to improve process, product performance and/or quality in an automotive supply chain, it needs to be reported to the supply chain. In general, there are two options:

- A process change notification requiring user approval. This is commonly referred to as “PCN”
- A process change the user is only informed about. This is commonly referred as “PCI” (Process change information) or “IN” (Information note).

7.2.2 Example(s)

A typical example of a change which requires user approval is a transfer to a new assembly location. Here the post-wafer-fab processing may be slightly different between the sites and can have a strong impact on the module quality and reliability. Even minor changes in the assembly process can influence the transistor characteristics, chip package interaction or drive difference in heat dissipation, etc.
All these aspects have an impact on the product performance or quality / reliability and need proper evaluation throughout the supply chain.
There are specific automotive guidelines, users can apply to assess the reporting requirements and whether user approval is required for the change currently assessed. The two most referenced ones are:

- JEDEC JESD-46 “Customer Notification of Product/Process Changes by Solid-State Suppliers” [7.2.4.1].
- ZVEI guideline “Guideline for Customer Notifications of Product and /or Process Changes (PCN) of Electronic Components specified for Automotive Applications” [7.2.4.2].

Existing and/or additional requirements can be captured in specific quality agreements between user and supplier.

7.2.3 Benefits

The benefits of using change management are:

- Clear change visibility in the supply chain (upstream and downstream).
- Explicit user approval for changes (when using PCN).

7.2.4 References

[7.2.4.1] https://www.jedec.org/; search for “J-STD-046”
[7.2.4.2] https://www.zvei.org/; search for “PCN form”

7.3 Product Reliability Monitoring

7.3.1 Background

Before a product or process is released, a thorough qualification is performed. When the reliability requirements are met, the product or process is released. After that, release changes to the quality of the incoming material or the conditions of equipment, process excursions can happen, or other deviations are possible. Many of these excursions and or deviations will be identified by applying the process control plan (see Section 4.3) and will be acted upon. Some others might be undetected and can influence the reliability of the product and consequently can become a risk for failures in the field. A periodical check on the reliability of the outgoing pieces is performed to investigate whether any changes in reliability performance have occurred and to eliminate or mitigate the effect of these changes. A plan is needed to perform this periodic check. The plan should cover all processes and product families and can be constructed from a technology and maturity perspective. Sample sizes can be smaller than for a qualification, since the monitoring is done to flag any changes. Structural similarity can be used to make the plan efficient. Various reliability tests will be done, and failures need to be investigated – refer also to Section 8.2 Failure Analysis. If the failure is confirmed relevant, a follow-up plan is needed.

7.3.2 Example(s)

Plan for quarterly monitoring of QFN package family.

Table 7.3.2-1: example of a product reliability monitoring test plan

Stress test	Conditions; duration	Sample Size	Criteria
TC	-65°C / 150°C; 500 c	45	No electrical reject at Final test at -40 °C / 25 °C / 125 °C; AM 14 devices: no delamination at bondable areas
THB	85°C / 85% RH at $V = V_{dd,max}$; 500 h	45	No electrical reject at Final test at -40°C / 25 °C / 125 °C;
HTSL	150 °C; 500 h	45	No electrical reject at Final test at -40°C / 25 °C / 125 °C; IMC 2 devices; >5 bonds/device: minimal diameter > 10 µm

7.3.3 Benefits

The benefits of using change management are:

- A historical baseline of the reliability performance is obtained for reference.
- Changes that impact the reliability can be identified and can be act upon immediately.
- During the safe launch period, a smart program can quickly provide important information about the reliability performance of a product and potential weaknesses.

7.3.4 References

[7.3.4.1] https://www.jedec.org/; search for “JESD659”

7.4 Defect Monitoring

7.4.1 Background

Effective defect reduction is built on three pillars: a mindset of continuous improvement, a disciplined, analytical approach and an effectively designed monitoring strategy. The monitoring strategy must successfully serve the simultaneous roles of defect discovery, baseline improvement excursion / outlier recognition, and control. The defect monitoring strategy is specified in the Control Plan where the method and frequency of monitoring critical process steps is detailed. Defect monitoring Control Plans are defined from the results of Process FMEA, as well as experience from prior process nodes and devices, validation results during Safe Launch, actions to reduce yield loss at electrical test, and corrective actions from 8D. Due to their higher reliability requirements and broader operating environments, the Defect Monitoring Control Plan for automotive semiconductors typically contains more defect inspection and measurement steps, greater sensitivity requirements, tighter control limits and more stringent reporting than their consumer equivalent.

The method defined for Defect Monitoring can be divided into two functional elements:

- Process: monitoring manufacturing with periodic inspection and measurement at critical steps to identify and reduce the sources of systematic and random defects, and
- Product: screening all individual wafers and devices at critical layers to recognize and eliminate materials from the supply chain that are judged as high risk for reliability failures.

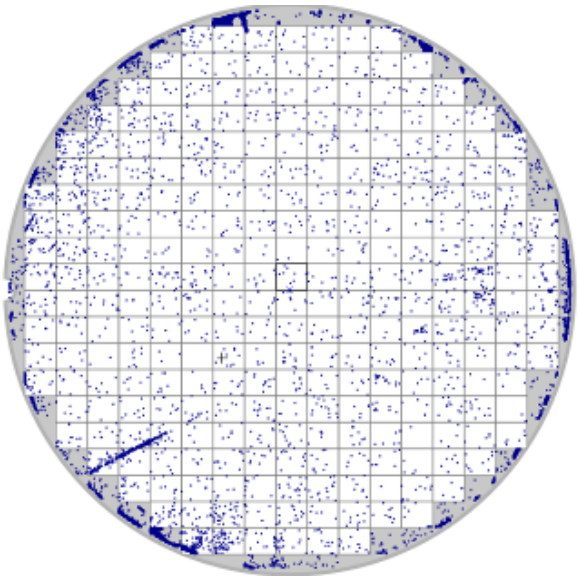


Figure 7.4.1-1: inspection wafer map showing defects from a single process step

7.4.2 Example(s)

While defect reduction is fundamental to improved reliability, defect monitoring strategies in pursuit of Zero Defect vary in their composition and complexity across device types, process nodes and supplier approaches. Assessing the effectiveness of a given approach can be simplified by disaggregating its concurrently operating functions to determine if each individual element is capable for its task.

Table 7.4.2-1: example of a Defect Monitoring Specification Table

Role	Function	Vehicle	Requirements	Output	BKM Verification
Engineering Analysis	Process window discovery, process corner and skew effects, integration, debug, split-lot problem solving and verification	Product or short loop	Highest sensitivity. Tunable to see relevant defect types. Reliable, repeatable results	DOE results	Appropriate sensitivity for device design. Available capacity for DOE. Proactive study of process window, process skews and resultant defects
Line Monitoring	Routine production module-level sampling, followed by review and classification to assess defect population	Product wafers	Routine full wafer scan on 1-2 wafers per lot on a sub-sampled percentage of lots at the end of modules and on critical interim layers.	Pareto chart and SPC chart	Recipe sensitivity (cap rate) to minimum relevant defect size. Die layout (care areas) and defect attributes used to bin defects for classification and impact.
Excursion Monitoring	Routine production layer-level monitoring for known process defect excursion sources	Product wafers	Higher speed inspection monitoring 3-25 wafers per lot at 7-40 wafer per hour throughput on excursion prone layers	SPC chart	Full wafer inspection. Binning by total defects, type, size and location. Illumination, polarization and detection channels tuned to capture known baseline defects
Tool Monitoring and IQC	Per day or per shift monitoring of all process tools and chambers to ensure they are in control and not contributing particles, flakes, or scratches. Validate quality of incoming wafers and raw materials	Bare test wafers	Sensitive, low noise, high-speed scans before and after loading the wafer into a process tool to isolate "adders" from that tool. Can be mechanical load/unload only or simulation of the process step	SPC chart	Recipes at appropriate S:N. Test wafer grade appropriate for needed sensitivity on critical layers. Pre and post recipes tuned to avoid false alarms from decoration. Central component of random defect continuous improvement program.
Metrology	Regular measurement of attributes that affect yield and parametric performance of devices, such as critical dimension, shape, wafer flatness, overlay, film thickness, implant, and composition	Test structures, targets or repeating pattern on product wafers	Accurate, precise and repeatable measurements on a cross-wafer distribution of sites	SPC chart	Precision to tolerance <10%. CpK $\geq$ 1.6. All critical sources of variability (Lot-to-Lot, Wafer-to-Wafer, cross wafer and within die monitored. Sufficient sampling and sites per wafer. No data smoothing. Proactive process feed-forward, and feed back
Screening	Identify maverick wafers and defective outlier die for removal from the supply chain. Enhance confidence in Known Good Die for die stacking, hybrid bonding and multi-die modules.	Product wafers	Very high-speed inspection with 100% wafer coverage on a few reliability critical layers.	Outliers identified	Outlier die or maverick wafers removed or flagged for further disposition at test. Defect attributes and location used to identify and weight outliers to stop escapes and reduce overkill
Packaging / Die sort	Finished die, advanced packaging and heterogeneous integration monitoring	Single or stacked bare die. Packaged die	High speed inspection, metrology and sorting	Pass/fail	6-sided inspection. Lead or bump inspection and metrology. Sidewall crack and delamination detection
Reticle	Reticle IQC and periodic requalification	Reticle	Time or usage-based recertification that a reticle is free from defects that will print in every reticle field	Pass/fail	

The monitoring systems in the Control Plan should have sufficient inherent capability for their assigned role. This can be validated either through available industry benchmarks or with sensitivity studies assessing the capture rate of target defect types versus relevant size for that process node (or equivalent GR&R for metrology). Production operating recipes that determine sensitivity and the corresponding SPC control limits can be set to recognize small excursions quickly without an overabundance of false alarms. Sufficient capacity is needed to perform a statistically significant sampling frequency of critical processing steps, while allowing for planned and unplanned down-time. Finally, control systems should be trustworthy: maintained, calibrated, and routinely validated with standard wafer monitors and trend data to assure their proper performance to specification, repeatability and matched output to other tools that share the same role.

For effective particle defectivity control, SPC charts can be set to limits so that unacceptable deviations from the Mean baseline performance can be recognized and an OCAP initiated. Western electric rules (or equivalent) should be applied to catch sudden spikes or diverging trends within the control limits.

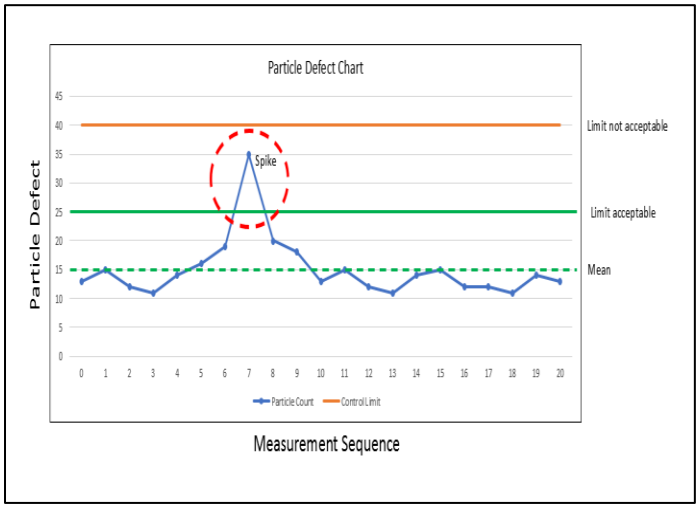


Figure 7.4.2-1: SPC chart

7.4.3 Benefits

An effective defect monitoring strategy identifies and controls the many variables involved in creating a mature, stable, high yielding semiconductor manufacturing process for reliable devices. Once stable, continuous improvement efforts and excursion monitoring assesses incoming raw materials and reduces supply disruptions and costs from scrap from process deviations while also reducing the number of shipped defective parts. A capable screening component is complementary in stopping escapes of outlier die or wafers while minimizing unintended “over-kill” of good die. Data analysis from defect monitoring employs SPC to ensure a process stays within defined limits, triggering an OCAP to quarantine non-conforming materials. It can be used to identify best performing “golden” process tools as well as underperforming tools requiring remediation. It can recognize and monitor failure prone areas of a device design in addition to augmenting pass-fail decisions during electrical test for latent defects, ambiguous results or test coverage gaps.

7.4.4 References

No public reference found.

8. PROBLEM SOLVING

8.1 Problem Solving Tools

8.1.1 Background

In the automotive industry, there are various methods used to assist people to solve various problems. Whether it is a tolerance stack up concern identified during qualification of a device that will not seat properly or the electrical parameters for a motor controller that is not spinning up properly, there are different tools available to help work toward the solution to the problem. This is not an exhaustive list of the tools that are available. Rather, we will discuss some of the more common tools used in the automotive industry.

8.1.2 Example(s)

Listed below, are the tools we will very briefly highlight in this introduction:

- 8D Method
- A-B-A Swap
- Fishbone diagram/Ishikawa diagram/Cause and Effect diagram
- 5 x (times) Why
- Pareto chart
- Fault Tree Analysis (FTA)

8.1.2.1 8D Method

The 8D method is short for 8 Disciplines. This tool walks the user through an organized method of collecting information/data, identifying the underlying cause of the failure, determining an appropriate fix for the failure and finally implementing the fix and sharing lessons learned with other groups who can benefit from the work. During this process, different people or disciplines, will come and go on the team as the project progresses.

8.1.2.2 A-B-A Swap

This method is intended to verify the failure is real and is typically used extensively in electronic applications. The idea is to have a known good assembly and the suspect assembly available for testing. Troubleshooting of the suspect assembly has identified a specific device as responsible for the failure. The suspect device is removed from the non-functioning assembly and installed in the known good assembly. The known good assembly is then powered up and tested. If the component being tested is in fact failing, the known good assembly should now show the same symptom as the suspect assembly. This is the A-B part of the swap. The final step, B-A would be to reinstall the suspect unit in the suspect assembly and confirm the failure is still present. In some cases, the suspect module has the "bad" device removed and replaced with a "good" device.

8.1.2.3 Fishbone Diagram/Ishikawa Diagram/Cause and Effect Diagram

This is a tool to help to determine the relationship of a particular failure symptom and identify the various potential causes for the symptom in a visual format. It is very helpful during the initial stages of problem identification.

8.1.2.4 5 Times (x) Why

This is a simple but powerful tool to understand the cause-and-effect relationship of a particular issue. One would typically begin with asking the question related to why the failure occurred. For example (from semiconductor assembly):

Problem: Lifted wire stitch occurred at the lead side.

1. Why was the wire stitch lifted? - Delamination occurred at package inner lead
2. Why did the delamination occur? - Punch tool hit the package
3. Why did the tool hit the package? - There was no clearance between tool and package body
4. Why was there no clearance between tool and mold? – By construction of the punch tool
5. Why was the tool designed that way? – There was no design rule on the clearance

Corrective action: Update the punch tool design rules and training

At any point in this process, one may arrive at the root cause for the problem being analyzed. When a question cannot be answered, then most likely the cause of the problem has been identified. The reason it is named "5 x Why" is due to anecdotal evidence that suggests most problems can be answered by

asking a question 5 times. However, this does not mean one must stop at 5. One could go to 7, 3 or maybe even 10 to get to the root cause of a particular problem.

8.1.2.5 Pareto Chart

This tool visually groups items based on frequency of occurrence in descending order typically. It is used to help determine what is the highest-ranking item based on the number of occurrences. This tool is most frequently used in manufacturing operations to help identify what project should be worked on next.

8.1.2.6 Fault Tree Analysis (FTA)

An FTA is a visual tool that diagrams a problem by mapping out possible causes. This is a good tool to use to help correlate the symptom seen by the user compared to the potential causes. This tool is popular since it effectively maps out areas to investigate that are related to the problem in a logical sequence.

8.1.3 Benefits

The benefit is to identify root causes and eliminate them in a structured way, thus reducing defective parts, avoiding recurrence, and moving closer to Zero Defects.

8.1.4 References

[8.1.4.1] VDA “8D - Problem Solving in 8 Disciplines” (Weblink: https://www.vda.de/en)

8.2 Failure Analysis Process

8.2.1 Background

The failure analysis process is a method used to identify the cause of an abnormality. This method can be applied in many different ways, from diagnosing a faulty software program to a defective microcontroller in a vehicle to the physical defect in the microcontroller itself. While the tools used are different the goal is the same, determine the cause of the failure. The one thing in common is a systematic approach.

8.2.2 Example

In this example, the focus will be on the microcontroller itself. Typically, one starts with a visual inspection followed by electrical testing to verify the failure described by the user. At this point the results can take different paths. If the failure is not confirmed, then a request is made of the user for additional information better describing the conditions of the failure. If the failure is not confirmed, the device is typically returned to the user for additional verification in the application.

If the failure is confirmed, the detailed circuit analysis begins. Sometimes the failure is obvious with an EIPD signature on an I/O pin. But in many cases, the design engineer is involved to help analyze the circuitry to isolate the specific circuit node affected. Once this is done, the physical deconstruction of the device takes place until the actual physical defect is found. Once the defect is found, typically the supplier would start a root cause investigation report and begin an internal investigation of the potential processes that are the most likely to cause the defect.

An example of a typical failure analysis flow chart is shown in Figure 8.2.2-1 below.

8.2.3 Benefits

This method helps suppliers and users to improve their products by supporting various other methods through providing knowledge of physics of failure and their relationship to design and application.

However, failure analysis is not just used to identify failures returned from users. It is also used quite extensively in the semiconductor manufacturing processes for continuous improvement activities.

8.2.4 References

[8.2.4.1] https://www.jedec.org; search for “JESD671”

Annex A Component problem analysis flowchart

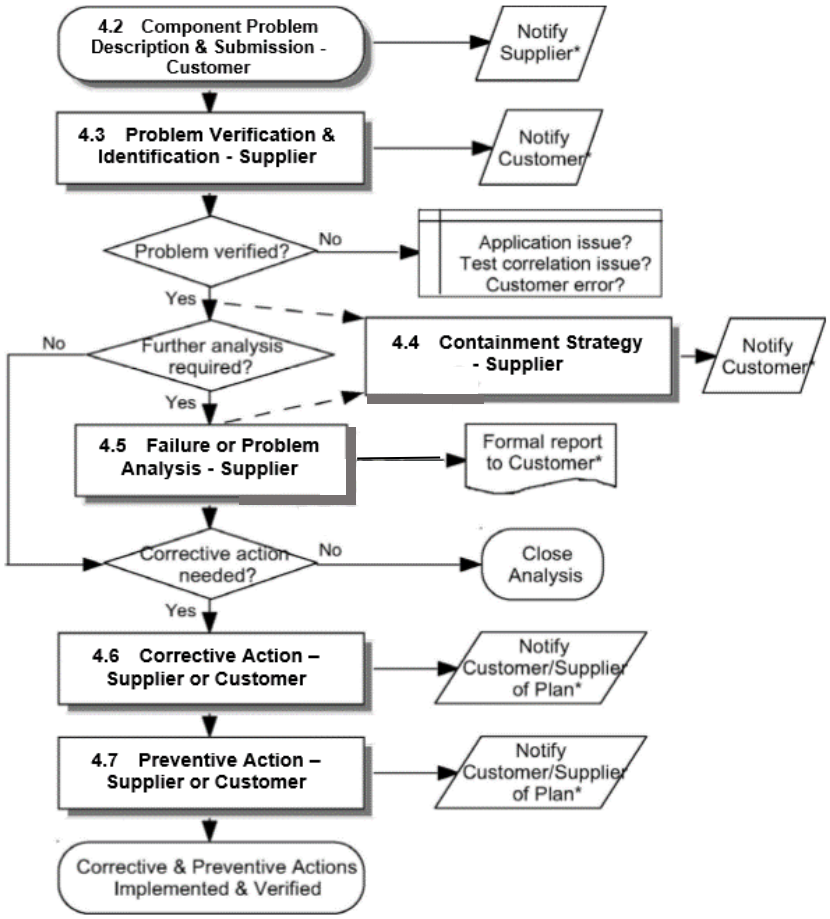


Figure 8.2.2-1: typical Failure Analysis (FA) flow