Changes in Non Volatile Memory Qualification Methods

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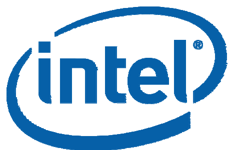
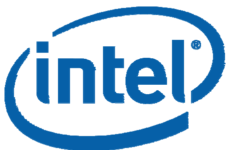


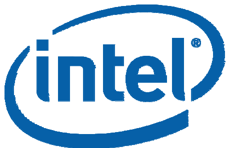
Introduction

- Industry standards for testing program/erase endurance and data retention capabilities of non-volatile memories (NVM) are being revised
  - Retention failure mechanisms and acceleration methods are technically out of date
  - “Solid” data patterns specified in standards neglect important effects
  - Standards and industry practice have gotten out of sync
- Task force formed to revise and update JEDEC standards for NVM memories endurance and data retention
  - Task force had representation from leading NVM manufacturers
  - 2 of the relevant standards (JEP112, JESD-A117) undergone revisions and ratified
  - JESD-47 document revisions is undergoing ballot now.
- AEC document for NVM endurance and data retention (AEC-Q100-005 Rev-B) is similar to old JEDEC standards and deserves careful revisit for current and future NVM memories



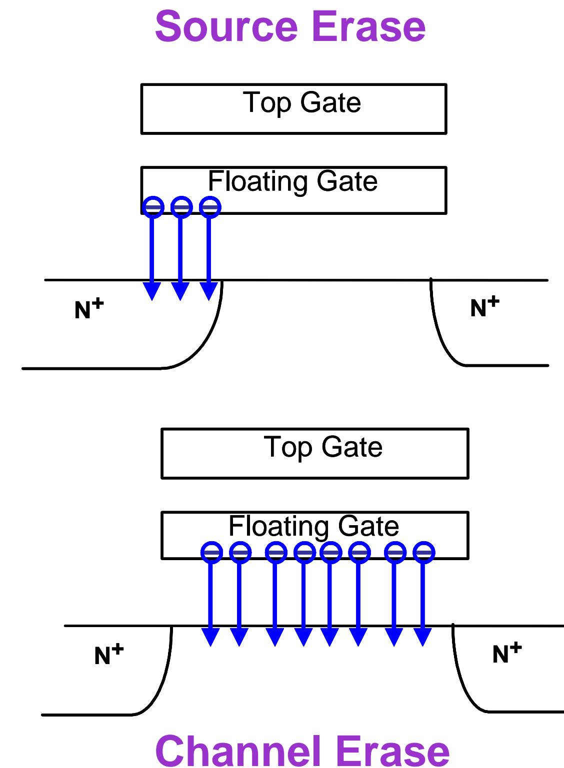
Agenda

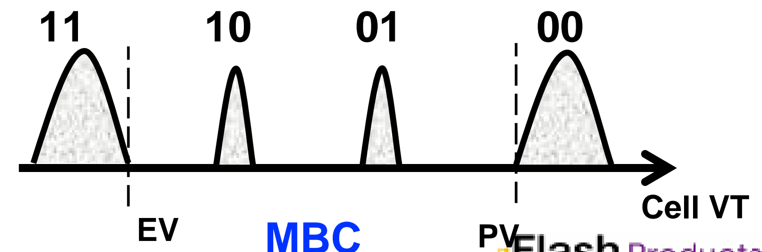
1. Key changes in NVM's in last decade
2. Specific gaps in JEDEC standards
3. Charge loss mechanism in Flash
4. Specific revisions for each standard
5. Overall status of JEDEC standards revision
6. JEDEC Revisions and Relevance to AEC

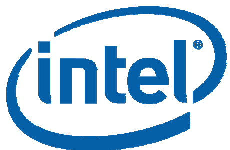


1. Key changes in NVM's in last decade

- **Technology**
  - THEN: 400 nm technology
    - NOR-dominated industry
    - No ECC or other error management
    - Smaller densities (8Mb, 16Mb)
    - Primarily floating gate memories
    - **Single bit per cell (SBC) architecture**
    - **Source side or negative gate erase**
  - NOW: 65 nm technology
    - NAND-dominated industry
    - ECC, bad-block management
    - Monolithic densities as high as 4Gb
    - Advent of dielectric storage
    - **Multi bit cells (MBC)**
    - **Channel erase**



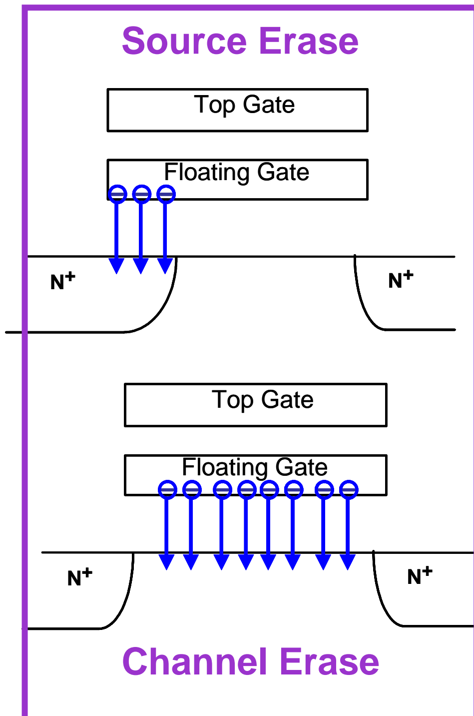


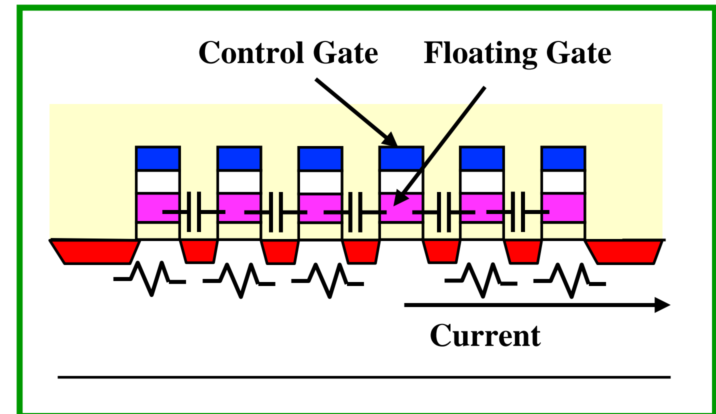


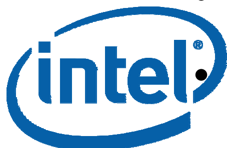
1. Key changes in NVM's in last decade

- **Failure modes and mechanisms: New mechanisms have arisen, old ones have diminished in importance**
  - **THEN:**
    - **Simple products with small number of stand alone bits**
    - **P/E Oxide damage confined to source side**
    - Ignorance of various failure mechanisms
    - Single charge loss mechanism: Ea = 0.6eV
  - **NOW:**
    - **High density, complex products, bit to bit interaction**
    - **P/E oxide damage spread across channel**
      - Responsible for large detrapping failure mechanism in both NOR and NAND
    - Wealth of data on different failure mechanisms
    - Two dominant mechanisms: detrapping (1.1eV), Stress Induced Leakage Current (SILC) (<0eV)

- **Qualification methods**
  - **THEN:**
    - Standards based qualifications
  - **NOW:**
    - Increased use of knowledge-based, application-specific qualification methods.
    - Improved characterization methods have evolved







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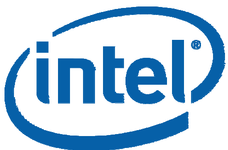
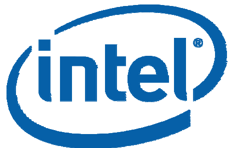


2. Gaps in JEDEC Endurance/Retention Standards

- **Inaccurate acceleration factors**
  - Literature references were from 1980's and early 1990"s
  - Sole charge-loss mechanism had 0.6 eV activation energy
  - No mention of negative temp acceleration for SILC (assumes 0.6eV)
  - No mention of detrapping mechanism (1.1eV)
  - 0.6 eV assumption led to standard 150°C bake, but this has negative acceleration for SILC and represents 300 years at 55°C for detrapping
  - Did not comprehend the now-understood importance of the cycling <u>rate</u> rather than just cycling <u>count</u>
  - Simple data patterns which did not fully test bit-to-bit interactions

- **Does not comprehend Flash architecture realities**
  - Required that every cell be cycled to max-spec cycles
    - Impractical: would take years to do this with high-density NOR
    - Unrealistic: real usage involves fewer cycles/block as # blocks increases with density
  - Written in terms of binary logic for SBC – incompatible with MBC which has quad states
    - "Cycle every cell from 1 to 0 to 1"
    - "Program all bits opposite to intrinsic state"

- **Follows a simplistic "worst case" view of reliability**
  - "Maximum # of program/erase cycles", "worst case temperature, voltage, and frequency", "worst-case pattern"
  - In reality, there is no single worst-case, because NVM's have multiple failure mechanisms that are worst-case under different conditions
  - In addition, industry is adopting knowledge-based qualifications rather than blanket worst-case conditions
    - Retention was for max-spec cycles followed by multi-year (equivalent) bake, but many manufacturers and users are moving to more realistic use conditions, in which the time between cycles is less when you perform more cycles



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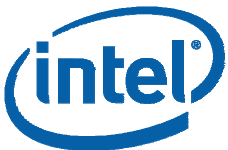
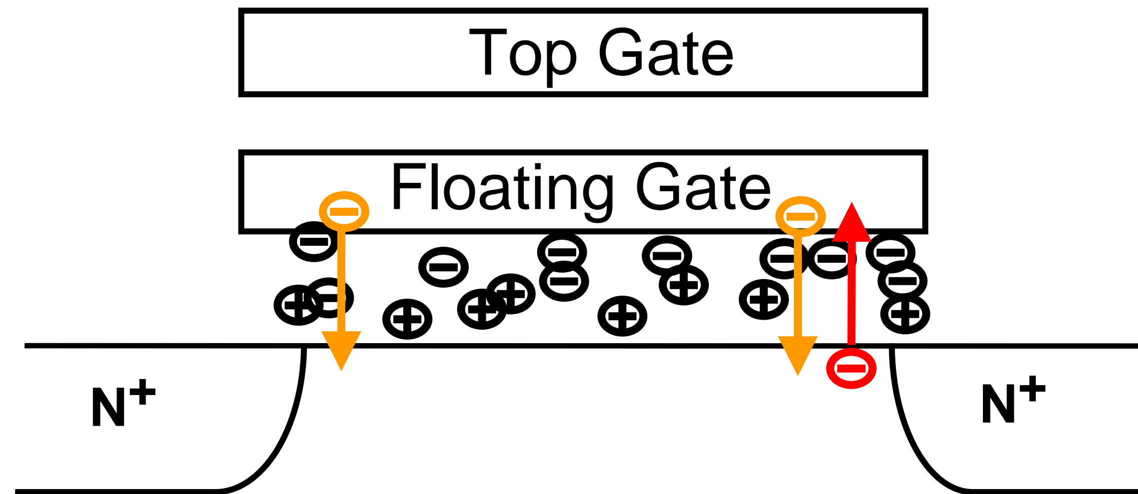
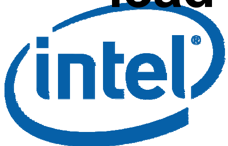


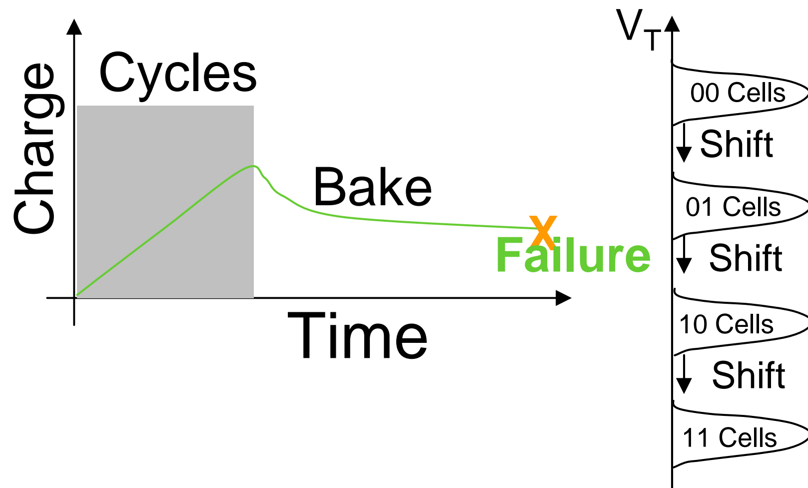
3. Trapping and Detrapping in Flash Memories

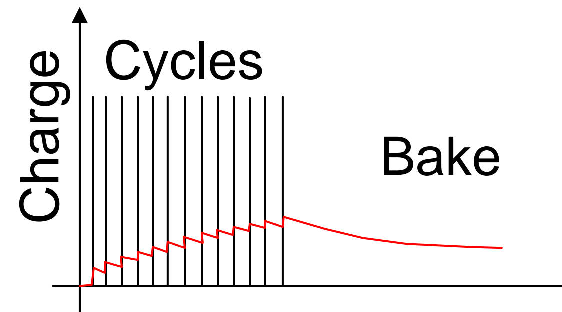


- Flash cell stores data in the form of charge on the floating gate
- Programming is used to inject electrons
- Erase is used to remove electrons
- Program/erase cycling leads to trapped charge in the oxide
- Trapped charge affects threshold voltage
- When the charge detraps over time, the threshold shifts, and this can lead to data loss

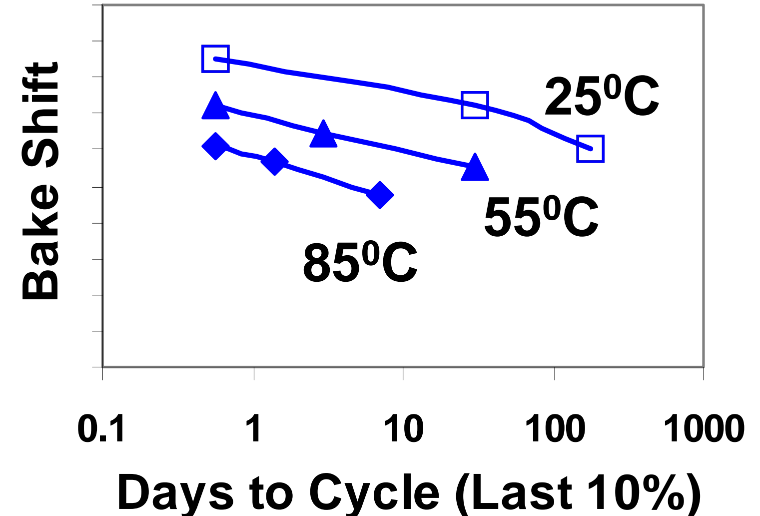


3. Review of High-Temperature Retention

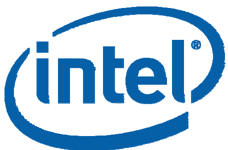




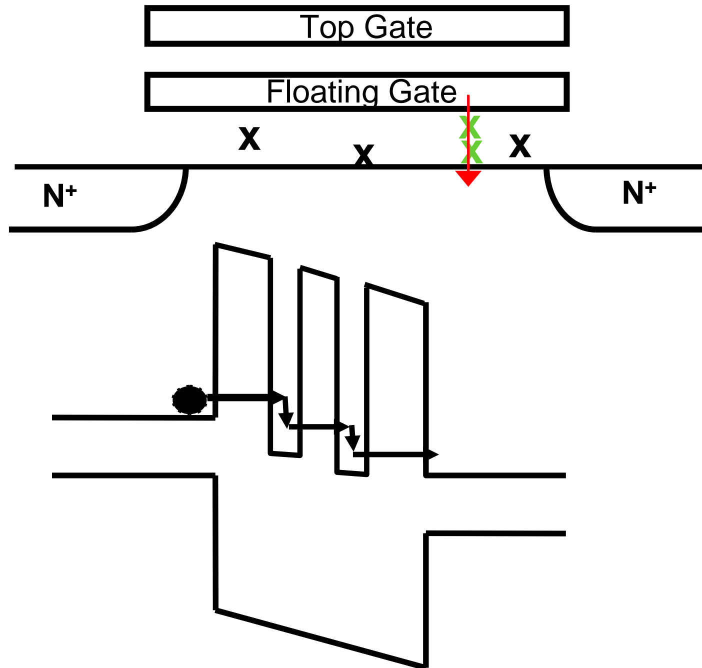
- **Charge builds up in the tunnel oxide during cycling, then detraps over time (left)**
  - The detrap is temperature accelerated (1.1-1.2 eV)
- **The detrap causes margin shifts and eventually retention failure (center)**
- **The distributed-cycling effect is the reduced bake shift which occurs when cycling is slower (Up right)**
  - Detrap during the delays between cycles reduces the detrap that can occur during the bake
- **This description applies to the Flash high-temperature retention mechanism, though there are other retention mechanisms (SILC, defect induced) that are not accelerated much by temperature**

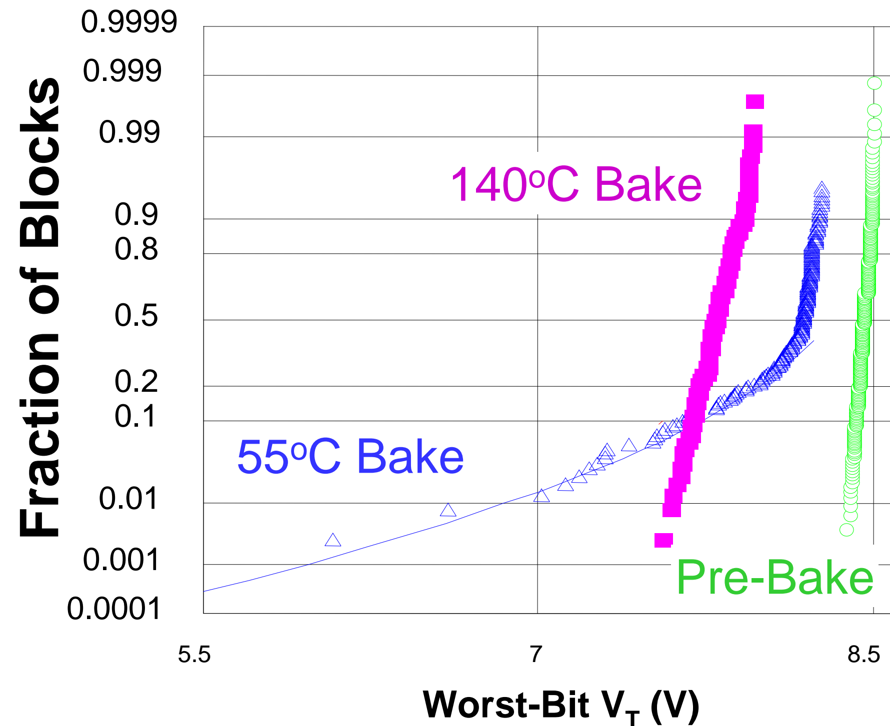


- **Intel performs distributed cycling by cycling at elevated temperature (usually 85°C) so that the time spent cycling matches a certain number of years at use temperature, using 1.1eV**

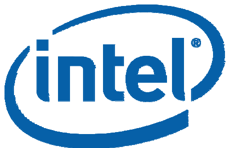


3. SILC -Related Retention





- **Most studied Flash data retention mechanism is SILC-related charge leakage**
- **Left: P/E cycling results in traps in the oxide, which occasionally “line up” in pairs to promote enhanced trap-assisted tunneling**
- **Very difficult to accelerate this mechanism, and any temperature raise can anneal**
  - Tunneling itself has very little temperature dependence
  - Worse (right) raising the temperature can de-accelerate the effect, because the traps anneal out



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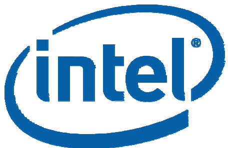
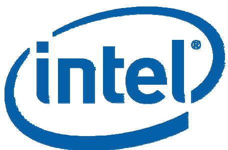


4. Overview of JEDEC Revisions

- **Relevant JEDEC documents being revised:**
  - JEP122: Failure Mechanisms and Models for Semiconductor Devices
    - Summarizes what is known about the reliability physics
  - JESD22-A117: EEPROM Program/Erase Endurance and Data Retention Test
    - Summarizes qualification procedures
  - JESD47: Stress-Test-Driven Qualification of Integrated Circuits
    - Specifies qualification requirements: times, temperatures, sample sizes, etc.

- **High-level view of the changes, and applicability to the AEC**
  - JEP122: Reliability physics brought up to date
    - This is entirely relevant to AEC
  - JESD-A117:
    - Updated procedures in light of architectural changes and new learning
    - Made more flexible so that the procedures can be used as a guide not only for fixed standards but also for knowledge-based qualifications
    - This is entirely relevant to AEC
  - JESD-47: Qualification conditions updated to reflect the dominant failure mechanisms and more realistic use conditions
    - JESD-47 does not attempt to specify qualification requirements for automotive applications, but some of the changes are nevertheless relevant to the AEC

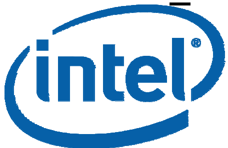


4. Specific Changes to JEDEC Documents

- **JEP122 included correct references and activation energies**
  - Low-to-negative activation energy for SILC
  - 1.1 – 1.2 eV for detrapping, with cycling-rate effects included
  - Reference for detrapping in dielectric-storage memories

- **JESD117 was revised to:**
  - Include Multi-bit Cell technologies (MBC)
  - Data patterns changed to quasi-random (checkerboard-like) to comprehend charge loss, charge gain, cell-to-cell crosstalk, and MBC effects
  - Tightened requirements for controlling unintentional delays between and after cycling
  - Specified acceptable use of intentional delays between cycles
  - Document positioned as procedural guide to executing qualification plan specified elsewhere (JESD47 standard or JESD94-type “knowledge based” qualifications)

- **JESD47A revisions include**
  - Endurance: Specify fraction of high-density arrays that must be cycled
    - Block-level cycling with different cycle counts
  - Retention: Sliding retention scale (10 years for lower cycle counts and 1 year for max-spec cycle count)
    - Bake time/temperature chosen based on 1.1 eV activation energy for detrapping mechanism
    - 25°C temperature lifetest added after cycling to comprehend <0.0eV mechanisms such as SILC
  - Guidance for how to comprehend error correction and wear leveling in media-managed devices
  - Guidance for when knowledge-based qualifications become necessary



4. Changes in JESD47 data retention spec

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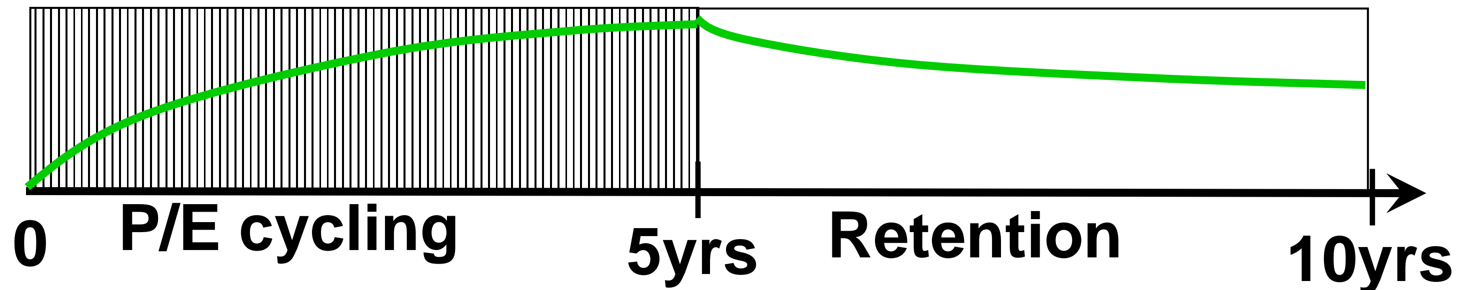
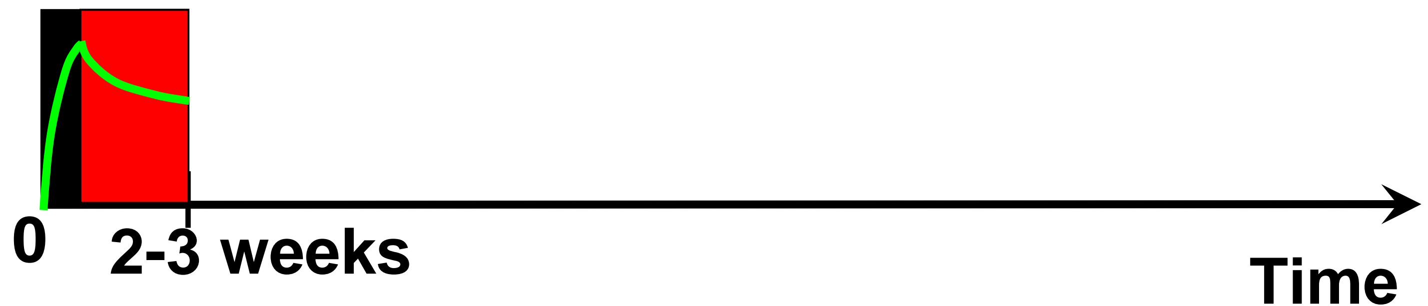
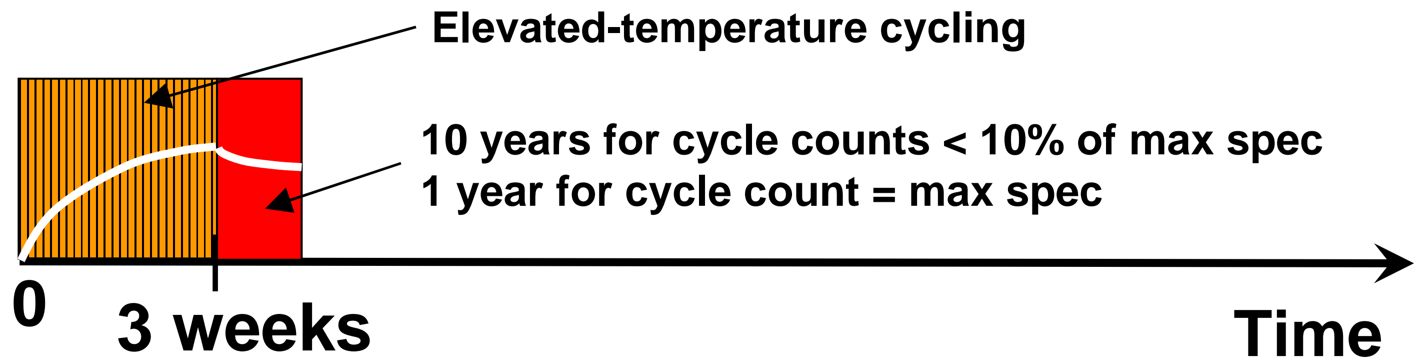
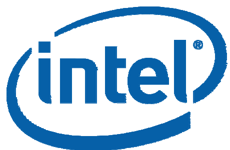


Old Spec:



Revised Spec





4. Revised JESD47 Flow for NVM Endurance and Data Retention testing

Fig. A: NVCE/HTDR/LTDR Flow Diagram

77 Units/Lot

NVCE

P/E cycling algorithm

Cycle Count	# Blocks/Sectors
100% max spec	# Possible in 1 week
10% max spec	# Possible in 1 week
1% max spec	# Possible in 1 week

Total cycling time: 500 hrs max

38 units

Room-temperature cycling per table (insert)
No inserted high-temperature delays

LTDR

Dynamic lifetest
Room temperature
500 hrs

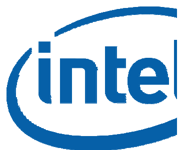
39 units

P/E cycle at 55°C to Tmax per table (insert)
Cycling time plus any inserted delays must be
- ≤ 3 weeks at 85°C
- ≤ 96 hrs at 100°C
- ≤ 10 hrs at 125°C

HTDR

High-temperature bake as shown below.

Cycle Count	Option 1 100°C	Option 2 125°C
100% spec	96 hrs	10 hrs
10% spec	1000 hrs	100 hrs
1% spec	1000 hrs	100 hrs



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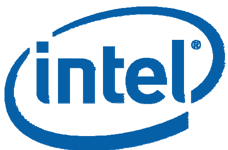
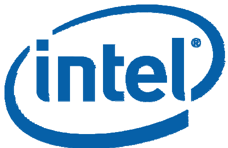


5. Overall Status of JEDEC Revisions

- **Three JEDEC documents relevant to NVM's are being revised:**
  - JEP122: Failure Mechanisms and Models for Semiconductor Devices
  - JESD22-A117: EEPROM Program/Erase Endurance and Data Retention Test
  - JESD47: Stress-Test-Driven Qualification of Integrated Circuits
- **Task group membership that discussed and ratified proposed JEDEC revisions:**
  - AMD/Spansion: Don Darling
  - Freescale: Peter Kuhn and Mohammad Suhail
  - Infineon: Helmut Hoebbel (late addition)
  - Intel: Neal Mielke and Venkat Vasudevan
  - Saifun: Meir Janai
  - Samsung: Jin-Hwan Kim
  - Sandisk (with approval from partner Toshiba): Jian Chen
  - ST Micro: Angelo Visconti
- **JEP122 and JESD22-A117 revisions are complete and released on the JEDEC web site**
  - A follow-on revision to JEP122 is in the works, chaired by Rich Blish of AMD, and that will add additional material relevant to non-volatile memories
- **JESD47 NVM changes are a small part of a complete re-write of that document, which is through two rounds of balloting and currently in its third (ballot issued 04/26/06, voting end 06/06/06)**
  - There have been very few objections to the NVM sections, and those have been resolved



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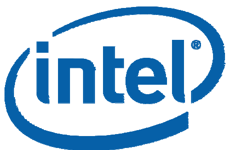

6. JEDEC Revisions and Relevance to AEC

- **NVM demand is growing in automotive industry due to new 'navigation' and 'car-infotainment' applications**
- **Current AEC document is AEC – Q100 – 005 –Rev – B (July 18, 2003) is out-of-sync with NVM industry trends**
  - Like old JEDEC, AEC-Q100 recommends cycling all cells to max specification, using worst-case conditions
  - Bake 1008 hrs 150°C
- **AEC Q100-005 fails to recognize**
  - Cycling all cells is impractical, at least for NOR
  - Baking at 1000hr at 150°C after cycling corresponds to >700 years
  - Worst case is a nonexistent concept since there are multiple failure mechanisms with different activation energies.

AEC should recognize NVM technology trends and develop testing requirements that are consistent with industry directions while meeting application needs.