A Comparison of Electrostatic Discharge Models and Failure Signatures for CMOS Integrated Circuit Devices

M. Kelly Delco Electronics Corporation 1800 E. Lincoln Road, M/S R117 Kokomo, Indiana 46904-9005 (317) 451-7084

T. Diep AT&T Bell Laboratories Engineering Research Center P.O. Box 900 Princeton, New Jersey 08542 (609) 639-2412

S. Twerefour Ford Microelectronics, Inc. 9965 Federal Drive Colorado Springs, Colorado 80921 (719) 528-7709 G. Servais Delco Electronics Corporation 1800 E. Lincoln Road, M/S R117 Kokomo, Indiana 46904-9005 (317) 451-7923

D. Lin AT&T Bell Laboratories Engineering Research Center P.O. Box 900 Princeton, New Jersey 08542 (609) 639-2414

G. Shah Ford Motor Company, ACD, Electronics Operations 17000 Rotunda Drive, Room C160 Dearborn, Michigan 48121 (313) 845-3599

ABSTRACT

Six different CMOS device codes were evaluated, according to available test standards, for Electrostatic Discharge (ESD) sensitivity using three ESD models:

- Human Body Model (HBM)
- Machine Model (MM)
- Field-Induced Charged Device Model (FCDM)

Four commercially available simulators were used: two to perform the HBM ESD evaluations and two to perform the MM ESD evaluations. FCDM stressing was performed using an AT&T designed simulator. All stressing was performed at AT&T Bell Laboratories, Delco Electronics, and Ford Microelectronics. The failure threshold voltage and failure signature associated with each ESD model and simulator were determined for each test sample. Threshold correlation and regression analyses were also performed.

Though the three ESD models and simulators created multiple failure signatures, they do not exhibit a high degree of overlap. Our results will show a high correlation between the ESD thresholds, failing pins, failing circuitry, and failing structures for HBM and MM stressing of the device codes evaluated.

INTRODUCTION

Over the past several years, ESD models have proliferated as Integrated Circuit (IC) users and manufacturers endeavor to predict IC performance in application environments. The test techniques being implemented have grown more complex as a myriad of test-pin combinations have been specified to guarantee device performance during production and field use. These complex requirements have resulted in: difficulty measuring ESD sensitivity; a need for large sample sizes; an uncertainty when correlating different simulators or facilities; and, because ESD stressing is considered a destructive test, a significant increase in cost of qualification.

Several papers have been published in the past few years exploring potential correlation between HBM / MM [1,2] and HBM / CDM [3,4,5]. However, an overall comparison of the three ESD models and the corresponding failure signatures for various CMOS technologies has not been reported to date.

In addition, the ESD sensitivity comparisons of previous investigations [1,2,3,4] were conducted to evaluate the effect of individual pin combinations or utilized a threshold definition of the 50% value for the cumulative probability plot. These procedures are not a representation of procedures followed by qualification engineers. The majority of qualification engineers determine test failures according to the failure criteria definition specified in industry test specifications. We have investigated the correlation between several ESD models from the practical standpoint of an individual tasked with performing an ESD qualification test. However, to assess the robustness of our analysis, we have also performed two additional sets of correlation analysis utilizing a 50% value and a first-fail value. In later sections of this paper, these results will be discussed showing that the correlation "big picture" is robust.

This paper discusses the results of a round-robin ESD experiment performed jointly by AT&T Bell Laboratories, Delco Electronics, and Ford Microelectronics. To minimize the number of ESD models required to provide a reasonably accurate prediction on the ESD susceptibility of an integrated

circuit, the investigation examined the correlation between three ESD models used by the electronics industry: Human Body Model (HBM), Machine Model (MM), and Field-Induced Charged Device Model (FCDM). The designed experiment contained two independent variables:

- Two different test systems performed HBM and MM stressing and one test system performed FCDM stressing.
- A total of six different CMOS devices were evaluated, with each participating company providing two device codes.

The testing approach attempted to quantify the failing ESD voltage level for each ESD model through execution of testing procedures defined in commonly used test standards. Once all ESD stressing was completed, resulting failure signatures and failure locations were identified. Optical and Scanning Electron Microscope (SEM) photographs are included to illustrate typical failure characteristics for each ESD model. The observed physical characteristics of the HBM, MM, and FCDM failures at various voltage levels provide a valuable reference tool for the failure analyst tasked with classifying a transient event resulting in ESD failure.

SELECTION OF TEST SAMPLES

To represent as many component CMOS technologies and packaging configurations as possible, each participating company provided two device codes of various pin counts for complete ESD characterization. Table 1 lists the devices chosen for the evaluation and the corresponding technology, packaging configuration, and functional description. These devices represent components used in the "real world."

Table 1. Devices used in round-robin experiment	Table 1:	Devices used	in round-robin	experiment
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Device	Package Type	Technology	Description
X1	44 PLCC	0.9 μm 3 volt / 5 volt CMOS	Echo cancellor
X2	100 EIAJ	0.9 μm 5 volt CMOS	ASIC for disk drive system
Х3	40 PDIP	1.5 μm 5 volt CMOS	Audio applications
X4	28 PLCC	1.5 μm 5 volt CMOS	Bus interface for communication and data
X5	28 PDIP	1.2 μm 5 volt CMOS	Controls module communications for vehicle
X6	24 PDIP	1.5 μm 5 volt CMOS	2K x 8 bit static RAM

TEST EQUIPMENT AND PROCEDURE

The Human Body Model is designed to simulate a human body discharging accumulated static charge (via a fingertip) through a device to ground (see Fig. 1). It comprises a series RC network of a 100 pF capacitor and a 1500 Ω resistor [6,7].



Figure 1: 500 volt HBM ESD discharge waveform through a short (for waveform details, see [6,7]).

The Machine Model is designed to simulate a machine (test equipment, furniture, etc.) discharging accumulated static charge through a device to ground (see Fig. 2). It comprises a series RC network of a 200 pF capacitor, a resistor of approximately 8.5 Ω , and an inductor of approximately 0.5 μ H [8].



Figure 2: 500 volt MM ESD discharge waveform through a short (for waveform details, see [8]).

The Charged Device Model, on the other hand, simulates a charged device (e.g., sliding down a shipping tube, etc.) discharging directly to ground (see Fig. 3) [9,10,11].



Figure 3: 500 volt FCDM ESD discharge waveform using a 4 pF module (for waveform details, see [11]).

All Human Body Model (HBM) and Machine Model (MM) ESD stressing was performed using two different commercially available ESD simulators and Field-Induced Charged Device Model (FCDM) ESD stressing was performed using an AT&T designed simulator [12,13]. To insure proper simulation and repeatable ESD results, simulator waveform performance was verified following the procedure outlined in the ESD Association HBM and MM ESD specifications [6,8] and the JEDEC FCDM ESD specification [11]. Based upon familiarity with the CDM event and characterization procedure, AT&T Bell Laboratories performed all FCDM stressing. Ford Microelectronics and Delco Electronics, both automotive electronics users and manufacturers, performed all HBM and MM ESD stressing.

Prior to ESD characterizations, complete DC parametric and functional testing per applicable device specification requirements was performed on all test samples. For HBM and MM stressing, all pins on each device were subjected to ESD stressing with three positive and three negative pulses with a one second delay between each pulse. Device stressing was accomplished following the pin combination criteria outlined in the ESD Association HBM and MM ESD specifications [6,8]. For FCDM stressing, each pin was stressed with three positive and three negative pulses with at least 0.1 second delay between pulses, following the procedure outlined in the JEDEC FCDM ESD specification [11].

The stress voltage levels for each ESD model were selected based on prior experience with the devices and are shown in Table 2. For devices X1 and X2, a step-stress procedure was used on a sample of three available devices per device code. For devices X3 through X6, a new sample of three devices was used at each stress voltage level to avoid any cumulative effect due to the ESD stressing itself [14]. A total of 933 devices were stressed for this study. Once the stressing was completed, all devices were returned to the originating company for complete DC parametric and functional testing per applicable device specification requirements. Devices failing the electrical testing criteria were then submitted for failure analysis.

ELECTRICAL RESULTS

To insure an accurate evaluation, all experimental devices were functionally tested at each location before and after being subjected to ESD stress. For devices X1 and X2, a 30% shift in I/V curve trace characteristics was used as the failure criteria. For devices X3 through X6, the failure criteria was a change in device functionality or leakage current exceeding the applicable device specification requirements, as specified in the industry ESD test specifications (ESD Association HBM, ESD Association MM, and JEDEC FCDM). The results of these tests were then used to determine the ESD threshold for each device code.

The results for the ESD stressing of all devices are summarized in Table 3. The summaries detail the failure threshold voltage levels and packaging configurations. All failure threshold voltage levels are listed as the last passing voltage level, P, and first failing voltage level, F, when applicable. If an entry lists only one threshold, either P or F, the testing procedure was unable to fully characterize the particular device. For devices without a passing voltage level, a value of zero volts was used as the default passing voltage level. Initial stressing of device X3 began at 6000 volts. However, further characterization revealed the failure threshold to be less than 6000 volts. Additional stressing was performed at lower stress voltage levels (3000 V, 4000 V, and 5000 V). Due to a limited number of available samples and time constraints, only Delco was able to complete a full characterization at the lower stress voltage levels (as indicated in Table 3).

Table 2:	Device Stres	ss Voltage	Levels

Device	HBM (V)	MM (V)	FCDM (V)
X1	500 to failure, steps of 500	50 to failure, steps of 50	200, 500, 1000
X2	500 to failure, steps of 500	50 to failure, steps of 50	200, 500, 1000, 1500, 2000
X3	3000, 4000, 5000, 6000	200, 300, 400, 500	200, 500, 1000, 1500, 2000
X4	1000, 1500, 2000	100, 150, 200	200, 500, 1000, 1500, 2000
X5	1000, 1500, 2000, 2500, 3000	100, 150, 200, 250, 300	200, 500, 1000, 1500, 2000
X6	2500, 3000, 3500, 4000, 4500, 5000, 5500, 6000	100, 150, 200, 250, 300	200, 500, 1000, 1500, 2000

Test	Package	HBM ESD (V)		MM ESD (V)		FCDM ESD (V)
Sample	Туре	Delco Stressing	Ford Stressing	Delco Stressing	Ford Stressing	AT&T Stressing
X1	44 PLCC	default (0) / F 500	default (0) / F 500	F 50	P 50 / F 100	P 500 / F 1000
X2	100 EIAJ	P 1000 / F 1500	P 1000 / F 1500	P 50 / F 100	P 100 / F 150	P 2000
Х3	40 PDIP	P 3000 / F 4000	F 6000	P 300 / F 400	F 400	P 500 / F 1000
X4	28 PLCC	P 1000 / F 1500	P 1000 / F 1500	P 100 / F 150	F 100	P 500 / F 1000
X5	28 PDIP	P 2000 / F 2500	P 2000 / F 2500	P 200 / F 250	P 200 / F 250	P 500 / F 1000
X6	24 PDIP	P 4000 / F 4500	P 4000 / F 4500	P 300	P 250 / F 300	P 500 / F 1000

Table 3: Results for HBM, MM, and FCDM ESD Stressing

Since the device stress voltage levels shown in Table 2 involved relatively large voltage increments (500 volts for HBM, 50 volts for MM, and 500 volts for FCDM), a failure threshold needed to be established for later correlation analysis. Based upon the stressing results for each ESD model (as shown in Table 3), a "best estimate" of failure threshold for each device was determined. These best estimate threshold values are shown in Table 4.

For HBM and MM stress results (devices stressed at two different locations), this "best estimate" was accomplished for each device by calculating the midpoint between the lower passing stress voltage level (identified with a P) and the lower failing stress voltage level (identified with a F). For example, device X1 lists MM stress results of 50 volts (Fail) for Delco stressing and 50 volts (Pass), 100 volts (Fail) for Ford stressing. The values used to determine the "best estimate" of failure threshold would then be 50 volts (Pass) and 50 volts (Fail), resulting in a best estimate value threshold of 50 volts.

For FCDM stress results, this "best estimate" was accomplished for each device by calculating the midpoint between the passing stress voltage level (identified with a P) and the failing stress voltage level (identified with an F). Device X2, with a passing stress voltage level equal to the FCDM stress limit, was assigned a "best estimate" threshold of the value listed in Table 3 (2000 volts).

Our method for determining the best estimate of the ESD failure threshold is a simple linear interpolation between a device's "pass" and "fail" voltage levels. Other methods of determining a failure threshold estimate exist. We will discuss two additional methods in a later section of this paper for the purpose of examining the robustness of our correlation analysis.

Table 4: "Best Estimate" Failure Thresholds

Device	HBM ESD (V)	MM ESD (V)	FCDM ESD (V)
X1	250	50	750
X2	1250	75	2000
Х3	3500	350	750
X4	1250	100	750
X5	2250	225	750
X6	4250	275	750

FAILURE ANALYSIS PROCEDURE

Once all experimental devices had been functionally tested, the devices failing the electrical testing acceptance criteria were submitted for failure analysis. Each device's failure location and signature were determined and documented for each ESD model.

The failure analysis techniques used by each participating company were universal and tend to follow the same structured flow [15]. First, the failure was verified using microscopes, curve tracing equipment, and automated test equipment (ATE). The failing component was then decapsulated and examined using optical microscopy, emission microscopy, and liquid crystal techniques.

When the failure could not be easily located, circuit analysis and fault isolation procedures were required; this normally involved the utilization of a microprobe station, Electron-beam test system (E-beam), or ion mill (Focused Ion Beam). Once the failure site was identified, subsurface analysis was required to further reveal the damage location. These techniques included cross-sectioning and Scanning Electron Microscopy (SEM). The failure signature was then documented and photographed.

FAILURE MODE ANALYSIS RESULTS AND DISCUSSION

Failure mode analysis procedures were aimed at establishing a physical signature associated with electrical failure of a device at the ESD threshold. All results are summarized in Table 5.

Nomarksi phase contrast and scanning electron microscopy (SEM) were performed on a number of ESD damaged devices. Failure analysis revealed the failure signatures to be consistent with classical ESD failure signatures:

- · Gate oxide damage
- Poly-filament & Poly-extrusion
- Metal melt filament through a junction
- · Contact spiking
- Metal burn-out

SEM examinations revealed that two HBM simulators performing ESD stressing at the same stress voltage level can produce different failure signatures for the same device [16] (see Figures 4 and 5). In addition, device X5 results indicate that the three ESD models produced three different failure signatures as shown in Figures 4 through 7.



Figure 4: Device X5; Delco stressing; HBM ESD failure signature showing poly-extrusion damage of an I/O pin protection circuitry NMOS transistor. Poly-extrusion damage resulted in shorting of the gate to drain.



Figure 5: Device X5; Ford stressing; HBM ESD failure signature showing gate oxide damage of an internal NMOS transistor.



Figure 6: Device X5; Delco and Ford stressing; MM ESD failure signature showing metal melt damage of an NMOS transistor located in the ESD protection circuitry.



Figure 7: Device X5; AT&T stressing; FCDM ESD failure signature showing gate oxide and poly-filament damage of an internal PMOS transistor.

Examination of failure analysis results for device X4 also indicates that a single failure signature (e.g., gate oxide damage) can be produced by all three ESD models on the same device (see Figures 8, 9, and 10).



Figure 8: Device X4; Delco and Ford stressing; HBM ESD failure signature showing gate oxide damage of an internal NMOS transistor.



Figure 9: Device X4; Delco and Ford stressing; MM ESD failure signature showing gate oxide damage of an internal PMOS transistor.



Figure 10: Device X4; AT&T stressing; FCDM ESD failure signature showing gate oxide damage of an internal NMOS transistor.

For device X3, Machine Model ESD stressing by Delco produced multiple failure signatures including metal burn-out (see Fig. 11), contact spiking (see Fig. 12), and gate oxide damage (see Fig. 13). Machine Model stressing by Ford, however, produced only the metal burn-out failure signature (see Fig. 11). Contact spiking was common to both Machine Model and Human Body Model ESD stressing by Delco (see Figures 12 and 14, respectively) while gate oxide damage was common to both Machine Model (Delco stressing) and Charged Device Model ESD stressing (see Figures 13 and 15, respectively).



Figure 11: Device X3, Delco and Ford stressing, MM ESD failure signature showing metal burn-out of an ESD protection circuitry Ground runner.



Figure 12: Device X3; Delco stressing; MM ESD failure signature showing contact spiking on an ESD protection circuitry resistor.



Figure 13: Device X3; Delco stressing; MM ESD failure signature showing gate oxide damage of an ESD protection circuitry NMOS transistor.



Figure 14: Device X3; Delco stressing; HBM ESD failure signature showing contact spiking on an ESD protection circuitry resistor.



Figure 15: Device X3; AT&T stressing; FCDM ESD failure signature showing gate oxide damage of an internal NMOS transistor.

Electrical testing of device X1, following HBM ESD stressing, indicated a short between Ground and substrate. Light emission analysis failed to reveal any defects under various biasing conditions. Further deprocessing also failed to reveal any visible defects. This may be due to the lowest stress voltage level (500 V) that created the ESD failure, as indicated in Table 3.

Based upon the results of the ESD stressing, we found that the failure signatures (as listed in the last column of Table 5) show only moderate overlap between the HBM and MM ESD stressing. However, even a complete overlap may not show a good correlation. This was demonstrated in a 1993 study [5] where there was only one failure signature (gate oxide breakdown) created by HBM, CDM, and "real world" ESD events. The complete overlap of the single failure signature did not result in a high degree of correlation because the failure site distribution patterns, when examined statistically, were completely different. In fact, the CDM damage pattern [5] had a high degree of correlation with the damage pattern obtained from field failures. The study [5] also indicated that failure signatures alone are a poor indicator of correlation. Similarly, the multiple failure signatures shown in Table 5 are not indicative of non-correlation; other factors must be considered. If we examine other failure characteristics shown in Table 5, we find that the failing pins, circuitry, and structures (shown in the third, fourth, and fifth columns of Table 5, respectively) show a strong correlation between HBM and MM.

Table 5: Device Failure Mode Results

Test Sample	ESD Model & Stressing Company	Failing Pin (Input, Output, Power)	Failing Circuitry (Protection, Internal)	Failing Structure (PMOS, NMOS, Diode)	Failure Signature
	HBM / Delco	Output	Protection	Diode	FMA Inconclusive
	HBM / Ford	Output	Protection	Diode	FMA Inconclusive
X1	MM / Delco	Output	Protection	Diode	Junction Damage
	MM / Ford	Output	Protection	Diode	Junction Damage
	FCDM / AT&T	VDD	Protection	PMOS	Gate Oxide
	HBM / Delco	I/O	Protection	NMOS	Gate Oxide
	HBM / Ford	I/O	Protection	NMOS	Gate Oxide
X2	MM / Delco	I/O	Protection	Diode	Junction Damage
	MM / Ford	I/O	Protection	Diode	Junction Damage
	FCDM / AT&T	No Fail	No Fail	No Fail	No Fail
	HBM / Delco	Output	Protection	Resistor	Contact Spiking
	HBM / Ford	GND	Protection	GND Runner	Metal Burn-out
X3	MM / Delco	Input, Output, & GND	Protection	GND Runner, Resistor, & NMOS	Metal Burn-out, Contact Spiking, & Gate Oxide
	MM / Ford	GND	Protection	GND Runner	Metal Burn-out
	FCDM / AT&T	I/O	Internal	NMOS	Gate Oxide
	HBM / Delco	I/O & VDD	Internal	NPN & PMOS	Contact Spiking & Gate Oxide
	HBM / Ford	Input	Internal	NMOS	Gate Oxide
X4	MM / Delco	VDD	Internal	PMOS	Gate Oxide
	MM / Ford	I/O & VDD	Internal	PMOS & NMOS	Gate Oxide & Contact spike
	FCDM / AT&T	Input	Internal	NMOS	Gate Oxide
	HBM / Delco	I/O	Protection	NMOS	Poly-extrusion
	HBM / Ford	VDD	Internal	NMOS	Gate Oxide
X5	MM / Delco	VDD	Protection	NMOS	Metal melt
	MM / Ford	VDD	Protection	NMOS	Metal melt
	FCDM / AT&T	VDD	Internal	PMOS	Gate Oxide & Poly-filament
	HBM / Delco	I/O	Protection	NMOS	Gate Oxide
	HBM / Ford	I/O	Protection	NMOS	Gate Oxide
X6	MM / Delco	No Fail	No Fail	No Fail	No Fail
	MM / Ford	I/O	Protection	NMOS & PMOS	Metal melt & Contact Spiking
	FCDM / AT&T	I/O	Protection	PMOS	Gate Oxide & Poly-filament

CORRELATION OF ESD THRESHOLDS

Using the failure threshold information found in Table 4, a correlation coefficient analysis [17] was performed for each pair of ESD model thresholds. The following summary table (Table 6) lists the corresponding correlation coefficients.

	Table 6:	ESD model	correlation	coefficients
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ESD Model Correlation Coefficient		Regression Analysis	
HBM to CDM	0.28	V _{HBM} = (1.63) x V _{CDM}	
HBM to MM	0.92	V _{нвм} = (11.73) x V _{MM}	
CDM to MM	0.42	V _{CDM} = (3.37) x V _{MM}	

As had been expected, the HBM and MM ESD thresholds have a high degree of correlation (with a correlation coefficient of 0.92) as compared to the other two model pairs (with relatively low correlation coefficients of 0.28 for HBM vs FCDM and 0.42 for CDM vs MM). The failing pins and failing locations also show a high correlation between the HBM and MM ESD models, consistent with the findings reported in a 1992 study (see Table C of [1]).

Regression analysis for the model Y = bX was also conducted. The results are shown in Table 6. These results clearly indicate that the HBM threshold is roughly twelve times (12X) higher than the MM threshold for the CMOS devices examined in this study. The other two regression results are not of interest due to the low correlation coefficients.

To determine the robustness of our correlation analysis, we also calculated correlation coefficients using the first-fail values, shown in Table 7, as the definition of "failure threshold" [1]. The results again show a high degree of correlation between the HBM and MM ESD models (a coefficient of 0.93 and a regression model of $V_{HBM} = (11.64) \times V_{MM}$). The first-fail correlation results between the HBM and CDM ESD models and the CDM and MM ESD models were relatively low (0.29 and 0.36, respectively), also consistent with our results.

Table 7: "First Failure" Failure Thresholds

Device	HBM ESD (V)	MM ESD (V)	FCDM ESD (V)
X1	500	50	1000
X2	1500	100	2500
Х3	4000	400	1000
X4	1500	100	1000
X5	2500	250	1000
X6	4500	300	1000

Another method of analyzing device failures is the use of probability distribution plots [16,18]. If a 50% value for the cumulative probability plot is used as the definition of "failure threshold" (see Table 8), consistent results are similarly obtained. The 50% value correlation analysis results show an even higher degree of correlation between the HBM and MM ESD models (a coefficient of 0.96 and a regression model of $V_{HBM} = (11.95) \times V_{MM}$). The 50% correlation results between the HBM and CDM ESD models and the CDM and MM ESD models were significantly lower (0.05 and 0.10, respectively).

Table 8: "50% Value" Failure Thresholds

Device	HBM ESD (V)	MM ESD (V)	FCDM ESD (V)
X1	250	50	750
X2	1250	100	2250
X3	4254	350	1121
X4	1100	111	750
X5	2544	280	750
X6	4378	300	1121

DISCUSSION OF THRESHOLD CORRELATION

In this section, we compare our results with other researchers. It is important to note that MM and CDM test methods were not fully developed in the industry until recently. Quality of data for earlier work may have reflected the immaturity of test methods. We will discuss the most recent work first. There is a 1995 report [19] on the HBM and CDM thresholds for CMOS that results in a correlation coefficient of 0.33, as compared to the 0.28 correlation coefficient we have obtained. These two numbers indicate that the correlation between HBM and CDM thresholds is low.

In a study conducted in 1992 [1], a comparison was made for the MM and HBM thresholds of sub-micron CMOS technologies for different pin combinations. The authors of the study had hoped to use median failure data, but the required stress voltage levels exceeded the simulator capacity. Consequently, four pairs of first-failure data were obtained with a very narrow range of threshold spread. The MM threshold spread was from 340 volts to 380 volts, or 10%, and the HBM threshold spread was from 8000 volts to 9000 volts, or 13%. The authors of the 1992 study included a fifth pair from the median failure threshold to "improve data completeness." The spreads, however, remained very small: 22% for MM and 40% for HBM. Using the first four pairs of first-failure data reported in the 1992 study, we calculated a correlation coefficient of 0.64. If all five data pairs were used, the correlation coefficient became 0.69 with a slope of 23 (as compared to a slope of 12 calculated in this paper) for the Y = bX regression analysis. By comparison, the ESD threshold spread, as determined in this paper, is much broader and ranges from 50 volts to 350 volts, or 86%, for MM and from 250 volts to 4250 volts, or 94% for HBM.

A study conducted in 1989 [2] reported HBM and MM ESD thresholds using IMCS (HBM and MM) and ETS (HBM only) simulators (the ESD Association MM ESD test method was not approved until June of 1994). All devices examined in the study were of CMOS technologies. Using the nearly 50 pairs of IMCS first-failure data as reported in the study, we calculated a correlation coefficient of 0.31. We also noticed that some of the devices (e.g., devices I2 and K) had MM thresholds as much as 2 times (2X) higher than the corresponding HBM thresholds (e.g., HBM = 1100 volts and MM = 2200 volts for device K using a negative stress voltage applied with respect to VDD). It is our opinion that the MM simulator used in the 1989 study was erratic.

CONCLUSION

More than 900 packaged CMOS ICs were used for the ESD evaluation reported in this paper. Electrical and physical failure analyses were conducted for failed devices. Threshold voltage levels were determined for all three ESD models and their correlation and regression analyses were performed. From our failure signature analysis, the following conclusions were reached:

- Two HBM ESD simulators produced different failure signatures on the same device at the same stress voltage level. This was also observed for the two MM ESD simulators.
- For device X5, the three ESD models produced three different failure modes (i.e., failure structure and signature).
- Similar gate oxide failure signatures can be produced by all three ESD models on the same device (device X4)
- The FCDM failure signatures were related only to the gate oxide area of the CMOS devices evaluated.
- Since failure signatures do not correlate for the same ESD model (HBM or MM) using different simulators, we believe failure signatures are a poor correlation indicator between different ESD models.

It was also discovered that the HBM and MM ESD models exhibited a relatively high degree of correlation for failure threshold levels. Our best estimates of ESD threshold levels for all three ESD models resulted in a 92% correlation coefficient between the HBM and MM ESD model thresholds. However, we did not observe a proportionally high degree of overlap in the failure signatures of the HBM and MM ESD models. This may be due to several variables including differences in simulator parasitics, stressing procedures, and variability allowed by current industry ESD test standards. On the other hand, our study does show that the HBM and MM threshold correlation is a robust metric, insensitive to the differences between failure signatures for HBM and MM ESD.

From our study on the failure threshold voltages and failure modes, we found that FCDM ESD tends to generate failure mechanisms not always reproducible by HBM or MM ESD, a conclusion consistent with other work [20,21]. Though the three ESD models and simulators created multiple failure signatures, they do not exhibit a high degree of overlap. Our results indicate a high correlation between the ESD thresholds, failing pins, failing circuitry, and failing structures for HBM and MM stressing of the device codes evaluated.

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