Automotive Electronics Council
Component Technical Committee

ATTACHMENT 5

AEC - Q101-005 Rev-A

CHARGED DEVICE MODEL (CDM)

ELECTROSTATIC DISCHARGE (ESD) TEST

Automotive Electronics Council

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Acknowledgment

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Council would especially like to recognize the following significant contributors to the revision of this document:

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Change Notification

The following summary details the changes incorporated into AEC-Q101-005 Rev-A:

- **Added Cover Page, Acknowledgement Page, Notice Page, and Change Notification Page.**
- **Section 1.2, Reference Documents: Added ANSI/ESDA/JEDEC JS-002 standard document reference and deleted ESDA S5.3.1 and JEDEC JESD22-C101 standard document references.**
- **NEW - Section 2, Additional Requirements (addendum to JS-002): Added new section of specific AEC-Q101-005 requirements beyond those stated in JS-002, including:**
  - **Section 2.1, Tester and Device Preparation**
  - **Section 2.2, Measurements**
  - **Section 2.3, Sample Size**
  - **Section 2.4, Discharge Requirements**
  - **Section 2.5, Detailed Procedure**
  - **Section 2.6, Small Package Considerations**
  - **Section 2.7, Wafer or Bare Die Considerations**
  - **Section 2.8, Failure Criteria**
  - **Section 2.9, Acceptance Criteria**
  - **Section 2.10, Test Reporting**
- **NEW - Table 2, Discrete Semiconductor CDM ESD Classification Levels: Modified content of Table 2 to align Classification Levels and Maximum Withstand Test Condition Levels with JS-002.**
- **NEW – Figure 1, Recommended Discrete Semiconductor CDM ESD Test Flow Diagram: Modified content of Figure 1 to align Classification Levels and Maximum Withstand Test Condition Levels with Table 2 and JS-002.**

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METHOD - 005

DISCRETE SEMICONDUCTOR CHARGED DEVICE MODEL (CDM) ELECTROSTATIC DISCHARGE (ESD) TEST

All CDM ESD testing performed on Discrete Semiconductor devices to be AEC Q101 qualified shall be per the latest version of the ANSI/ESDA/JEDEC JS-002 specification with the following clarifications and requirements. Text enhancements and differences made since the last revision of this document are shown as underlined areas.

1. SCOPE

1.1 Description

The purpose of this specification is to establish a reliable and repeatable procedure for determining the CDM ESD sensitivity for discrete semiconductor devices.

1.2 Reference Documents:

ANSI/ESDA/JEDEC JS-002, Charged Device Model (CDM), Device Level

2. Additional Requirements (addendum to JS-002)

2.1 Tester and Device Preparation

2.1.1 Devices used for CDM stressing shall not have been used for any prior stress tests.

2.1.2 ESD damage prevention procedures shall be used before, during, and after CDM and post parametric testing.

NOTE: See the latest revision of ANSI/ESD S20.20, JESD625, IEC 61340-5-1 or company-specific handling procedures for guidance.

2.1.3 Devices shall be clean before testing. If needed, cleaning should be completed in compliance with company-approved procedures.

NOTE: Isopropanol (isopropyl alcohol) is typically used for cleaning.

2.1.4 The CDM tester probe and field plate / dielectric shall be clean and dry before testing. Cleaning may be performed periodically or based on waveform acceptance using isopropanol (isopropyl alcohol).

NOTE: Surfaces should be allowed to dry before testing.

2.1.5 Determination and setting of CDM field plate voltage factor and voltage offsets may only be done during full qualification of the CDM test system. Voltage factors and voltage offsets may not be adjusted based on routine waveform verification or based on product test waveforms or results.

NOTE: Section 6.5.2 of JS-002 describes conditions requiring CDM test system qualification or -re-qualification.

2.1.6 The same voltage factor adjustments and voltage offsets from qualification shall be used for product at all test conditions and polarities. The qualification procedure described in JS-002 Annex G.1 shall be used for both positive and negative stress determination of offsets to provide separate uniform positive stress offsets and uniform negative stress offsets.

2.2 Measurements

Prior to ESD testing, complete parametric testing (initial electrical verification) shall be performed on all sample groups and all devices in each sample group per applicable user device specification at room temperature followed by hot temperature, unless specified otherwise in the user device specification. A data log of each device shall be made listing all parameter measurements as defined in Table 1. The data log will be compared to the parameters measured during final electrical verification testing to determine the failure criteria of Section 2.8.

2.3 Sample Size

Each sample group shall be composed of ten (10) devices per stress test condition. Each sample group shall have all device pins and/or terminals stressed at one (1) test condition level, following the recommended test flow diagram of Figure 1. Each stress test condition requires a new sample group of ten (10) devices.

2.4 Discharge Requirements

The use of three (3) discharges at each stress level is required. Three (3) positive followed by three (3) negative discharges is also allowed, as well as three alternating sets of positive and negative discharges. Please refer to Annex F of JS-002 for detailed procedure of the single and dual discharge procedures.

2.5 Detailed Procedure

The ESD testing procedure shall be per one of the three options below:

2.5.1 CDM ESD Test Procedure - Option 1

Separate test sample groups shall be submitted for every classification test condition per Section 2.9 and Figure 1 followed by functional testing.

2.5.2 CDM ESD Test Procedure - Option 2

Test samples shall be submitted for the lowest starting test condition per Section 2.9 and Figure 1 followed by functional test. If all samples pass, the same samples, or fresh samples, are then stressed at the next higher classification test condition and functionally tested. This procedure shall be followed until the failing test condition is reached or the samples pass TC 1000.

2.5.3 CDM ESD Test Procedure - Option 3

The ESD testing procedure shall be per the recommended test flow of Figure 1 and as follows:

a. Place clean DUT “dead-bug” with device body in direct contact with the dielectric on top of the field plate.

b. Follow the recommended test flow diagram of Figure 1. Set the test condition stress level to positive TC 500.

c. Elevate the potential of the DUT by applying the TC 500 stress level to the field plate.

d. Select a PUT and ground (discharge) the DUT, using either discharge method as described in Annex F of JS-002.

e. If using the single discharge procedure, set the test condition stress level to negative TC 500, select the same PUT as in step (d) and ground (discharge) the DUT. If using the dual discharge procedure, this step has already been completed.

f. Repeat steps (c) through (e) using the next PUT. The use of a new sample group for each stress polarity is also acceptable.

g. Repeat steps (b) through (f) until every PUT (all device pins, including power and ground pins) is discharged at the specified test condition level and polarity.

h. Test the next device in the sample group and repeat steps (a) through (g) until all devices in the sample group have been tested at the specified test condition level and polarity.

i. Submit the devices for complete parametric testing (final electrical verification) per the user device specification at room temperature followed by hot temperature, unless specified otherwise in the user device specification, and determine whether the devices meet the acceptance criteria specified in Section 2.9. It is permitted to perform the parametric testing (final electrical verification) per user device specification after all sample groups have been stressed.

j. Using the next sample group, select the next test condition stress level as specified in Figure 1 and repeat steps (a) through (i).

k. Repeat steps (a) through (j) until failure occurs or the device fails to meet the TC 125 stress test condition.

2.6 Small Package Considerations

CDM testing of discrete semiconductors in small packages is very challenging. The vacuum used to hold the package in place during testing is not effective when the package is under a few square millimeters. The capacitance between the device under test and the field plate is also very small, which results in very fast CDM current pulses. These pulses have non-negligible peak currents, but have very fast rise times and very narrow pulse widths, making the pulses impossible to measure with standard 1 GHz measurement systems. Additionally, the total charge within the pulses is so small that CDM failures of discrete semiconductors in very small packages have seldom been seen. For these reasons, the testing of discrete semiconductors in very small packages is often not performed (as agreed between supplier and customer) due to the difficulty of testing and the very low chance of failure. Any device or package that could not be completely CDM stressed due to package size shall be recorded.

2.7 Wafer or Bare Die Considerations

The test methods described in this standard may also be used to evaluate devices that are shipped as wafers or bare dice. Standardized CDM stressing of wafers or bare dice is not defined due to equipment limitations. Products shipped as bare dice may be placed in a package for purposes of performing CDM stressing, as determined by package test limitations and agreement between supplier and customer. The package used for this stressing shall be recorded.

2.8 Failure Criteria

A device will be defined as a failure if, after exposure to ESD pulses, the device fails any of the following criteria:

a. The device exceeds the allowable shift values for the specific key parameters listed in Table 1. Other device parameters and allowable shift values may be specified in the user device specification. During initial parametric testing, a data log shall be made for each device listing the applicable parameter measurement values. This data log will be compared to the parameters measured during final parametric testing to determine the shift value. Devices exceeding the allowable shift value will be defined as a failure.

b. The device no longer meets the user device specification requirements. Complete parametric testing (initial and final electrical verification) shall be performed per applicable user device specification at room temperature followed by hot temperature, unless specified otherwise in the user device specification.

Table 1: Key Parameters and Allowable Shift Values

Device Type	Parameters	Maximum Allowable Shift Values
Bipolar	I_{CES}, I_{CBO}, and I_{EBO}	Ten times (10X) the initial measurement
FET	I_{DSS} and I_{GSS}	Ten times (10X) the initial measurement
IGBT	I_{CES} and I_{GES}	Ten times (10X) the initial measurement
Diode	I_R	Ten times (10X) the initial measurement

2.9 Acceptance Criteria

A device passes a stress test condition level if all devices stressed at that test condition level and below pass. All the samples must meet the measurement requirements specified in Section 2.2 and the failure criteria requirements specified in Section 2.8. Using the classification levels specified in Table 2, the supplier shall classify the devices according to the maximum withstand test condition level. Due to the complex nature of the CDM event, a change in manufacturing process, design, materials, or device package may require reclassification according to this test method.

Table 2: Discrete Semiconductor CDM ESD Classification Levels

Classification Level	Maximum Withstand Test Condition
C0a	< TC 125
C0b	TC 125 to < TC 250
C1	TC 250 to < TC 500
C2a	TC 500 to < TC 750
C2b	TC 750 to < TC 1000
C3	TC 1000 [1]

[1] For test conditions above TC 1000, depending on geometry of the device package, corona effects may limit the actual pre-discharge voltage and discharge current.

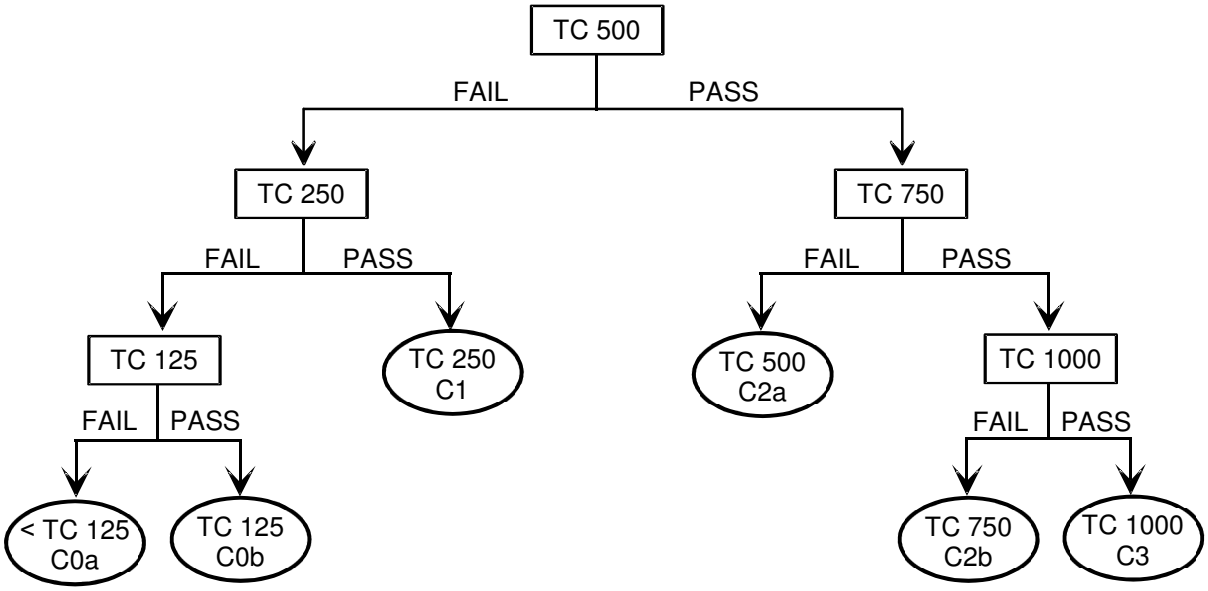

Figure 1: Recommended Discrete Semiconductor CDM ESD Test Flow Diagram

2.10 Test Reporting

Upon completion of the required testing defined herein, a report of the testing performed and detailed results, as defined below, including any deviations, shall be submitted to the user upon request.

a. Sample Details
- Package configuration (e.g., lead pitch, pin count, lead form, etc.)
- Sample sizes

b. Test Details
- Discharging method (e.g., single or dual)
- Stress test condition (TC) levels
- Test/Pin partitioning (if applicable)
- Package orientation during testing
- Exceptions to any tests performed
  - Special considerations for small packages
  - Mounting package on a surrogate
  - Wafer/bare die

c. Test Results
- Summary of results

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Revision History

Rev #	Date of change	Brief summary listing affected sections
-	July 18, 2005	Initial Release.
A	Jan. 29, 2019	Complete revision. Added reference to ANSI/ESDA/JEDEC JS-002 as accepted Charged Device Model Standard document. Added new Section 2, Additional Requirements (addendum to JS-002), listing specific AEC-Q101-005 requirements beyond those stated in JS-002.