Automotive Electronics Council
Component Technical Committee

ATTACHMENT 5

AEC - Q101-005 Rev-

CAPACITIVE DISCHARGE MODEL (CDM) ELECTROSTATIC DISCHARGE (ESD) TEST

Automotive Electronics Council
Component Technical Committee

METHOD - 005

DISCRETE COMPONENT
CHARGED DEVICE MODEL (CDM)
ELECTROSTATIC DISCHARGE (ESD) TEST

1. SCOPE

1.1 Description:

The purpose of this specification is to establish a reliable and repeatable procedure for determining the CDM ESD sensitivity for electronic components. This test method does not include socketed CDM.

1.2 Reference Documents:

ESD Association Specification STM5.3.1
JEDEC Specification EIA/JESD22-C101

1.3 Terms and Definitions:

The terms used in this specification are defined as follows.

1.3.1 Charged Device Model (CDM) ESD:

An ESD pulse meeting the waveform criteria specified in this test method, approximating an ESD event that occurs when a component becomes charged (e.g., triboelectric) and discharges to a conductive object or surface.

1.3.2 Component Failure:

A condition in which a component does not meet all the requirements of the acceptance criteria, as specified in section 5, following the ESD test.

1.3.3 Device Under Test (DUT):

An electronic component being evaluated for its sensitivity to ESD.

1.3.4 Electrostatic Discharge (ESD):

The transfer of electrostatic charge between bodies at different electrostatic potentials.

1.3.5 Electrostatic Discharge Sensitivity:

An ESD voltage level resulting in component failure.

1.3.6 ESD Simulator:

An instrument that simulates the charged device model ESD pulse as defined in this specification.

1.3.7 Pin Under Test (PUT):

The pin and/or terminal under test; this includes all component pins as well as all power supply and ground pins.

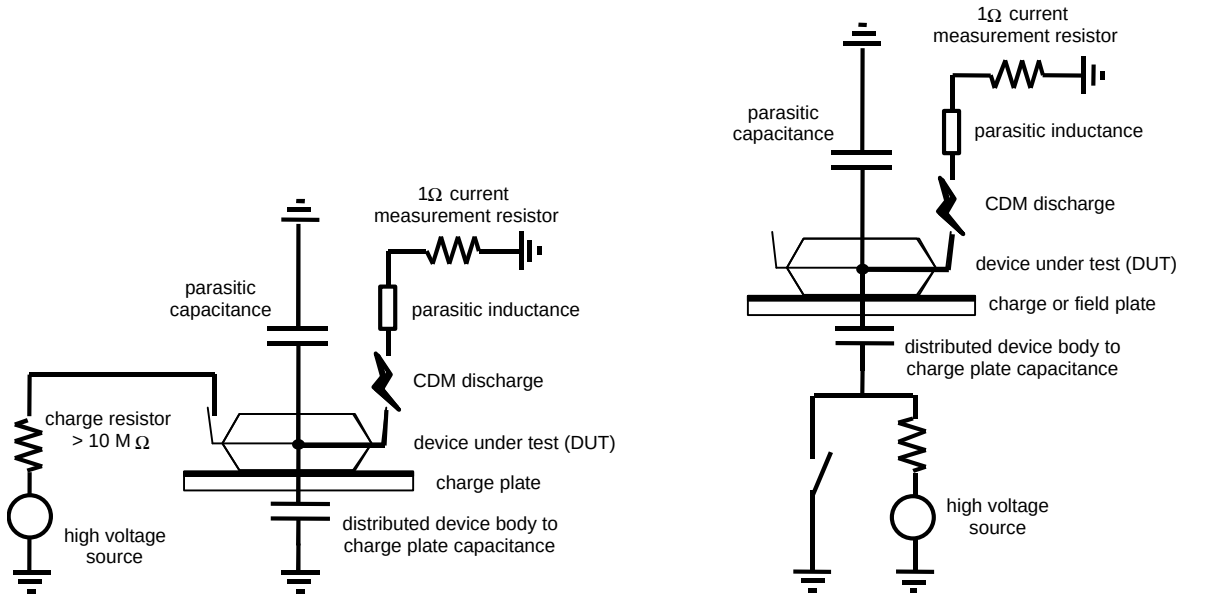
1.3.8 Withstanding Voltage:

The ESD voltage level at which, and below, the component is determined to pass the failure criteria requirements specified in section 4.

2. EQUIPMENT:

2.1 Test Apparatus:

The apparatus for this test consists of an ESD pulse simulator; Figure 1 shows a typical equivalent CDM ESD circuit. Other equivalent circuits may be used, but the actual simulator must be capable of supplying pulses that meet the waveform requirements of Table 2, Table 3, and Figure 3.



(a) Direct charge CDM **(b) Field induced charge CDM**

Note: Parasitics in the charge and discharge path of the test equipment can greatly affect test results

Figure 1: Charged Device Model ESD Typical Equivalent Circuit for (a) Direct Charge and (b) Field Induced Charge

2.2 Measurement Equipment:

Equipment shall include an oscilloscope/digitizer, current probe, attenuators, and cable/connector assemblies to verify conformance of the simulator output pulse to the requirements of this document as specified in Table 2, Table 3, and Figure 3.

2.2.1 Oscilloscope/Digitizer:

The oscilloscope/digitizer shall have a minimum bandwidth of 1.0GHz and nominal input impedance of 50Ω (Tektronix SCD1000, HP 7104, or equivalent).

2.2.2 Current Probe:

The current probe shall be an inductive current transducer or coaxial resistive probe with a minimum bandwidth of 5GHz.

2.2.3 Attenuator:

The attentuator, if required, shall be high precision (+0.1dB precision at 1.0GHz) with impedance of 50Ω.

2.2.4 Cable/Connector Assembly:

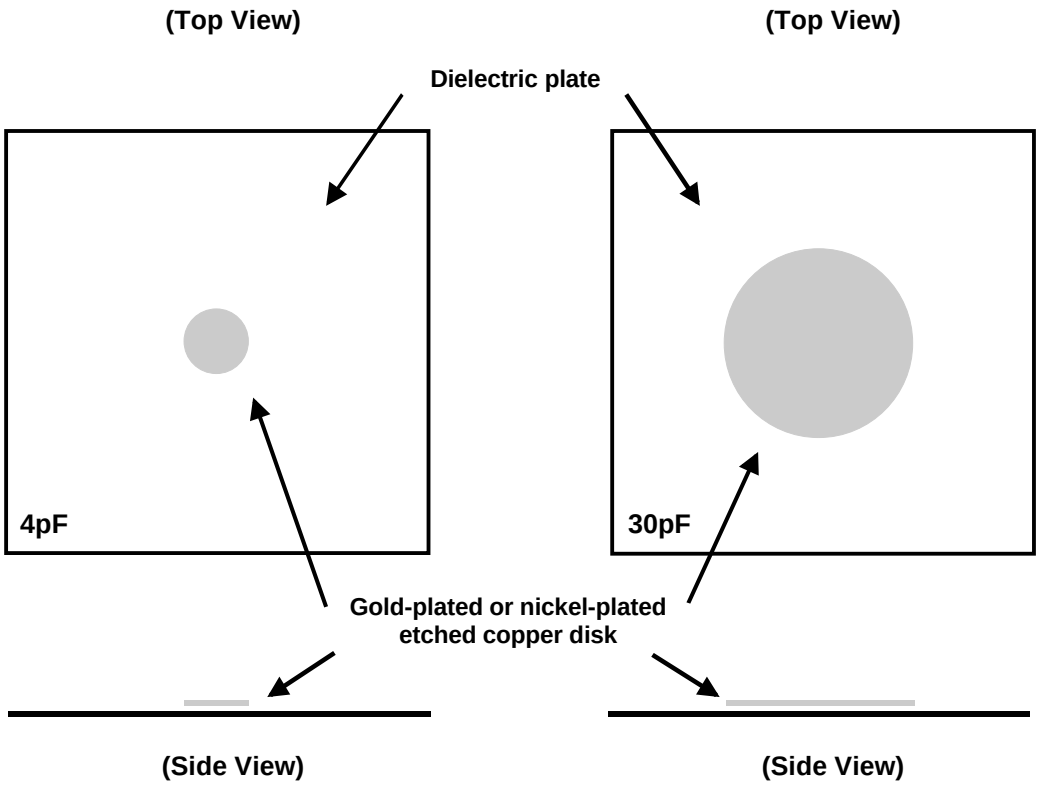
The cable/connector assembly, if required, shall be low loss (less than 0.4dB loss up to 1GHz) with impedance of 50Ω.

2.2.5 Verification Modules:

The two verification modules shall be gold-plated or nickel-plated etched copper disks on single sided FR-4 material (thickness = 0.8mm). The disks shall be: 1) a small disk (diameter approximately = 9 mm) configuration with a capacitance value of 4pF ±5% measured at 1MHz, and 2) a large disk (diameter approximately = 26mm) configuration with a capacitance of 30pF ±5% measured at 1MHz. Each disk shall be created using an etching process and centered on FR-4 material measuring at least 30mm by 30mm. Capacitance shall be measured with the non-metallized and non-disk side of the verification module in direct contact with the metal surface of a ground plane. Verification module parameters and illustrations are shown in Table 1 and Figure 2.

Table 1: Verification Module Parameters

Verification Module	Parameter	Accepted Value
4pF	Capacitance	3.8pF to 4.2pF
	Disk diameter	~ 9mm
	FR-4 material size	≥ 30mm by 30mm
	FR-4 thickness	0.8mm
30pF	Capacitance	28.5pF to 31.5pF
	Disk diameter	~ 26mm
	FR-4 material size	≥ 30mm by 30mm
	FR-4 thickness	0.8mm



(a) 4pF verification module (~ 9mm disk) **(b) 30pF verification module (~ 26mm disk)**

Figure 2: Verification Module Illustrations, (a) 4pF and (b) 30pF

2.2.6 Capacitance Meter:

The capacitance meter shall have a resolution of 0.2pF when measured at 1.0MHz with 3% accuracy.

2.3 Equipment Calibration and Qualification:

All peripheral equipment (including but not limited to the oscilloscope/digitizer, current probe, attenuators, cable/connector assemblies, verification modules, and capacitance meter) shall be periodically calibrated according to manufacturer's recommendations. A period of one (1) year is the maximum permissible time between full calibration tests. Qualification of the CDM simulator must be performed during initial acceptance testing or after repairs that are made to the equipment that may affect the waveform. The simulator must meet the requirements of Table 2 and Figure 3 for five (5) consecutive waveforms at all voltage levels using the 4pF verification module shown in Figure 2. Simulators not capable of producing the maximum voltage level shown in Table 2 shall be qualified to the highest voltage level possible. The simulator must also meet the requirements of Table 3 and Figure 3 for five (5) consecutive waveforms at the 500 volt level using the 30pF verification module shown in Figure 2. Thereafter, the test equipment shall be periodically qualified as described above; a period of one (1) year is the maximum permissible time between full qualification tests.

2.4 Verification Module Calibration:

The capacitance value of verification modules can be dramatically degraded by excessive use (indentations due to repetitive pogo pin contact, cracks in metallization, warping, etc.). Therefore, to ensure proper capacitance values, it is recommended that module capacitance be verified per section 2.4.1. When modules are degraded to the point they no longer meet the specified capacitance requirements shown in Table 1, they must be replaced.

2.4.1 Verification Module Capacitance Measurement Procedure:

a. Using the 4pF verification module, place the non-metallic side of the module in direct contact with the metallic surface of a ground plane. Capacitance measurements can be affected by air gaps between the module and the ground plane (e.g., due to warping of the FR-4 material, etc.). Therefore, the air space between the module and the ground plane must be minimized. This can be accomplished by applying slight pressure using the capacitance meter probes; care must be taken to avoid damaging the disk metallization.

b. Using the capacitance meter defined in section 2.2.6, measure the capacitance of the verification module to the ground plane. The capacitance value shall meet the requirements defined in Table 1.

c. Repeat steps (a) and (b) using the 30pF verification module.

2.5 Simulator Waveform Verification:

The performance of the simulator can be dramatically degraded by parasitics in the discharge path. Therefore, to ensure proper simulation and repeatable ESD results, it is recommended that waveform performance be verified using the 4pF verification module. The waveform verification shall be performed prior to performing CDM testing. If at any time the waveforms do not meet the requirements of Table 2 and Figure 3 at the 500 volt level, the testing shall be halted until waveforms are in compliance.

2.5.1 Waveform Verification Procedure:

a. Prior to performing waveform verification, verification modules and tester components (e.g., pogo pin, charge plate, etc.) must be cleaned with isoproponal (isopropyl alcohol) using a procedure approved by the user's internal safety organization. Once clean, avoid direct skin contact. If handling is required, the use of vacuum tweezers or personnel finger cots is strongly recommended.

b. Place the 4pF verification module in direct contact with the charge plate of the CDM simulator. If a dielectric film is used during component testing, it shall be less than 130 microns thick and must be in place during the waveform verification procedure.

c. Set the horizontal time scale of the oscilloscope at 0.5 nanoseconds per division or less.

d. Raise the charge plate potential to positive 500 volts. With the discharge pin centered within the 4pF metallic disk, bring the discharge pin in direct contact with the verification module and initiate a discharge.

e. Measure and record the rise time, first peak current, second peak current, third peak current, and full width at half height. All parameters must meet the limits specified in Table 2 and Figure 3.

f. Raise the charge plate potential to negative 500 volts. With the discharge pin centered within the 4pF metallic disk, bring the discharge pin in direct contact with the verification module and initiate a discharge.

g. Measure and record the rise time, first peak current, second peak current, third peak current, and full width at half height. All parameters must meet the limits specified in Table 2 and Figure 3.

Table 2: CDM Waveform Specification for 4pF Verification Module

Voltage Level (V)	1st peak current for 4pF I_{p1}(A) (±20%)	2nd peak current for 4pF I_{p2} (A)	3rd peak current for 4pF I_{p3} (A)	Rise Time t_r (ps)	Full width at half height for 4pF **FWHH** (ps)
250	2.25	< 50% of I_{p1}	< 25% of I_{p1}	< 400	< 600
500	4.50	< 50% of I_{p1}	< 25% of I_{p1}	< 400	< 600
1000	9.00	< 50% of I_{p1}	< 25% of I_{p1}	< 400	< 600
2000	18.00	< 50% of I_{p1}	< 25% of I_{p1}	< 400	< 600

Table 3: CDM Waveform Specification for 30pF Verification Module

Voltage Level (V)	1st peak current for 30pF * I_{p1} (A) (±20%)	2nd peak current for 30pF * I_{p2} (A)	3rd peak current for 30pF * I_{p3} (A)	Rise Time T_r for 30pF * (ps)	Full width at half height for 30pF * **FWHH** (ps)
500	14.00	< 50% of I_{p1}	< 25% of I_{p1}	< 400	< 1000

*** The 30pF verification module is used only during Equipment Qualification as specified in section 2.3.**

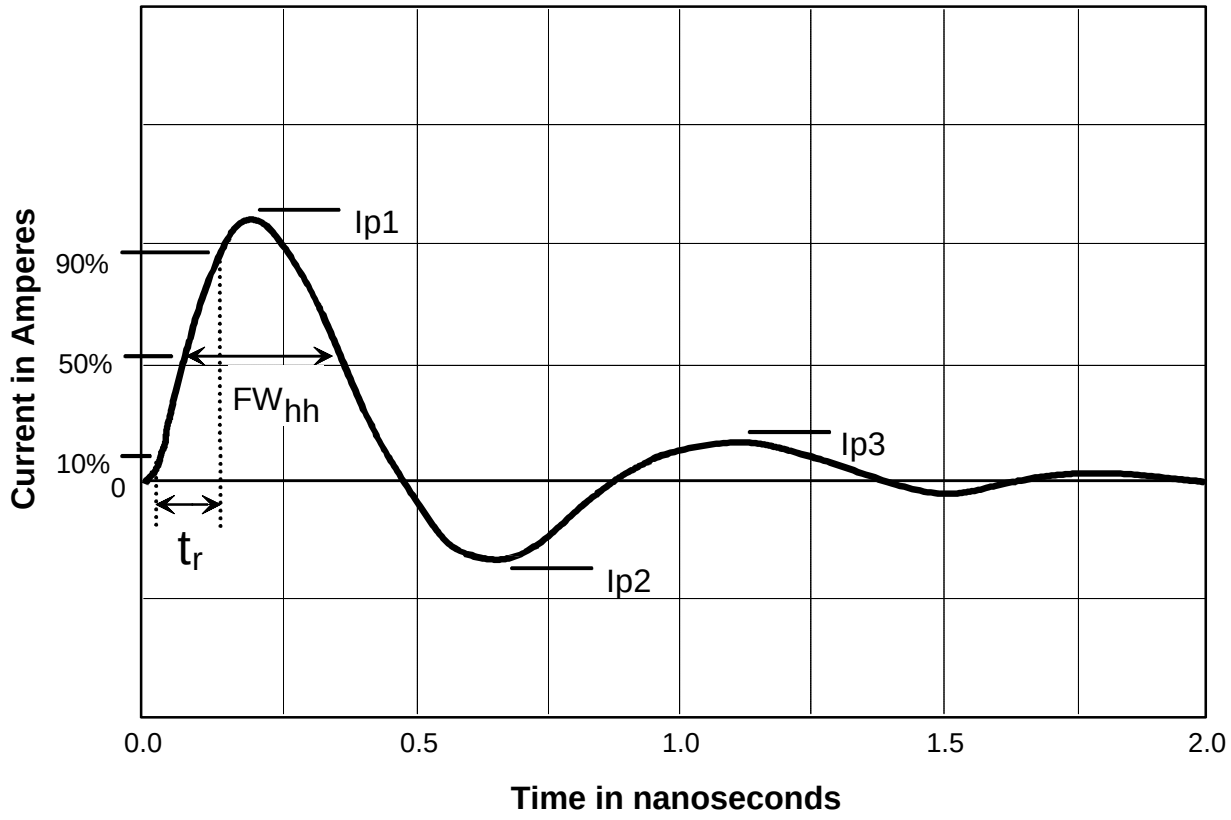


Figure 3: Typical CDM Current Waveform

3. PROCEDURE:

3.1 Sample Size:

Each sample group shall be composed of ten (10) components per stress voltage level. Each sample group shall have all component pins and/or terminals (including power and ground pins) stressed at one (1) voltage level, following the test flow diagram of Figure 4. Each stress voltage level requires a new sample group of ten (10) components.

3.2 Charging and Discharging Methods:

There are two acceptable methods of charging a DUT: Direct Charging and Field-induced Charging. Either method may be used to perform CDM ESD testing and must be recorded. While several methods exist for discharging a DUT, the direct contact discharge method is the only acceptable method to discharge a DUT for this test method.

3.2.1 Direct Charging Method:

The DUT is placed “dead-bug” (upside down with pins and/or terminals pointing up) with component body in direct contact with the charge plate and charged either through the pin(s) providing the best ohmic connection to the substrate of the DUT or through all DUT pins simultaneously (see Figure 1). To prevent damaging the DUT, ensure both the component and charging mechanism are at ground potential prior to initiating the CDM test. Contact to the charging pin(s) must be made prior to raising the charge potential. Once the DUT is charged, a pin under test (PUT) is discharged (except any pin(s) directly connected to the substrate of the

DUT). It is permissible to leave the charging probe in direct contact with the charging pin during the discharge event provided the discharge waveform meets the requirements of Table 2, Table 3, and Figure 3. After discharging the PUT, the DUT shall be re-charged and the process is repeated for each pin to be tested. All charge pins must be recorded.

3.2.2 Field-induced Charging Method:

The DUT is placed "dead-bug" (upside down with pins and/or terminals pointing up) with component body in direct contact with the field charging plate and charged by raising the potential of the charge plate (see Figure 1). To prevent damaging the DUT, ensure both the component and charge plate are at ground potential prior to initiating the CDM test. Once the DUT is charged, a pin under test (PUT) is discharged. After discharging the PUT, the DUT shall be re-charged and the process is repeated for each pin to be tested. The field charging plate shall be at least seven times (7X) larger in area than the DUT and shall meet the requirements of Table 2, Table 3, and Figure 3. If a dielectric film is used during component testing, it shall be less than 130 microns thick and must be in place during the waveform verification procedure.

3.2.3 Charging Small Components:

Small component packages may not be able to hold enough charge to meet the specified discharge voltage levels. For these packages, perform the test once and, if there is insufficient charge, the supplier must instead perform both HBM and MM ESD testing. The supplier shall document that the package could not hold sufficient charge to perform the CDM ESD test.

3.2.4 Direct Discharging Method:

Direct contact discharge is initiated within a relay and can add parasitics to the discharge path (care must be taken to minimize these parasitics). A discharge probe (e.g., pogo pin), connected to the relay, is placed in direct contact with the PUT and produces a very repeatable CDM event.

3.3 Test Temperature:

Each component shall be subjected to ESD pulses at room temperature.

3.4 Measurements:

Prior to ESD testing, complete parametric testing (initial electrical verification) shall be performed on all sample groups and all components in each sample group per applicable user device specification at room temperature followed by hot temperature, unless specified otherwise in the user device specification. A data log of each component shall be made listing all parameter measurements as defined in Table 4. The data log will be compared to the parameters measured during final electrical verification testing to determine the failure criteria of section 4.

3.5 Cleaning Method:

To avoid charge loss during CDM testing, components should be cleaned with isopropanol (isopropyl alcohol) using a procedure approved by the local safety organization. Components should then be handled only by vacuum tweezers, personnel wearing finger cots or equivalent, or plastic tweezers which have been neutralized by holding in an ionized air stream. The CDM tester should be cleaned periodically with isopropanol (isopropyl alcohol) to remove any surface contamination that could result in charge loss. Particular attention should be paid to the discharge probe, charging probe, and the charge plate on which the component is placed.

3.6 Detailed Procedure:

The ESD testing procedure shall be per the test flow diagram of Figure 4 and as follows:

a. Place clean DUT “dead-bug” (upside down with pins and/or terminals pointing up) with component body in direct contact with the charge plate.

b. Follow the recommended test flow diagram of Figure 4.

c. Select a charging method and charge the DUT to a positive potential.

d. Select a PUT and discharge the DUT. After discharging, wait a minimum of 1 second and re-charge the DUT. The use of three (3) discharges at each charge voltage polarity is required.

e. Set the charge voltage to a negative potential.

f. Repeat steps (c) through (d) using the same PUT.

g. Repeat steps (b) through (f) until every PUT (all component pins and/or terminals) is discharged at the specified voltage.

h. Test the next component in the sample group and repeat steps (a) through (g) until all components in the sample group have been tested at the specified voltage level.

i. Submit the components for complete parametric testing (final electrical verification) per the user device specification at room temperature followed by hot temperature, unless specified otherwise in the user device specification, and determine whether the components meet the failure criteria requirements specified in section 4. It is permitted to perform the parametric testing (final electrical verification) per user device specification after all sample groups have been tested.

j. Using the next sample group, select the next stress voltage level as specified in Figure 4 and repeat steps (a) through (i).

k. Repeat steps (a) through (j) until failure occurs or the component fails to meet the 125 volt stress voltage level.

4. FAILURE CRITERIA:

A component will be defined as a failure if, after exposure to ESD pulses, the component fails any of the following criteria:

1. The component exceeds the allowable shift values for the specific key parameters listed in Table 4. Other component parameters and allowable shift values may be specified in the user device specification. During initial parametric testing, a data log shall be made for each component listing the applicable parameter measurement values. This data log will be compared to the parameters measured during final parametric testing to determine the shift value. Components exceeding the allowable shift value will be defined as a failure.

2. The component no longer meets the user device specification requirements. Complete parametric testing (initial and final electrical verification) shall be performed per applicable user device specification at room temperature followed by hot temperature, unless specified otherwise in the user device specification.

Table 4: Key Parameters and Allowable Shift Values

Component Type	Parameters	Maximum Allowable Shift Values
Bipolar	I_{CES}, I_{CBO}, and I_{EBO}	Ten times (10X) the initial measurement
FET	I_{DSS} and I_{GSS}	Ten times (10X) the initial measurement
IGBT	I_{CES} and I_{GES}	Ten times (10X) the initial measurement
Diode	I_R	Ten times (10X) the initial measurement

5. ACCEPTANCE CRITERIA:

A component passes a voltage level if all components stressed at that voltage level and below pass. All the samples must meet the measurement requirements specified in section 3 and the failure criteria requirements specified in section 4. Using the classification levels specified in Table 5, the supplier shall classify the components according to the maximum withstanding voltage level. Due to the complex nature of the CDM event, a change in manufacturing process, design, materials, or component package may require reclassification according to this test method.

Table 5: Discrete Component CDM ESD Classification Levels

Component Classification	Maximum Withstand Voltage
C0	≤ 125 V
C1	> 125 V to ≤ 250 V
C2	> 250 V to ≤ 500 V
C3	> 500 V to ≤ 750 V
C4	> 750 V to ≤ 1000 V
C5	> 1000 V

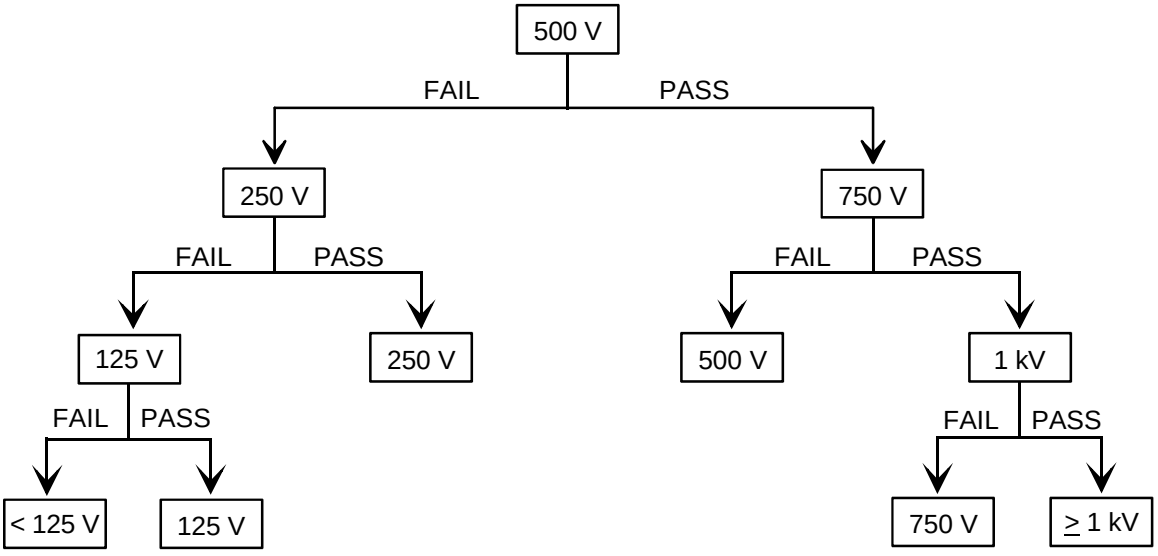


Figure 4: Discrete Component CDM ESD Test Flow Diagram

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Revision History

Rev #	Date of change	Brief summary listing affected sections
-	July 18, 2005	Initial Release.