Automotive Electronics Council
Component Technical Committee

ATTACHMENT 4

AEC - Q101-004 Rev-

MISCELLANEOUS TEST METHODS

Automotive Electronics Council

Component Technical Committee

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METHOD - 004

MISCELLANEOUS TEST METHODS

1. SCOPE

1.1 Description:

This document establishes the procedure and criteria for performing miscellaneous qualification tests referred to in Table 2 (Process Change Guidelines for the Selection of Tests) of AEC-Q101. The tests described in this document are:

Section 2 - Unclamped Inductive Switching (UIS)
Section 3 - Dielectric Integrity (DI)
Section 4 - Destructive Physical Analysis (DPA)

2. UNCLAMPED INDUCTIVE SWITCHING (UIS):

2.1 Description:

This test is used to determine the capability of a power MOSFET or IGBT to dissipate energy stored in an inductive load. Power MOSFETs have a parasitic back diode that is subjected to the energy stored in the inductor when the device is turned off, if no external clamp is provided. This test can also be used to determine ruggedness of IGBTs with a clamp incorporated within the package. Data generated by this test will be used to compare the ruggedness of power devices before and after various supplier initiated process changes. This is considered a destructive test. Devices subjected to the test shall not be shipped as production material.

2.2 Equipment:

The following equipment is required to conduct the test:

a. Oscilloscope with probes to measure drain current and voltage.
b. Inductors capable of handling the current range of interest without saturating.
c. Power supply capable of supplying the required voltage and current.
d. Pulse generator (to drive the gate).

2.3 Supplier Defined Variables:

a. Drain Current (I_D)
b. Gate Voltage (V_{GS})
c. Rated Breakdown Voltage ($V_{(BR)DSS}$)
d. Supply Voltage (V_{DD})
e. Time in Avalanche (t_{AV})
f. Inductance (L)

2.4 UIS Test Procedure:

2.4.1 The DUT is connected to the test fixture as shown in Figure 1.

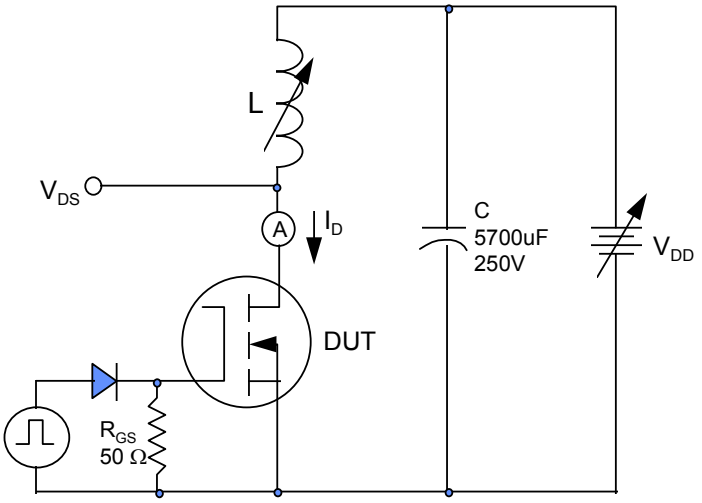

Figure 1: UIS Test Circuit

2.4.2 The Gate of the DUT is connected to a pulse generator to provide a single pulse with the signal level at the maximum rated gate to source voltage.

2.4.3 The gate is turned on allowing current to ramp in the inductor to the pre-determined value (see Figure 2).

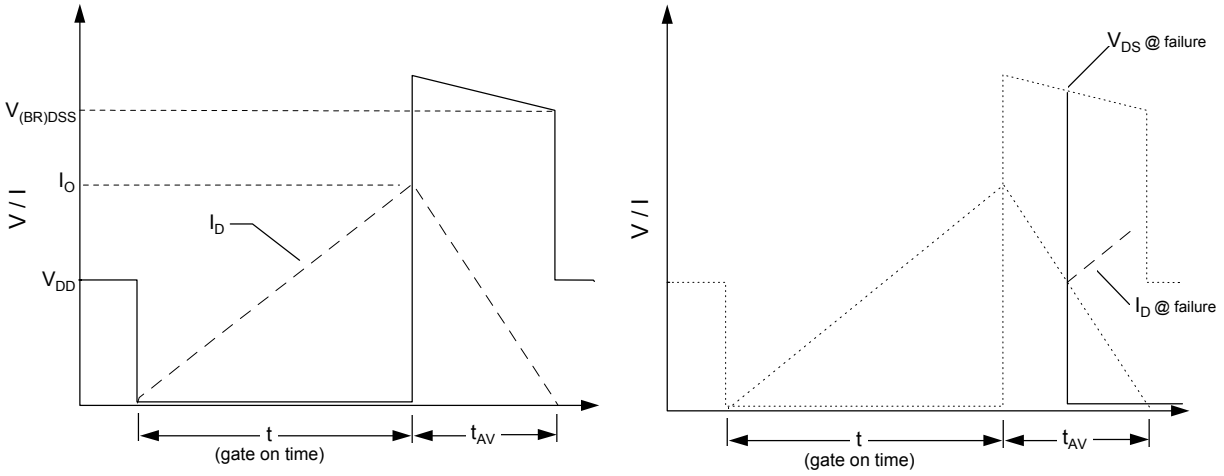

Figure 2: UIS Test Waveforms

2.4.4 When the pre-determined current value is reached, the gate is turned off, and the drain voltage and current is monitored (voltage & current) with an oscilloscope during reverse blocking to insure that the back diode clamps until the inductor energy is dissipated.

2.4.5 Increase the current in maximum 1 amp increments until failure. A failure is indicated by a collapse of the blocking voltage before the inductor energy is dissipated **OR** the presence of current flow after the inductor energy has dissipated (indicating latch-up).

2.4.6 Record I_{AV} & V_{DS} at the point where failure occurs. Capability is expressed as a function of the time in avalanche and current. Time in avalanche can be calculated using the formula:

$$t_{AV} = \frac{L * I_{AV}}{V_{DS\ @\ failure} - V_{DD}}$$

3. DIELECTRIC INTEGRITY (DI):

3.1 Description:

This test is used to determine the dielectric strength of the gate oxide of a power MOSFET or other MOS gated device. Data generated by this test will be used to compare the ruggedness of power devices before and after various supplier initiated process changes. This is considered a destructive test. Devices subjected to the test shall not be shipped as production material.

3.2 Equipment:

The following equipment is required to conduct the test:

a. Voltage controlled power supply
b. Sensitive current measurement instrument

3.3 Dielectric Integrity Test Procedure:

a. The DUT is connected to the test equipment as shown in Figure 3.

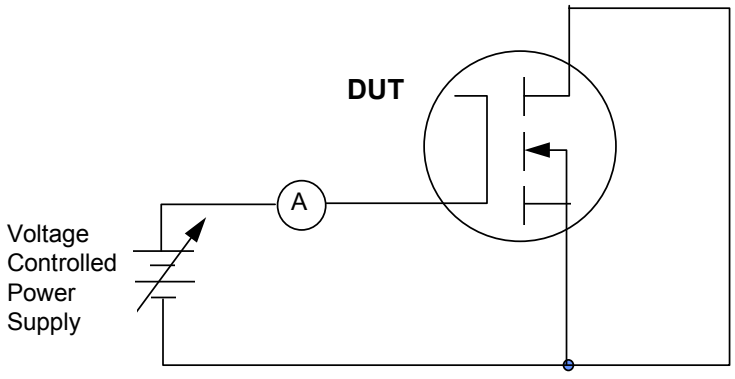

Figure 3: Dielectric Integrity Test Circuit

b. The voltage is increased in maximum 1 volt increments while the gate current is monitored.

c. Dielectric strength is defined as the gate voltage reading previous to which the gate current increases by an order of magnitude (from the previous reading).

d. Record and report this voltage and current for each DUT.

4. DESTRUCTIVE PHYSICAL ANALYSIS (DPA):

4.1 Description:

The purpose of this examination is to determine the capability of a device's internal materials, design, and workmanship to withstand forces induced by various stresses induced during environmental testing.

4.2 Equipment:

a. Optical microscope having magnification capability of up to 50X
b. De-capsulation equipment

4.3 Procedure:

a. Parts selected for this test must have successfully completed environmental testing as defined in Table 2 (Process Change Guidelines for the Selection of Tests) of AEC-Q101.

b. The parts shall be opened or de-capsulated in order to expose the internal die/substrate and determine the extent of any mechanical damage. The process used to de-capsulate the device must insure that it does not cause degradation of the leads and bonds. The internal die or substrate must be completely exposed and free of packaging material.

c. The devices shall be examined under a magnification of up to 50X to the criteria listed in section 4.4, herein.

d. Failed devices shall be analyzed to determine the cause of the failure. A Failure Analysis Report documenting this analysis shall be prepared on all failures. If the analysis shows that the failure was caused by the package opening process, the test shall be repeated on a second group of parts.

4.4 Failure Criteria:

Devices shall be considered failed if they exhibit any of the following:

a. Visible evidence of non-conforming to the devices' Certificate of Design, Construction and Qualification.
b. Visible evidence of corrosion, contamination, delamination or metallization voids.
c. Visible evidence of die/substrate cracks or defects (e.g. scratches, glassivation, etc.).
d. Visible evidence of wire, die, or termination bond defects.
e. Visible evidence of dendrite growth or electromigration.

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Revision History

Rev #	Date of change	Brief summary listing affected sections
-	May 15, 1996	Initial Release.