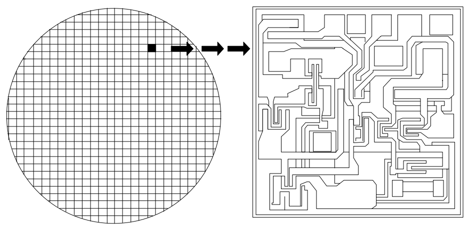
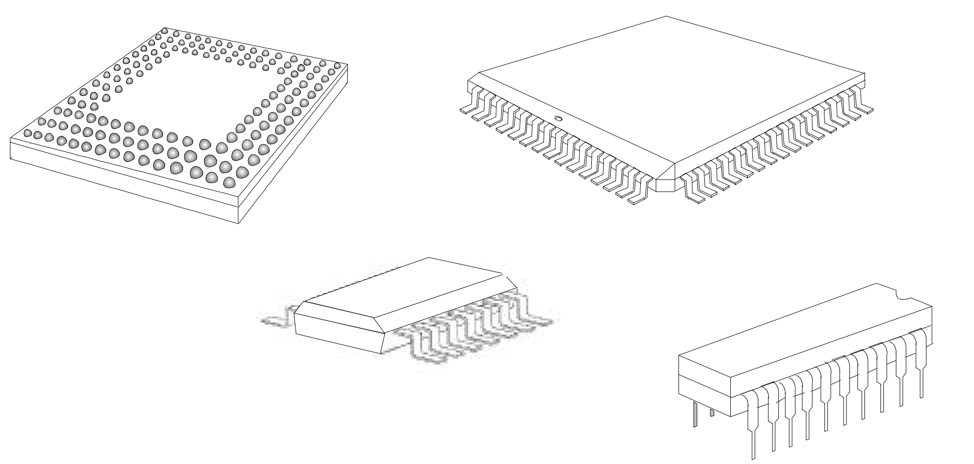
AEC - Q100 - REV-E
January 31, 2001



STRESS TEST QUALIFICATION FOR INTEGRATED CIRCUITS



Automotive Electronics Council
Component Technical Committee

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Acknowledgment

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STRESS TEST QUALIFICATION FOR PACKAGED INTEGRATED CIRCUITS

Text enhancements and changes made since the last revision of this document are shown as double underlined areas. Several figures have also been revised, but changes to those areas have not been underlined.

1. SCOPE

1.1 Description

This document contains a set of stress tests and defines the minimum stress test driven qualification requirements and references test conditions for qualification of integrated circuits (ICs) per this specification. This document also includes special requirements for Plastic Ball Grid Array (PBGA) type packages that use solder ball interconnects. Use of this document does not relieve the IC supplier of their responsibility to meet their own company's internal qualification program. In this document, "user" is defined as all customers using a device qualified per this specification. The user is responsible to confirm and validate all qualification data that substantiates conformance to this document. Supplier usage of the device temperature grades as stated in this specification in their part information is strongly encouraged.

1.1.1 Purpose

The purpose of this specification is to determine that a device is capable of passing the specified stress tests and thus can be expected to give a certain level of quality / reliability in the application.

1.1.2 Definition of Stress-Test Qualification

Stress-Test "Qualification" is defined as successful completion of the test requirements outlined in this document.

1.1.3 Definition of Part Operating Temperature Grade

The part operating temperature grades are defined below:

Grade 1: -40°C to +125°C ambient operating temperature range
Grade 2: -40°C to +105°C ambient operating temperature range
Grade 3: -40°C to +85°C ambient operating temperature range
Grade 4: 0°C to +70°C ambient operating temperature range

DaimlerChrysler	date	Delphi Delco Electronics Systems	date	Visteon Corporation	date
Peter Voetsch	1/15/01	Gerald E. Servais	1/09/01	William Giffen	1/19/01

1.1. 4 Approval for Use in an Application

"Approval" is defined as user approval for use of a part in their application. The user's method of approval is beyond the scope of this document.

1.2 Reference Documents

Current revision of the referenced documents will be in effect at the date of agreement to the qualification plan. Subsequent qualification plans will automatically use updated revisions of these referenced documents
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1.2.1 Military

1. MIL-STD-883 Test Methods and Procedures for Microelectronics

1.2.2 Industrial

1. JEDEC JESD-22 Reliability Test Methods for Packaged Devices
2. EIA/JESD78 IC Latch-Up Test
3. UL-STD-94 Tests for Flammability of Plastic materials for parts in Devices and Appliances
4. AEC-Q001 Guidelines For Part Average Testing
5. EIA/JESD46-A Guidelines for User Notification of Product/Process Changes by Semiconductor Suppliers
6. J-STD-020 Moisture/Reflow Sensitivity Classification for Plastic Integrated Circuit Surface Mount Devices

2. GENERAL REQUIREMENTS

2.1 Objective

The objective of this specification is to establish a standard that defines operating temperature grades for integrated circuits based on a minimum set of qualification requirements.

2.2 Precedence of Requirements

In the event of conflict in the requirements of this standard and those of any other documents, the following order of precedence applies:

1 . The purchase order
2. The individual device specification
3. This document
4. The reference documents in Section 1.2 of this document
5 . The supplier's data sheet

For the device to be considered a qualified part per this specification, the purchase order and/or the individual device specification can not waive or detract from the requirements of this document.

2.3 Use of Generic Data to Satisfy Qualification and Requalification Requirements

2.3.1 Definition of Generic Data

The use of generic data to simplify the qualification process is strongly encouraged. Generic data can be submitted to the user as soon as it becomes available to determine the need for any additional testing. To be considered, the generic data must be based on a matrix of specific requirements associated with each characteristic of the device and manufacturing process as shown in Table 4 and Appendix 1**. If the generic data contains any failures, the data is not usable as generic data unless the supplier has documented and implemented corrective action or containment for the failure condition that is acceptable to the user.**

Appendix 1 defines the criteria by which components are grouped into a qualification family for the purpose of considering the data from all family members to be equal and generically acceptable to the qualification of the device in question. For each stress test, two or more qualification families can be combined if the reasoning is technically sound (i.e., supported by data). Table 1 provides guidelines showing how the available part test data may be applied to reducing the number of lots required for qualification.

With proper attention to these qualification family guidelines, information applicable to other devices in the family can be accumulated. This information can be used to demonstrate generic reliability of a device family and minimize the need for device-specific qualification test programs. This can be achieved through qualification and monitoring of the most complex (e.g. more memory,

Table 1 Part Qualification/Requalification Lot Requirements

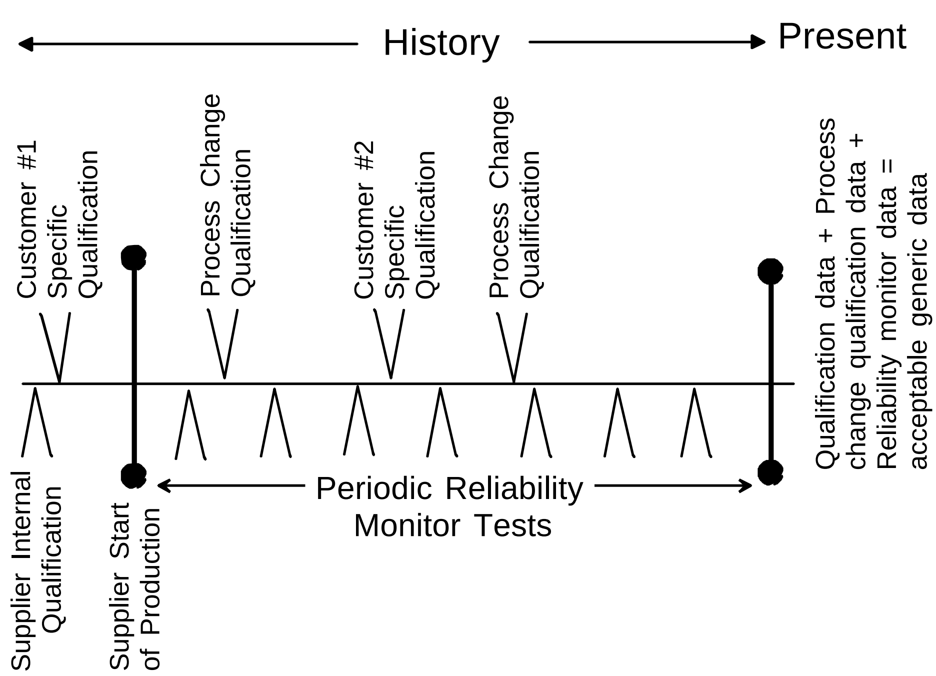
Part Information	Lot Requirements for Qualification
New device, no applicable generic data.	Lot and sample size requirements per Table 2
A part in a family is qualified. The part to be qualified is less complex and meets the Family Qualification Definition per Appendix 1.	Only device specific tests as defined in 4.2 are required. Lot and sample size requirements per Table 2 for the required tests.
A new part that has some applicable generic data.	Review Table 4 to determine required tests from Table 2. Lot and sample sizes per Table 2 for the required tests.
Part process change.	Review Table 4 to determine which tests from Table 2 are required. Lot and sample sizes per Table 2 for the required tests.
Part was environmentally tested to all the test extremes, but was end point electrically tested at a temperature less than the Grade required.	The endpoint electrical testing on at least 1 lot (that completed qualification testing) must meet or exceed the temperature extremes for the device Grade required. Sample sizes shall be per Table 2.
Qualification/Requalification involving multiple sites.	Refer to Appendix 1 paragraph 3.
Qualification/Requalification involving multiple families.	Refer to Appendix 1 paragraph 3.

A/D, larger die size) device in the qualification family and applying this data to less complex devices that subsequently join this family. Sources of generic data should come from supplier-certified test labs, and can include internal supplier's qualifications, cell structure/standard circuit characterization and testing, user-specific qualifications and supplier's in-process monitors. The generic data to be submitted must meet or exceed the test conditions specified in Table 3. Endpoint test temperatures must address the worst case temperature extremes for the device operating temperature grade being qualified on at least one lot of data. Failure to do so will result in the supplier testing 1 lot or, if there is no applicable or acceptable existing generic data, 3 lots for the stress test(s) in question on the device to be qualified. The user(s) will be the final authority on the acceptance of generic data in lieu of test data.

Table 4 defines a set of qualification tests that must be considered for any changes proposed for the component. The Table 4 matrix is the same for both new processes and requalification associated with a process change. This table is a superset of tests that the supplier and user should use as a baseline for discussion of tests that are required for the qualification in question. **It is the supplier's responsibility to present rationale for why any of the recommended tests need not be performed.**

2.3.2 Time Limit for Acceptance of Generic Data

There are no time limits for the acceptability of generic data as long as all reliability data taken since the initial qualification is submitted to the user for evaluation. This data must come from the specific part or a part in the same qualification family, as defined in Appendix 1. This data includes any customer specific data (if customer is non-AEC, withhold customer name), process change qualification and periodic reliability monitor data, see Figure 1.



Note: Some process changes (e.g., die shrink) will affect the use of generic data such that data obtained before these types of changes will not be acceptable for use as generic data,

Figure 1 Generic Data Time Line

2.4 Test Samples

2.4.1 Lot Requirements

Test samples shall consist of a representative device from the qualification family. Where multiple lot testing is required due to a lack of generic data, test samples as indicated in Table 2 must be composed of approximately equal numbers from three non-consecutive wafer lots, assembled in three non-consecutive molding lots. That is, they must be separated in the fab or assembly process line by at least one non-qualification lot.

2.4.2 Production Requirements

All qualification devices shall be produced on tooling and processes at the manufacturing site that will be used to support part deliveries at production volumes. Other electrical test sites may be used for electrical measurements after their electrical quality is validated.

2.4.3 Reusability of Test Samples

Devices that have been used for nondestructive qualification tests may be used to populate other qualification tests. Devices that have been used for destructive qualification tests may not be used any further except for engineering analysis.

2.4.4 Sample Size Requirements

Sample sizes used for qualification testing and/or generic data submission must be consistent with the specified minimum sample sizes and acceptance criteria in Table 2. Acceptance criteria for larger generic sample sizes can be calculated using the method in section 2.6.

If the supplier elects to use generic data for qualification, the specific test conditions and results must be recorded and available to the user. Existing applicable generic data should first be used to satisfy these requirements and those of section 2.3 for each test requirement in Table 2. Device specific qualification testing should be performed if the generic data does not satisfy these requirements.

2.4.5 Pre- and Post-stress Test Requirements

Endpoint test temperatures (room, hot and/or cold) are specified in the "Additional Requirements" column of Table 3 for each test. The specific value of temperature must address the worst case operating temperature grade extremes on at least one lot of data (generic or device specific) submitted per test. For example, if a supplier designs a device intended solely for use in an operating temperature Grade 3 environment (e.g. - 40°C to + 85°C), the endpoint test temperature extremes need only address those application limits. Qualification to applications in higher operating temperature grade environments (e.g. - 40°C to + 125°C for Grade 1) will require testing of at least one lot using these additional endpoint test temperature extremes.

2.5 Definition of Test Failure After Stressing

Test failures are defined as those devices not meeting the individual device specification, criteria specific to the test, or the supplier's data sheet, in the order of significance as defined in section 2.2. Any device that shows external physical damage attributable to the environmental test is also considered a failed device. If the cause of failure is agreed (by the manufacturer and the user) to be due to mishandling or ESD, the failure shall be discounted, but reported as part of the data submission.

2.6 Criteria for Passing Qualification

Passing all appropriate qualification tests specified in Tables 1 and 2, either by performing the test (acceptance of zero failures using the specified minimum sample size) or demonstrating acceptable generic data (using an equivalent total percent defective at a 90% confidence limit for the total required lot and sample size), qualifies the device per this document. If the qualification tests have failures, the device or qualification family may be granted "qualification status" only if corrective action or proper containment is demonstrated and approved by the user. **If the generic data contains any failures, the data is not usable as generic data unless the supplier has documented and implemented corrective action or containment for the failure condition that is acceptable to the user.**

Any unique qualification tests or conditions requested by the user and not specified in this document shall be negotiated between the supplier and user requesting the test.

When submitting monitor or qualification test data from generic products to satisfy the qualification requirements of this document, the number of samples and the total number of defective devices occurring during those tests must satisfy the following mathematical test:

$$\frac{\mathrm{Chi}^2}{ss_{gen}} \le \frac{4.61}{(ss \times \#\,lots)_{T1}}$$

Where: $ss_{gen} \ge (ss \times \#\,lots)_{T1}$ and $\#\,lots_{gen} \ge \#\,lots_{T1}$

Chi^2 is the chi-square goodness-of-fit test statistic at a 90% level of confidence (a = 0.90). A partial table of values is included below in Table A. The number of degrees of freedom is D.F. = 2(c + 1), where c is the number of failures contained in ss_{gen}.

ss is the total number of samples in the generic sampling base (ss_{gen}) or from the requirement in Table 2 ($(ss \times \#\,lots)_{T1}$) for the stress test in question.

TABLE A - Chi^2 @ 90% CONFIDENCE LEVEL

c	Chi^2	c	Chi^2	c	Chi^2	c	Chi^2
0	4.61	5	18.5	10	30.8	15	42.6
1	7.78	6	21.1	11	33.2	16	44.9
2	10.6	7	23.5	12	35.6	17	47.2
3	13.4	8	26.0	13	37.9	18	49.5
4	16.0	9	28.4	14	40.3	19	51.8

For example, if a supplier had data from 700 samples of temperature cycling, the maximum number of failures that this sampling would allow for the device in question to be considered qualified for this test requirement is:

$$Chi^2 \leq \frac{(700)(4.61)}{(3)(77)} = 13.97 \quad \text{and } c \leq 3 \text{ failures from Table A.}$$

If the qualification test needs to be performed, use the accept on zero criteria in the table above with the appropriate sample size. If there is applicable generic data as defined in Section 2.3, acceptance will be based on the Chi-square test statistic. This will be applied to the total percent defective of the data that meet or exceed the equivalent specified in this document for accept on zero at the specified sample size.

3. QUALIFICATION AND REQUALIFICATION

3.1 Qualification of a New Device

The stress test requirements for qualification of a new device are shown in Figures 2, 3, and 4 and are listed in Table 2, with the corresponding test conditions defined in Table 3. For each qualification, the supplier must have data available for all of these tests, whether it is stress test results on the device to be qualified or acceptable generic data. A review shall also be made of other devices in the same generic family to ensure that there are no common failure mechanisms in that family. Justification for the use of generic data, whenever it is used, must be demonstrated by the supplier and approved by the user.

For each device qualification, the supplier must have available a Certificate of Design, Construction and Stress Test Qualification data (see Appendix 2) and data indicating the level of fault grading of the software used for qualification (when applicable to the device type) per Q100-007 that will be made available to the customer upon request.

3.2 Requalification of a Changed Device

Requalification of a device is required when the supplier makes a change to the product and/or process that impacts the form, fit, function, quality and/or reliability of the device (see Table 4 for guidelines).

3.2.1 Process Change Notification

The supplier will meet the requirements of JEDEC Std No. 46 “Guidelines for User Notification of Product/Process Changes by Semiconductor Suppliers” for product/process changes.

3.2.2 Changes Requiring Requalification

As a minimum, any change to the product, as defined in Appendix 1, requires performing the applicable tests listed in Tables 2 and 3, using Table 4 to determine the requalification test plan. Table 4 should be used as a guide for determining which tests are applicable to the qualification of a particular part change or whether equivalent generic data can be submitted for that test(s).

3.2.3 Criteria for Passing Requalification

All requalification failures shall be analyzed for root cause, and corrective and preventive actions established as required. **The device or qualification family may be granted "qualification status" if, as a minimum, proper containment is demonstrated and approved by the user.**

3.2.4 User Approval

A change may not affect a device's operating temperature grade, but may affect it's performance in an application. Individual user authorization of a process change will be required for that user's particular application(s), and this method of authorization is outside the scope of this document.

4 QUALIFICATION TESTS

4.1 General Tests

Test flows are shown in figures 2, 3, and 4 and test details are given in Tables 2 and 3. Not all tests apply to all devices. For example, certain tests apply only to ceramic packaged devices, others apply only to devices with E^2PROM memory, and so on. The applicable tests for the particular device type are indicated in the "Note" column of Table 2 and the "Additional Requirements" Column of Table 3. The "Additional Requirements" column of Table 3 also serves to highlight test requirements that supersede those described in the referenced test method.

4.2 Device Specific Tests

The following tests must be performed on the specific device to be qualified for all hermetic and plastic packaged devices. Generic data is not allowed for these tests. Device specific data, if it already exists, is acceptable.

1. Electrostatic Discharge (ESD) - Testing shall be done at all voltages and polarities until there is confidence that a family pin/ESD circuit combination (with the same layout) has no sensitivity window. Then the device may be tested only at the specification maximum voltage.

2. Latch-up (LU) - All product.

3. Electrical Distribution - The supplier must demonstrate, over the operating temperature grade, voltage and frequency ranges, that the device is capable of meeting the parametric limits of the device specification. This data must be taken from at least three lots, or one matrixed (or skewed) process lot, and must represent enough samples to be statistically valid, see Q100-009. It is strongly recommended that the final test limits be established using AEC-Q001 Guidelines For Part Average Testing.

4 Other Tests - A user may require other tests in lieu of generic data based on his experience with a particular supplier.

4.3 Wearout Reliability Tests

Testing for the failure mechanisms listed below must be available to the user whenever a new technology or material relevant to the appropriate wearout failure mechanism is to be qualified.

The data, test method, calculations and internal criteria need not be demonstrated or performed on the qualification of every new device, but should be available to the user upon request.

- Electromigration
- Time-Dependent Dielectric Breakdown - for all MOS technologies.
- Hot Carrier Injection - for all MOS technologies below 1 micron.

Qualification Test Flow For Electrical Tests

Note: See Tables 2 & 3 for details of test methods.

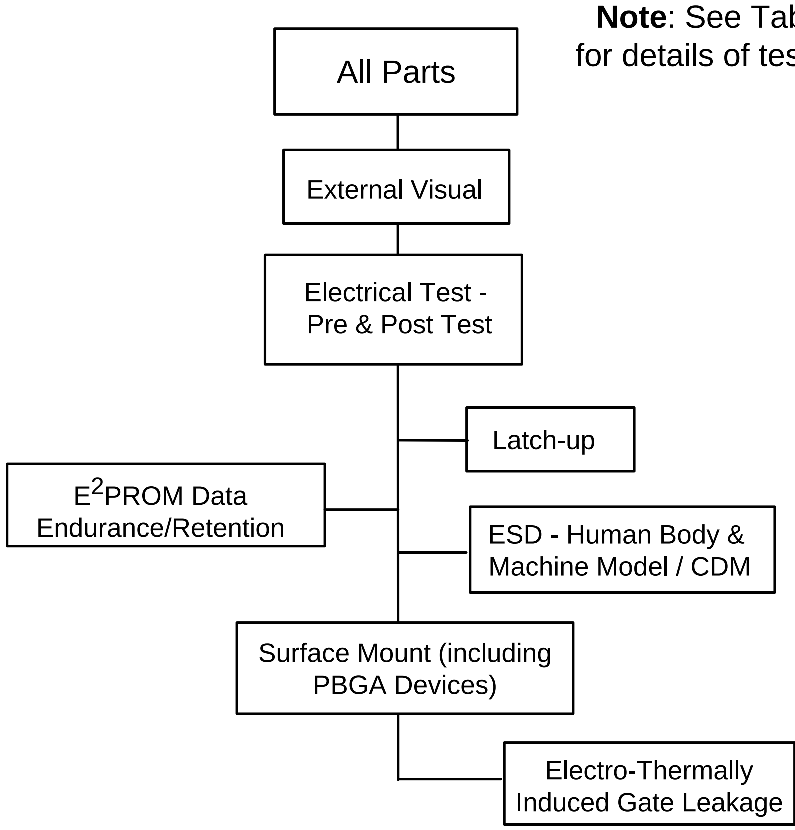


Figure 2 Qualification Test Flow for Electrical Testing

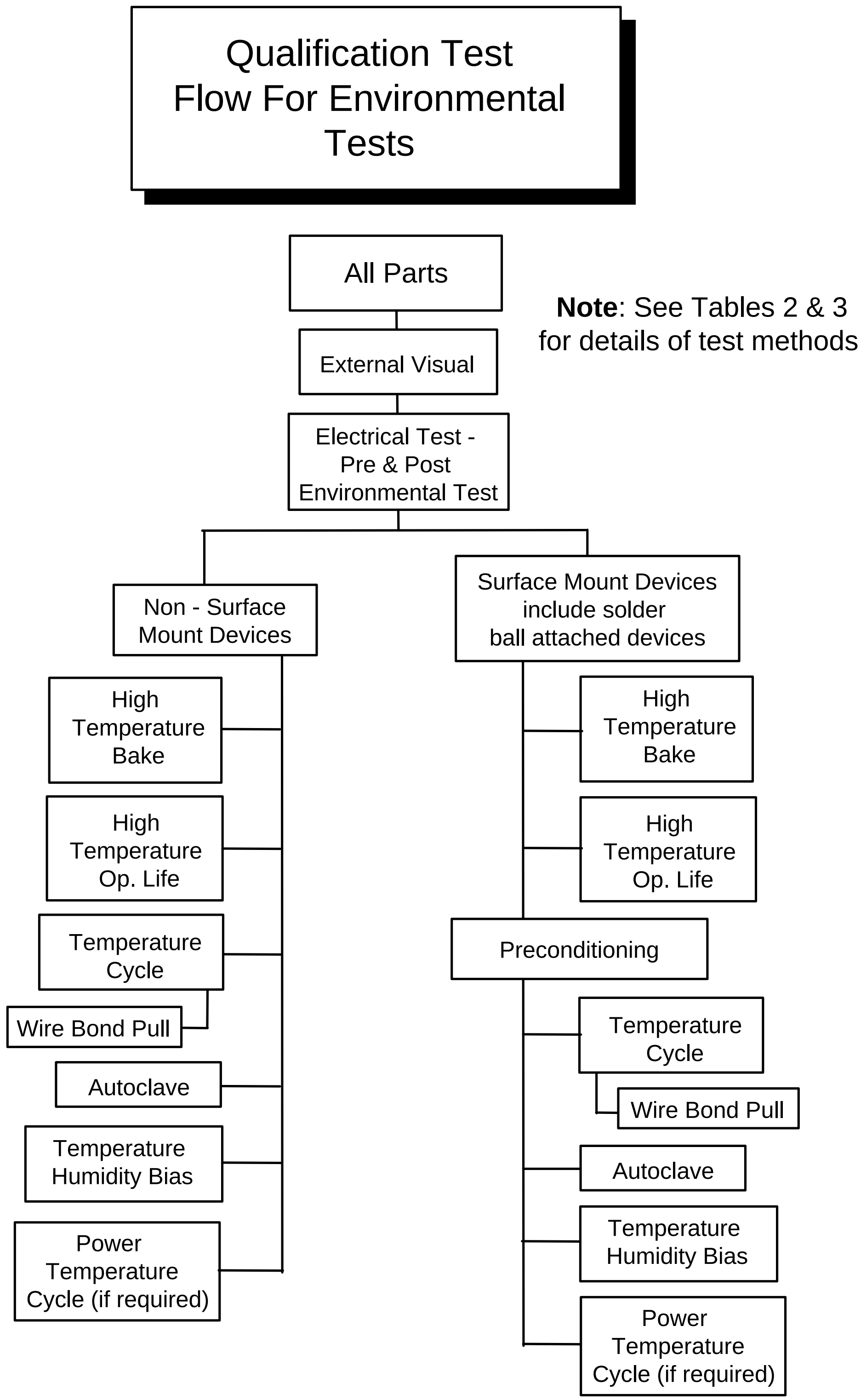
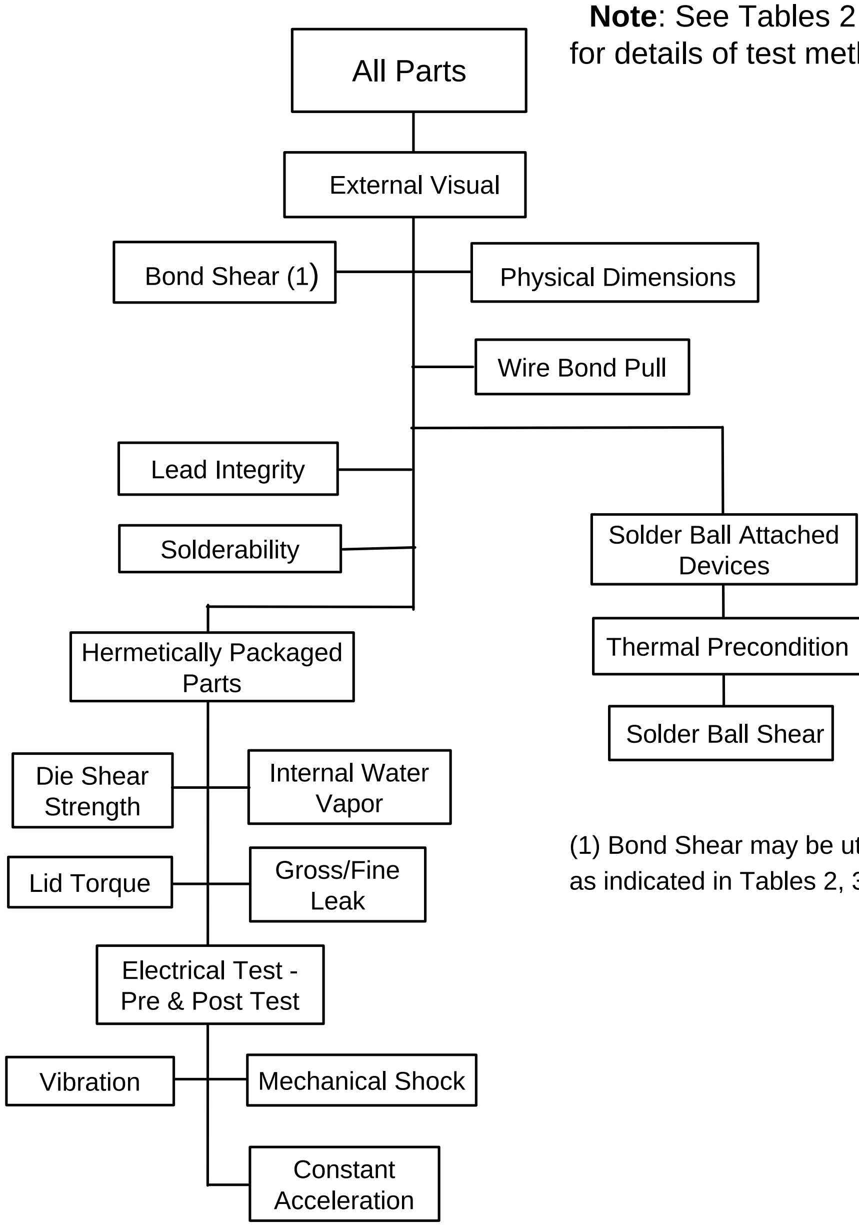


Figure 3 Qualification Test Flow for Environmental Tests

Qualification Test Flow Mechanical Qualification Tests

Note: See Tables 2 & 3 for details of test methods.



(1) Bond Shear may be utilized as indicated in Tables 2, 3, & 4.

Figure 4 Qualification Test Flow for Mechanical Tests

TABLE 2 - QUALIFICATION TEST DEFINITIONS						
Stress	**Abr.**	**#**	**Notes**	**Sample Size per Lot**	**Number of lots**	**Accept on # failed**
Pre- and Post-Stress Electrical Test – test software used shall meet the requirements of Q100-007.	TST	1	H, P, B, N, G	Qualification devices tested per the requirements of the appropriate test(s)		0
High Temperature Operating Life	HTOL	2	H, P, B, D, G	77	3 - see note**	0
High Temperature Bake	HTB	3	H, P, B, D, G	77	1 - see note**	0
Preconditioning	PC	4	P, B, S, N, G	All surface-mount qualification devices to be subjected to THB, TC, and AC		0
Temperature Humidity Bias <u>or</u> HAST	THB or HAST	5	P, B, D, G	77	3 - see note**	0
Autoclave or Unbiased HAST	AC or UHST	6	P, B, D, G	77	3 - see note**	0
Temperature Cycling	TC	7	H, P, B, D, G	77	3 - see note**	0
Power Temperature Cycling	PTC	8	H, P, B, D, G	77	1	0
Mechanical Shock	MS	9	H, D, G	39	3 - see note**	0
Vibration Variable Frequency	VVF	10	H, D, G	Performed as a sequential test for mechanical integrity of hermetic packaged devices		
Constant Acceleration	CA	11	H, D, G			
Gross/Fine Leak	GFL	12	H, D, G			
External Visual	EV	13	H, P, N, G, B	All qualification Devices submitted for testing		0
Physical Dimensions	PD	14	H, P, B, D, G	30	1	$P_{pk} \geq 1.66$ or $C_{pk} \geq 1.33$
Lead Integrity	LI	15	H, P, D, G	45 leads from a min. of 5 devices	1	0
Lid Torque	LT	16	H, D, G	5	1	0
Wire Bond Pull Strength	BPS	17	H, P, B, D, G	30 bonds from a min. of 5 devices	1	0 and $P_{pk} \geq$ 1.66 or $C_{pk} \geq 1.33$

TABLE 2 - QUALIFICATION TEST DEFINITIONS

Stress	Abr.	#	Notes	Sample Size per Lot	Number of lots	Accept on # failed
Bond Shear (see Appendix 3)	BS	18	H, P, B, D, G	30 bonds from a min. of 5 devices	1	0 and $P_{pk} \geq$ 1.66 or $C_{pk} \geq$ 1.33
Solder Ball Shear	SBS	19	B	5 balls from a min. of 10 devices	3 – see note **	0
Die Shear Strength	DSS	20	H, D, G	5	1	0
Electrostatic Discharge	ESD	21	H, P, B, D	min. 3/V level/ model	1	0
Latch-up	LU	22	H, P, B, D	6	1	0
Internal Water Vapor	IWV	23	H, D, G	3	1	0
Solderability	SD	24	H, P, B, D, G	15	3 - see note**	0
E^2PROM Data Endurance/ Retention Test	ET	25	H, P, B ,D, G	77	1	0
Early Life Failure Rate	ELFR	26	H, P, B, N G	800	3 - see note**	0
Gate Leakage	GL	27	D, P, B, G, S	6	1	0
Electrical Distributions	ED	28	H, P, B, D	30	3	$P_{pk} \geq$ 1.66

TABLE 3 – TABLE OF METHODS REFERENCED

Stress	Abr.	#	Reference	Additional Requirements*
Pre- and Post-Stress Electrical Test	TST	1	User or Supplier specification	Test is performed as specified in the applicable stress reference and the additional requirements in Table 3. Test software used shall meet the requirements of Q100-007.
High Temperature Operating Life	HTOL	2	JA108	150°C T_a for 408 hours or 125°C T_a for 1000 hours. (junction temperature not to exceed 175°C) at V_{cc} (max) at which dc and ac parametrics are guaranteed. Static or dynamic bias (per engineering spec). Thermal shut-down shall not occur during this test. Tri-temp TST before and after HTOL.

TABLE 3 – TABLE OF METHODS REFERENCED				
Stress	**Abr.**	**#**	**Reference**	**Additional Requirements***
High Temperature Bake	HTB	3	JA103	150^oC/1000 hours or 175^oC/500 hours for plastic. 250^oC/10 hours or 200^oC/72 hours for ceramic packaged devices. TST before and after at room and hot temperatures.
Preconditioning	PC	4	J-STD-020 & JA113	Performed on surface mount devices only. PC performed before THB, AC, and TC stresses. It is recommended that J-STD-020 be performed to determine at what preconditioning level to perform in the actual preconditioning stress per JA113. The minimum acceptable level for qualification is level 3 per JA113. Delamination from the die surface in JA113/J-STD-020 is acceptable if the device passes the subsequent Qualification tests. Any replacement of devices must be reported. TST before and after at room temperatures.
Temperature Humidity Bias or HAST	THB or HAST	5	J A101 or JA110	For surface mount devices, PC before THB, 85^oC/85%RH/1000 hours or HAST 130^oC/85%RH**/**96 hours. TST before and after THB or HAST at room and hot temperatures.
Autoclave or Unbiased HAST	AC or UHST	6	JA102 or JA118	For surface mount devices, PC before AC, 121^oC/15 psig/96 hours or unbiased HAST at 130°C/85%RH/ 96 hours. TST before and after AC or UHST at room temperature.
Temperature Cycling	TC	7	JA104 (see Appendix 3 for package opening procedure)	PC before TC for surface mount devices, condition C (-65^oC to 150^oC) for 500 cycles or (-50^oC to 150^oC) for 1000 cycles. TST before and after TC at hot temperature. Three gram-force bond pull strength (BPS) after decap on five devices from one lot on corner bonds (2 bonds per corner), and one mid-bond per side ***on each device***.
Power Temperature Cycling	PTC	8	JA105	Test is performed only on devices with maximum rated power $\geq$ 1 watt or $\Delta T_j \geq 40^oC$ or devices designed to drive inductive loads. -40^oC to $+125^oC$ for 1000 cycles, thermal shut-down shall not occur during this test. TST before and after PTC at room and hot temperatures.
Mechanical Shock	MS	9	M2002	Y1 plane only, 5 pulses, 0.5 msec duration, 1500 g peak acceleration. TST after CA.
Vibration Variable Frequency	VVF	10	M2007	20 Hz to 2 KHz to 20 Hz (logarithmic variation) in >4 minutes, 4X in each orientation, 50 g peak acceleration. TST after CA.
Constant Acceleration	CA	11	M2001	Y1 plane only, 30 K g-force for <40 pin packages, 20 K g-force for 40 pins and greater. TST at room temperature.
Gross/Fine Leak	GFL	12	M1014	Any single-specified fine test followed by any single-specified gross test.
External Visual	EV	13	JB101	

TABLE 3 – TABLE OF METHODS REFERENCED

Stress	Abr.	#	Reference	Additional Requirements*
Physical Dimensions	PD	14	JB100	See applicable JEDEC standard outline and individual device spec for significant dimensions and tolerances.
Lead Integrity	LI	15	JB105	Not required for surface mount devices
Lid Torque	LT	16	M2024	
Wire Bond Pull Strength	BPS	17	M2011	Condition C or D, min. pull strength after temperature cycling = 3 grams.
Bond Shear	BS	18	AEC-Q100-001	See Appendix 3 procedure for details on the acceptance criteria and how to perform the test.
Solder Ball Shear	SBS	19	AEC-Q100-010	PC Thermally (two 220°C reflow cycles) before integrity (mechanical) testing.
Die Shear Strength	DSS	20	M2019	For ceramic devices only.
Electrostatic Discharge	ESD	21	AEC-Q100-002, AEC - Q100-003, & Q100-011	See attached procedure for details on how to perform the test. TST before and after ESD at room and hot temperatures. It is anticipated that a future revision of Q100 will adopt Q100-011 Field Induced Charged Device Model (FCDM) as a replacement for Q100-003 Machine Model (MM) ESD. Suppliers capable of performing Q100-011 FCDM may adopt this change now.
Latch-up	LU	22	AEC-Q100-004	See attached procedure for details on how to perform the test. TST after LU at room and hot temperatures.
Internal Water Vapor	IWV	23	M1018	
Solderability	SD	24	JB102	If burn-in screening is normally performed on the device before shipment, samples for SD must first undergo burn-in. Perform 8 hour steam aging prior to testing (1 hour for Au-plated leads).
E^2PROM Data: Endurance Test Retention Test	ET	25	AEC-Q100 - 005	For devices that contain E^2PROM only. TST before and after at room and hot temperatures. This test does not replace other stress test qualification requirements.
Early Life Failure Rate	ELFR	26	AEC-Q100 - 008	Devices that pass this stress can be used to populate other stress tests. Generic data is applicable. TST before and after ELFR at room and hot temperature.
Electro-Thermally Induced Gate leakage Test	GL	27	AEC-Q100-006	TST before and after at room temperature.
Electrical Distributions	ED	28	AEC-Q100-009	Supplier and user to mutually agree upon electrical parameters to be measured.

LEGEND FOR TABLES 1 AND 2

Notes:
- H Required for hermetic packaged devices only.
- P Required for plastic packaged devices only.
- B Required Solder Ball Surface Mount Packaged devices only.
- N Nondestructive test, devices can be used to populate other tests or they can be used for production.
- D Destructive test, devices are not to be reused for qualification or production.
- S Required for surface mount plastic packaged devices only.
- G Generic data allowed. See Section 2.3, Table 1, and Appendix 1.

Methods:
- M MIL-STD-883, the most current revision and notice.
- J JEDEC JESD-22, the most current method.
- # Reference Number for the particular test.

* All electrical testing before and after the qualification stresses are performed to the limits of the individual device specification in temperature and limit value.

** The number of lots required for qualification testing will depend on the amount and usefulness of generic data on the device or device family to be qualified, see section 2.3 and Appendix 1. In many cases use of generic data will result in only one lot being required for qualification.

TABLE 4 - Process Change Qualification Guidelines for the Selection of Tests

2. High Temperature Operating Life
3. High Temperature Bake
5. Temperature Humidity Bias or HAST
6. Autoclave or Unbiased HAST
7. Temperature Cycling
8. Power Temperature Cycle
9-12. Mechanical Sequence
13. External Visual
14. Physical Dimensions
15. Lead Integrity
16. Lid Torque
17. Bond Pull Strength
18. Ball Bond Shear
19. SBS (solder ball shear)
20. Die Shear
21. Electrostatic Discharge
22. Latch-up
23. Internal Water Vapor
24. Solderability
25. E^2PROM Testing
26. Early Life Failure Rate Induced Gate
27. Electro-Thermally Leakage gate leakage
28. Electrical Distribution

EM Electromigration
HCI Hot Carrier Injection
TDB Time Dependent Dielectric Breakdown

Note: A letter or "●" indicates that performance of that stress test should be considered for the appropriate process change

Test # From Table 3	2	3	5	6	7	8	9-12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28			
Process Attribute	HTOL	HTB	THB	AC	TC	PTC	MSQ	EV	PD	LI	LT	BPS	BS	SBS	DSS	ESD	LU	IWV	SD	ET	ELFR	GL	ED	EM	HCI	TDB
DESIGN																										
Active element Design	●			●	●	M										●	●			DJ	●	S	●	D	D	D
Circuit rerouting					A	M										●	●					S	●			
Wafer dimension	●				E	M						E	E			E	E				●		●			
WAFER FAB																										
Lithography	●		●		●	M						●	●								G		●			
Die Shrink	●		●	●		M										●	●			DJ	●	S	●	●	●	●
Diffusion/doping	●					M										●	●				G	S	●			
Polysilicon	●				●	M										●	●			DJ		S	●			
Metallization	●		●	●	●	M						●	●									S	●	●		
Passivation/oxide	●		K	K	●	M						●	K			●	●			DJ	GN	PS	●		●	●
Backside operation	●				●	M	H								H	M	●									
FAB site transfer	●		●	●	●	M	H					●	●		H	●	●			J	●	S	●	●	●	●
ASSEMBLY																										
Die overcoat	●	●	●	●	●	M												H				S				
Leadframe Plating		●	●	●	●	M		●		●		C			H				●							
Bump Metal System	●	●	●	●	●	M		●	●					●												
Leadframe material		●		●	●	M	H	●	●	●		●			H				●							
Leadframe dimension				●	●	M	H	●	●	●									●							
Wire bonding		●		●	●	Q	H					●	●										M			
Die scribe/separate			●	●	●	M																				
Die prep clean	●		●	●		M						●	●		H											
Package marking								●											B							
Die attach	●		●	●	●	M	H								H			H					●			
Molding compound	●	●	●	●	●	M		●	●	●									●		●	S				
Molding process	●	●	●	●	●	M		●	●	●									●			S				
Hermetic sealing		H		H	H		H	H	H	H	H							H								
New package	●	●	●	●	●	M	H	●	●	●		●	●	T	H	●		H	●		●	S	●			
Ass'y site transfer	●		●	●	●	M	H	●	●	●		●	●	T	H			H	●		●	S	●			

A Only for peripheral routing
B For Symbol rework, new cure t,T
C If bond to leadfinger
D Design rule change
S Required for surface mounted plastic packaged devices only.

E Thickness only
G Only from non-100% burned-in parts
H Hermetic only
J E or E^2PROM
Q Wire diameter decrease

K Passivation only
M For devices requiring PTC
N Passivation and gate oxide
P Passivation and Interlevel dielectric
T Only for Solder Ball Surface Mounted Packages

APPENDIX 1 - Definition of a Qualification Family

The qualification of a particular process will be defined within, but not limited to, the categories listed below. The supplier will provide a complete description of each process and material of significance. There must be valid and obvious links between the data and the subject of qualification.

For devices to be categorized in a qualification family, they all must share the same major process and materials elements as defined below. All devices using the same process and materials are to be categorized in the same qualification family for that process and are qualified by association when one family member successfully completes qualification with the exception of the device specific requirements of section 4.2.

Prior qualification data obtained from a device in a specific family may be extended to the qualification of subsequent devices in that family.

For broad changes that involve multiple attributes (e.g. site, material(s), process(es)), refer to section 3 of this appendix and section 2.3 of Q100, which allows for the selection of worst-case test vehicles to cover all the possible permutations.

1. Fab Process

Each process technology (e.g., CMOS, NMOS, Bipolar, etc.) must be considered and qualified separately. No matter how similar, processes from one fundamental fab technology cannot be used for another. For BiCMOS devices, data must be taken from the appropriate technology based on the circuit under consideration.

Family requalification with the appropriate tests is required when the process or a material is changed (see Table 4 for guidelines). The important attributes defining a qualification family are listed below:

1) **Wafer Fab Technology** (e.g., CMOS, NMOS, Bipolar, etc.)

2) **Wafer Fab Process** - consisting of the same attributes listed below:
   - Circuit element feature size (e.g., layout design rules, die shrinks, contacts, gates, isolations)
   - Substrate (e.g. orientation, doping, epi, wafer size)
   - Number of masks (supplier must show justification for waiving this requirement)
   - Lithographic process (e.g. contact vs. projection, E-beam vs. X-ray, photoresist polarity)
   - Doping process (e.g. diffusion vs. ion implantation)
   - Gate structure, material and process (e.g. polysilicon, metal, salicide, wet vs. dry etch)
   - Polysilicon material, thickness range and number of levels
   - Oxidation process and thickness range (for gate and field oxides)
   - Interlayer dielectric material and thickness range
   - Metallization material, thickness range and number of levels
   - Passivation material and thickness range
   - Die backside preparation process and metallization

3) **Wafer Fab Site**

2. Assembly Process - Plastic or Ceramic

The processes for plastic and ceramic package technologies must be considered and qualified separately. For devices to be categorized in a qualification family, they all must share the same major process and material elements as defined below. Family requalification with the appropriate tests are required when the process or a material is changed. The supplier must submit technical justification to the user to support the acceptance of generic data with pin (ball) counts, die sizes, substrate dimensions / material / thickness, paddle sizes and die aspect ratios different than the device to be qualified.

The important attributes defining a qualification family are listed below:

1) **Package Type** (e.g. DIP, SOIC, PLCC, QFP, PGA, PBGA)
   - Same cross-sectional dimensions (width x height).
   - Range of paddle (flag) size (maximum and minimum dimensions) qualified for the die size/ aspect ratio under consideration.
   - Substrate base material (e.g., PBGA)

2) **Assembly Process** - consisting of the same attributes listed below:
   - Leadframe base material
   - Leadframe plating (internal and external to the package)
   - Die attach material
   - Wire bond material, wire diameter, and process
   - Plastic mold compound, organic substrate material or ceramic package material
   - Solder Ball metallization system (if applicable)
   - Heatsink type, material, dimensions

3) **Assembly Site**

3. Qualification of Multiple Sites and Families

Multiple Sites

When the specific product or process attribute to be qualified or requalified will affect more than one wafer fab site or assembly site, a minimum of one lot of testing per affected site is required.

Multiple Families

When the specific product or process attribute to be qualified or requalified will affect more than one wafer fab family or assembly family, the qualification test vehicles should be: 1) One lot of a single device type from each of the families that are projected to be most sensitive to the changed attribute, or 2) Three lots total (from any combination of acceptable generic data and stress test data) from the most sensitive families if only one or two families exist.

Below is the recommended process for qualifying changes across many process and product families:

1) Identify all products affected by the proposed process changes.

2) Identify the critical structures and interfaces potentially affected by the proposed process change.

3) Identify and list the potential failure mechanisms and associated failure modes for the critical structures and interfaces (see the example in Table 4). Note that steps 1 to 3 are equivalent to the creation of an FMEA.

4) Define the product groupings or families based upon similar characteristics as they relate to the structures and device sensitivities to be evaluated, and provide technical justification for these groupings.

5) Provide the qualification test plan, including a description of the change, the matrix of tests and the representative products, that will address each of the potential failure mechanisms and associated failure modes.

6) Robust process capability must be demonstrated at each site (e.g. control of each process step, capability of each piece of equipment involved in the process, equivalence of the process step-by-step across all affected sites) for each of the affected process step(s).

Table 4 - Example of Failure Mode/Mechanism List for a Passivation Change

Critical Structure or Interface:	Potential Failure Mechanism	Associated Failure Modes	On These Products
Passivation to Mold Compound interface	Passivation Cracking - Corrosion	Functional Failures	All Die
	Mold Compound-Passivation Delamination	Corner Wire Bond Failures	Large Die
Passivation to Metallization interface	Stress-induced Voiding	Functional Failures	Die with Minimum Width Metal Lines
	Ionic Contamination	Leakage, Parametric Shifts	All Die
Polysilicon and Active Resistors	Piezoelectric Leakage	Parametric Shifts (Resistance, Gain, Offset)	Analog products

APPENDIX 2 - Certification of Design, Construction and Qualification

The following information, as applicable, is required to identify a component that has met the requirements to be classified as a operating temperature Grade 1 - 4 integrated circuit.

1. User(s) part number, where applicable.
2. Supplier part number and data sheet.
3. Location of die fabrication facility and process identifier.
4. Location of assembly facility and process identifier.
5. Location of final quality control (test) facility.
6. Die family number, if applicable.
7. Die technology description (channel/gate length, process technology, supplier process ID, number of transistors and/or gates and number of mask steps)
8. Die dimensions (width, length, thickness) in mils.
9. Die metallization material and number of layers.
10. Die passivation and/or coating, and thickness range.
11. Pictorial cross-section of the basic device structure (transistor with gates and contacts) detailing all nominal dimensions and material compositions (each level of die metallization and interlayer dielectric, barrier metals, gate and field oxides).
12. Die backside preparation method and metallization.
13. Die separation method (% sawed through).
14. Die attach material (supplier ID) and method.
15. Type and pin (ball) count of package, and differences of package to the individual device specification, if any.
16. Ceramic package material or plastic mold compound (supplier ID) and flammability rating. Must meet UL-94 V1 or better for flammability.
17. Bond wire material(s) and diameter(s).
18. Wire bonding diagram and bonding process identifiers.
19. Type of wire bond at the die and leadframe or post.
20. Leadframe (die paddle, bonding fingers and external leads) material, dimensions and plating material and thickness.
21. Barrier material used between solder ball and substrate (e.g., PBGA)
22. Header material, if applicable.
23. Measured or derived values of θ_{ja} .
24. Test circuits, bias(es) and operational conditions imposed during the supplier's life and environmental tests.
25. Fault grade percentage of final test program, per Q100-007. (for digital ICs and digital section of BICMOS.
26. Substrate material, thickness, and size (e.g.,PBGA)
27. Heatsink dimensions and material

APPENDIX 3 - Plastic Package Opening For Wire Bond Testing

1.0 Purpose

The purpose of this Appendix is to define a guideline for opening plastic packaged devices so that reliable wire pull or bond shear results will be obtained. This method is intended for use in opening plastic packaged devices to perform wire pull testing after temperature cycle testing or for bond shear testing.

2.0 Materials and Equipment

2.1 Etchants

Various chemical strippers and acids may be used to open the package dependent on your experience with these materials in removing plastic molding compounds. Red Fuming Nitric Acid has demonstrated that it can perform this function very well on novolac type epoxies, but other materials may be utilized if they have shown a low probability for damaging the bond pad material.

2.2 Plasma Strippers

Various suitable plasma stripping equipment can be utilized to remove the plastic package material.

3.0 Procedure

Using a suitable end mill type tool or dental drill, create a small impression just a little larger than the chip in the top of the plastic package. The depth of the impression should be as deep as practical without damaging the loop in the bond wires.

Using a suitable chemical etchant or plasma etcher, remove the plastic material from the surface of the die, exposing the die bond pad, the loop in the bond wire, and at least 75% of the bond wire length. Do not expose the wire bond at the lead frame (these bonds are frequently made to a silver plated area and many chemical etchants will quickly degrade this bond making wire pull testing impossible).

Using suitable magnification, inspect the bond pad areas on the chip to determine if the package removal process has significantly attacked the bond pad metallization. If a bond pad shows areas of missing metallization, the pad has been degraded and shall not be used for bond shear or wire pull testing. Bond pads that do not show attack can be used for wire bond testing.

Revision History

Rev#	Date of change	Brief summary listing affected paragraphs
-	June 9, 1994	Initial Release.
A	May 19, 1995	Added copyright statement, Revised sections 2.3, 2.4.1, 2.4.4, 2.4.5, 2.8, 3.2 and 4.2, Table 2, 3, 4 and Appendix 1, 2, and Added Appendix 3.
B	Sept. 6, 1996	Revised 1.1, 1.2.3, 2.3, 3.1, 3.2.1, Table 2, 3, 4 and Appendix 2.
C	Oct. 8 , 1998	Revised 1.1,1.1.3, 1.2.2, 2.2, 2.3, 2.4.2, 2.4.5, 2.6, 3.1, 3.2.1, 3.2.3, 2.3.4, 4.1, 4.2, Table 3, Table 4, Appendix 2, Appendix 3. Added 1.1.1, Figures 1, 2, & 3, Test Methods Q100-008 & -009. Deleted 2.7, & 2.8.
D	Aug. 25, 2000	Revised 1.1, 2.3, Figure 2, Figure 3, Figure 4, Table 2, Table 3, Table 4, Appendix 1, Appendix 2. Added 2.3.2, test methods -010, and –011, Figure 1.
E	Jan. 31, 2001	Revised Figure 4.

ATTACHMENT 1

AEC - Q100-001 REV-C

WIRE BOND SHEAR TEST

Acknowledgment

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Council would especially like to recognize the following significant contributors to the development of this document:

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Automotive Electronics Council
Component Technical Committee

Change Notification

The following summary details the changes incorporated into AEC-Q100-001 Rev-C:

- **Section 1.3.4.4, Type 4 - Die Surface Contact: Corrected wording to reflect bond shear type where the shear tool contacts the die surface, rather than the bonding surface as stated in Rev - B.**
- **Added new Section 1.3.5, Footprint: Added new definition for "footprint"; changed numbers of subsequent sections to reflect the addition.**
- **Section 3.6 step b, Footprint Inspection of Aluminum Wedge/Stitch Bonds: Added wording to clarify method used to remove wire for footprint inspection.**
- **Figure 3, Wire Bond Shear Types: Updated figure to reflect wording correction made to Type 4 - Die Surface Contact.**
- **Minor wording changes were made to the following: Section 1.1, 1.3.1, 1.3.4.1, 1.3.4.5, 2.2, 2.5, 3.2, and 3.5.**

Automotive Electronics Council
Component Technical Committee

METHOD - 001

WIRE BOND SHEAR TEST

Text enhancements and differences made since the last revision of this document are shown as underlined areas. Several figures have also been revised, but changes to these areas have not been underlined.

1. SCOPE

1.1 Description

This test establishes a procedure for determining the strength of the interface between a gold ball bond and a package bonding surface, or an aluminum wedge/stitch bond and a package bonding surface, on either pre-encapsulation or post-encapsulation devices. This strength measurement is extremely important in determining two features:

1) the integrity of the metallurgical bond which has been formed.

2) the reliability of gold and aluminum wire bonds to die or package bonding surfaces.

This test method can be used only when the ball height and diameter for ball bonds, or the wire height (1.25 mils and larger at the compressed bond area) for wedge/stitch bonds, are large enough and adjacent interfering structures are far enough away to allow suitable placement and clearance (e.g., above the bonding surface and between adjacent bonds) when performing the wire bond shear test.

The wire bond shear test is destructive. It is appropriate for use in process development, process monitoring, and/or quality assurance.

1.2 Reference Documents

Not Applicable

1.3 Terms and Definitions

The terms and definitions shall be in accordance with the following sections.

1.3.1 Ball Bond

The welding of a thin wire, usually gold, to a die bonding surface, usually an aluminum alloy bond pad, using a thermal compression or thermosonic wire bonding process. The ball bond includes the enlarged spherical portion of the wire (sometimes referred to as the nail head and formed by the flame-off and first bonding operation in thermal compression and thermosonic process), the underlying bonding surface, and the intermetallic weld interface. For the purposes of this document, all references to ball bonds are applicable to gold ball bonds on die bonding surfaces; other ball bond material combinations may require a new set of failure criteria (see section 4.1).

Chrysler	Date	Delphi Delco Electronics Systems	Date	Visteon Automotive Systems	Date
[signature]	9/28/98	[signature]	10/1/98	[signature]	9/25/98
Richard A. Chow - Wah		Gerald E. Servais		Douglas Sendelbach	

1.3.2 Bonding Surface

Either 1) the die surface (e.g., die bond pad) or 2) the package bonding surface (e.g., plated leadframe post or finger, downbond to the flag or paddle, etc.) to which the wire is ball, wedge, or stitch bonded.

1.3.3 Bond Shear

A process in which an instrument uses a chisel shaped tool to shear or push a ball or wedge/stitch bond off the bonding surface (see Figure 1). The force required to cause this separation is recorded and is referred to as the bond shear strength. The bond shear strength of a gold ball bond, when correlated to the diameter of the ball bond, is an indicator of the quality of the metallurgical bond between the gold ball bond and the die bonding surface metallization. The bond shear strength of an aluminum wedge/stitch bond, when compared to the manufacturer's bond wire tensile strength, is an indicator of the integrity of the weld between the aluminum wire and the die or package bonding surface.

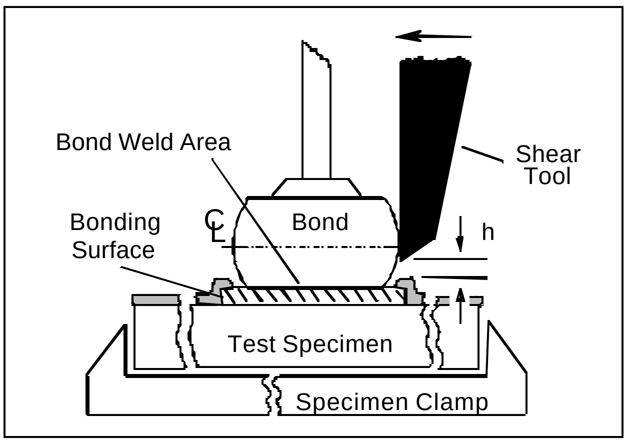


Figure 1: Bond Shear set-up

1.3.4 Definition of Bond Shear Types for Ball and Wedge/Stitch Bonds (see Figure 3)

1.3.4.1 Type 1 - Bond Lift

A separation of the entire wire bond from the bonding surface with only an imprint being left on the bonding surface. There is very little evidence of intermetallic formation or welding to the bonding surface metallization.

1.3.4.2 Type 2 - Bond Shear

A separation of the wire bond where: 1) A thin layer of bonding surface metallization remains with the wire bond and an impression is left in the bonding surface, or 2) Intermetallics remain on the bonding surface and with the wire bond, or 3) A major portion of the wire bond remains on the bonding surface.

1.3.4.3 Type 3 - Cratering

A condition under the bonding surface metallization in which the insulating layer (oxide or interlayer dielectric) and the bulk material (silicon) separate or chip out. Separation interfaces which show pits or depressions in the insulating layer (not extending into the bulk) are not considered craters. It should be noted that cratering can be caused by several factors including the wire bonding operation, the post-bonding processing, and even the act of wire bond shear testing itself. Cratering present prior to the shear test operation is unacceptable.

1.3.4.4 Type 4 - Die Surface Contact

The shear tool contacts the die surface and produces an invalid shear value. This condition may be due to improper placement of the specimen, a die surface not parallel to the shearing plane, a low shear height, or instrument malfunction. This bond shear type is not acceptable and shall be eliminated from the shear data.

1.3.4.5 Type 5 - Shearing Skip

The shear tool removes only the topmost portion of the ball or wedge/stitch bond. This condition may be due to improper placement of the specimen, a die surface not parallel to the shearing plane, a high shear height, or instrument malfunction. This bond shear type is not acceptable and shall be eliminated from the shear data.

1.3.4.6 Type 6 - Bonding Surface Lift

A separation between the bonding surface metallization and the underlying substrate or bulk material. There is evidence of bonding surface metallization remaining attached to the ball or wedge/stitch bond.

1.3.5 Footprint

An impression of the compressed wedge/stitch bond area created in the bonding surface during the ultrasonic wire bonding process. The bond footprint area is normally larger than the actual metallurgical weld interface.

1.3.6 Shear Tool or Arm

A tungsten carbide, or equivalent, chisel with specific angles on the bottom and back of the tool to insure a shearing action.

1.3.7 Wedge/Stitch Bond

The welding of a thin wire, usually aluminum, to a die or package bonding surface using an ultrasonic wire bonding process. The wedge bond, sometimes referred to as a stitch bond, includes the compressed (ultrasonically bonded) area of the bond wire and the underlying bonding surface. When wedge/stitch bonding to an aluminum alloy bonding surface, no intermetallic exists because the two materials are of the same composition; but rather the two materials are combined and recrystallized by the ultrasonic energy of the welding process. For the purposes of this document, all references to wedge/stitch bonds are applicable to aluminum wedge/stitch bonds only; gold wedge/stitch bonds are not required to be wire bond shear tested.

2. APPARATUS AND MATERIAL

The apparatus and materials required for wire bond shear testing shall be as follows:

2.1 Inspection Equipment

An optical microscope system or scanning electron microscope providing a minimum of 30X magnification.

2.2 Measurement Equipment

An optical microscope or measurement system capable of measuring the wire bond diameter to within ± 0.1 mil.

2.3 Workholder

Fixture used to hold the device being tested parallel to the shearing plane and perpendicular to the shear tool. The fixture shall also eliminate device movement during wire bond shear testing. If using a caliper controlled workholder, place the holder so that the shear motion is against the positive stop of the caliper. This is to insure that the recoil movement of the caliper controlled workholder does not influence the wire bond shear test.

2.4 Wire Bond Shear Equipment

The wire bond shear equipment must be capable of precision placement of the shear tool approximately 0.1 mil above the topmost part of the bonding surface. This distance (h) shall insure the shear tool does not contact the die or package bonding surface and shall be less than the distance from the topmost part of the bonding surface to the center line (C_L) of the ball or wedge/stitch bond.

2.5 Bond Shear Tool

Required shear tool parameters include but are not limited to: flat shear face, sharp shearing edge, and shearing width of 1.5 to 2 times (1.5X to 2X) the bond diameter or bond length. The shear tool should be designed to prevent plowing and drag during wire bond shear testing. The shear tool should be clean and free of chips (or other defects) that may interfere with the wire bond shear test.

3. PROCEDURE

3.1 Calibration

Before performing the wire bond shear test, it must be determined that the equipment has been calibrated in accordance with the manufacturer's specifications and is presently in calibration. Recalibration is required if the equipment is moved to another location.

3.2 Visual Examination of Wire Bonds to be Shear Tested After Decapsulation

Before performing wire bond shear testing on a device which has been opened using wet chemical and/or dry etch techniques, the bonding surfaces shall be examined to insure there is no absence of metallization on the bonding surface area due to chemical etching. Ball or wedge/stitch bonds on bonding surfaces with evidence of degradation from chemical attack or absence of metallization shall not be used for wire bond shear testing. Wire bonds on bonding surfaces without degradation from chemical attack may not be attached to the bonding surface due to other causes (e.g., package stress). These wire bonds are considered valid and shall be included in the shear data as a zero (0) gram value. Wire bonds must also be examined to <u>ensure</u> adjacent interfering structures are far enough away to allow suitable placement and clearance (above the bonding surface and between adjacent wire bonds) <u>when performing the wire bond shear test</u>.

3.3 Measurement of the Ball Bond Diameter to Determine the Ball Bond Failure Criteria

Once the bonding surfaces have been examined and prior to performing wire bond shear testing, the diameter of all ball bonds (from at least one representative sample to be tested) shall be measured and recorded. For asymmetrical ball bonds, determine the average using both the largest ($d$large) and the smallest diameter ($d$small) values (see Figure 2). These ball bond diameter measurements shall be used to determine the mean, or average, diameter value. The resulting mean, or average, ball bond diameter shall then be used to establish the failure criteria as defined in section 4.1. If process-monitor data has established the nominal ball bond diameter, then that value may be used to determine the failure criteria as defined in section 4.1.

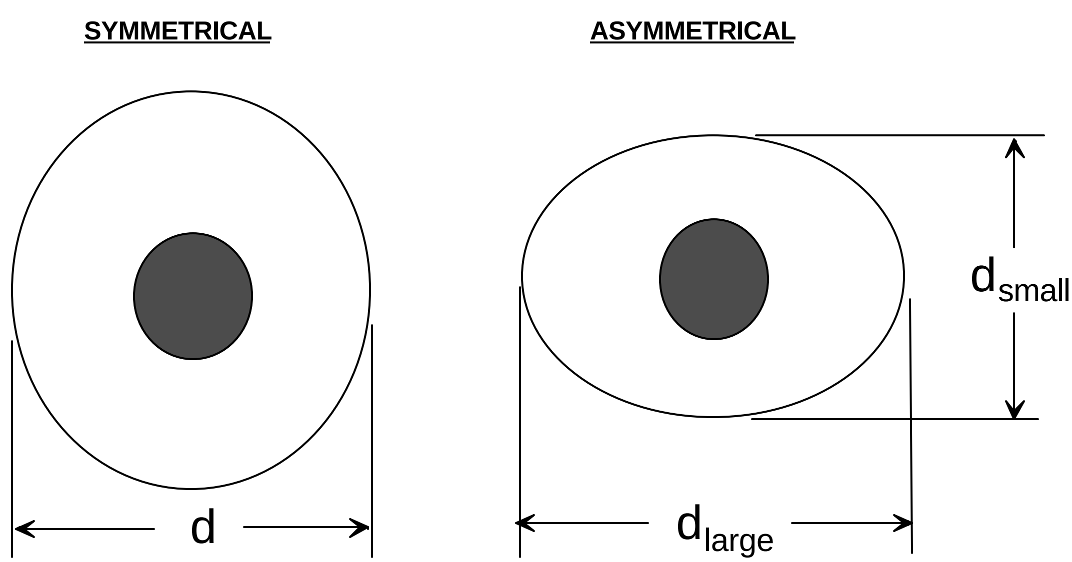


Figure 2: Ball bond diameter measurement (symmetrical vs. asymmetrical)

3.4 Wire Bond Shear Test Procedure

The wire bond shear testing procedure shall be performed as follows:

a. The wire bond shear equipment shall pass all self diagnostic tests prior to performing the wire bond shear test.

b. The wire bond shear equipment and test area shall be free of excessive vibration or movement. Examine the shear tool to verify it is in good condition and is not bent or damaged. Check the shear tool to verify it is in the up position.

c. Adjust the workholder to match the device being tested. Secure the device to the workholder. Make sure the die or package bonding surface is parallel to the shearing plane of the shear tool. It is important that the shear tool does not contact the bonding surface or adjacent structures during the shearing operation as this will give incorrect high readings.

d. Position the device so that the wire bond to be tested is located adjacent to the shear tool. Lower the shear tool (or raise the device depending upon wire bond shear equipment used) to approximately the die or package bonding surface but not contacting the surface (approximately the thickness of the wire bond above the die or package bonding surface).

e. For ball bond shear testing, position the ball bond to be tested so that the shear motion will travel perpendicular to the die edge. Wire bond shear testing is required for ball bonds located at the die bonding surface interface only.

f. For aluminum wedge/stitch bond shear testing, a wire height at the compressed bond area of 1.25 mils and larger is required. For wires too small for wire bond shear testing (less than 1.25 mils in height at the compressed bond area), only a footprint inspection is required (see section 3.6). Position the wedge/stitch bond to be tested so that the shear motion will travel toward the long side of the wedge/stitch bond and is free of any interference (i.e. shear the outside wedge/stitch bond first and then shear toward the previously sheared wedge/stitch bond). Wire bond shear testing is required for aluminum wedge/stitch bonds located at die and package bonding surfaces; gold wedge/stitch bonds are not required to be wire bond shear tested.

g. Position the shear tool a distance of approximately one ball bond diameter (or one aluminum wire diameter for wedge/stitch bonds) from the wire bond to be shear tested and shear the wire bond.

3.5 Examination of Sheared Wire Bonds

All wire bonds shall be sheared in a planned/defined sequence so that later visual examination can determine which shear values should be eliminated due to an improper shear. The wire bonds shall be examined using at least 30X magnification to determine if the shear tool skipped over the wire bond (type 5) or the shear tool scraped or plowed into the die surface (type 4). See Figure 3 for bond shear types and illustrations.

Readings in which either a bond shear type 4 or 5 defective shear condition occurred shall be eliminated from the shear data. Bond shear type 1, 2, 3, and 6 shall be considered acceptable and included in the shear data.

Sheared wire bonds in which a bond shear type 3 cratering condition has occurred shall be investigated further to determine whether the cracking and/or cratering is due to the wire bonding process or the act of wire bond shear testing. Cratering caused prior to the wire bond shear test operation is unacceptable. Cratering resulting from the act of wire bond shear testing shall be considered acceptable and included in the shear data.

3.6 Footprint Inspection of Aluminum Wedge/Stitch Bonds

a. All aluminum wire bonding processes to both die and package bonding surfaces shall have a bond footprint inspection performed.

b. For wires too small for wire bond shear testing (less than 1.25 mils in height at the compressed bond area), the wires shall be removed at the wedge/stitch bond location using a small sharp blade to peel or pluck the wire bond from the bonding surface. The removal of the aluminum wire shall be sufficient such that the wire bond interface can be visually inspected and the metallurgical wire bond area determined.

c. For larger wires (greater than 1.25 mils in height at the compressed bond area), the wires shall be inspected after wire bond shear testing to examine the failure mode and to determine the wedge/stitch bond footprint coverage.

3.7 Bond Shear Data

Data shall be maintained for each wire bond sheared. The data shall identify the wire bond (location, ball bond and/or wire diameter, wire material, method of bonding, and material bonded to), the shear strength, and the bond shear type (as defined in section 1.3.4 and Figure 3).

4. FAILURE CRITERIA

The following failure criteria are not valid for devices that have undergone environmental stress testing or have been desoldered from circuit boards.

4.1 Failure Criteria for Gold Ball Bonds

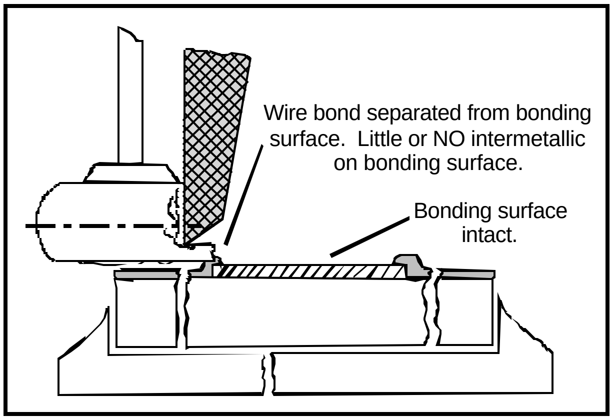
The gold ball bonds on a device shall be considered acceptable if the minimum individual and sample average ball bond shear values are greater than or equal to the values specified in Figure 4 and Table 1. This criteria is applicable for gold wire ball bonds on aluminum alloy bonding surfaces. Other material combinations may require a new set of failure criteria.

Alternate minimum ball bond shear values may be proposed by the supplier if supporting data justifies the proposed minimum values.

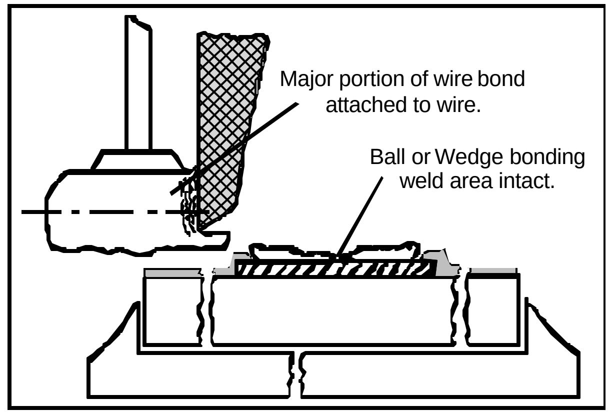
4.2 Failure Criteria for Aluminum Wedge/Stitch Bonds

The aluminum wedge/stitch bonds on a device shall be considered acceptable if the minimum shear values are greater than or equal to the manufacturer's bond wire tensile strength.

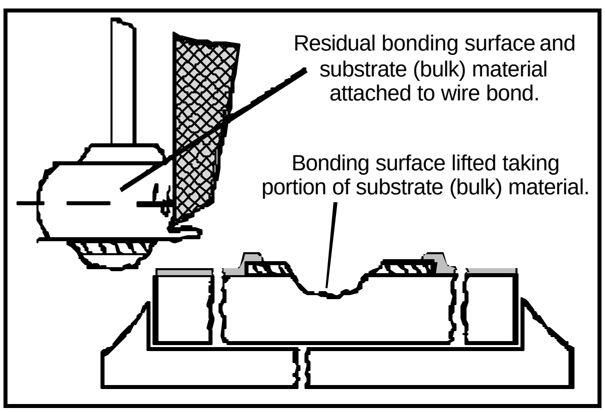
In addition, the percent of the wedge/stitch bond footprint in which bonding occurs shall be greater than or equal to 50%. If it is necessary to control the wire bonding process using SPC for percent coverage, a C_{pk} value can be calculated to this limit.



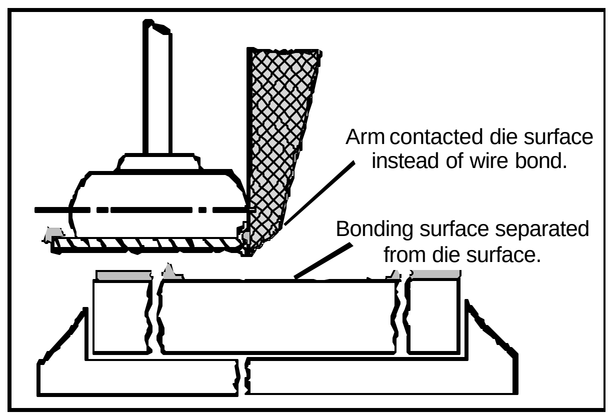
TYPE 1: Bond Lift



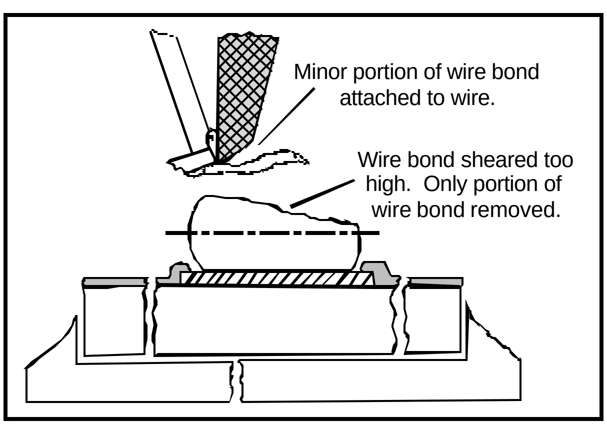
TYPE 2: Bond Shear - Gold/Aluminum



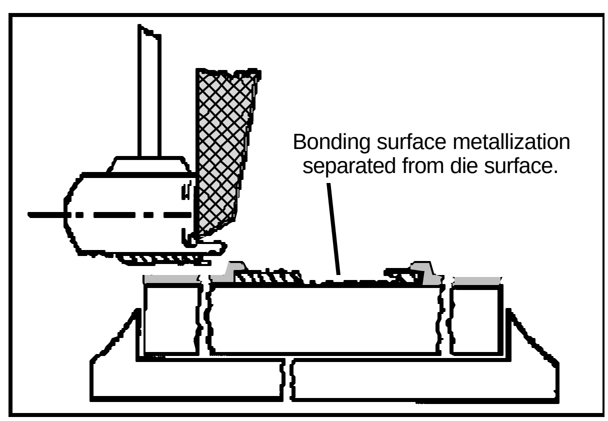
TYPE 3: Cratering



TYPE 4: Die Surface Contact



TYPE 5: Shearing Skip



TYPE 6: Bonding Surface Lift

Figure 3: Wire Bond Shear Types *

*** (Shear types are illustrated using ball bonds; these types also apply to wedge/stitch bonds)**

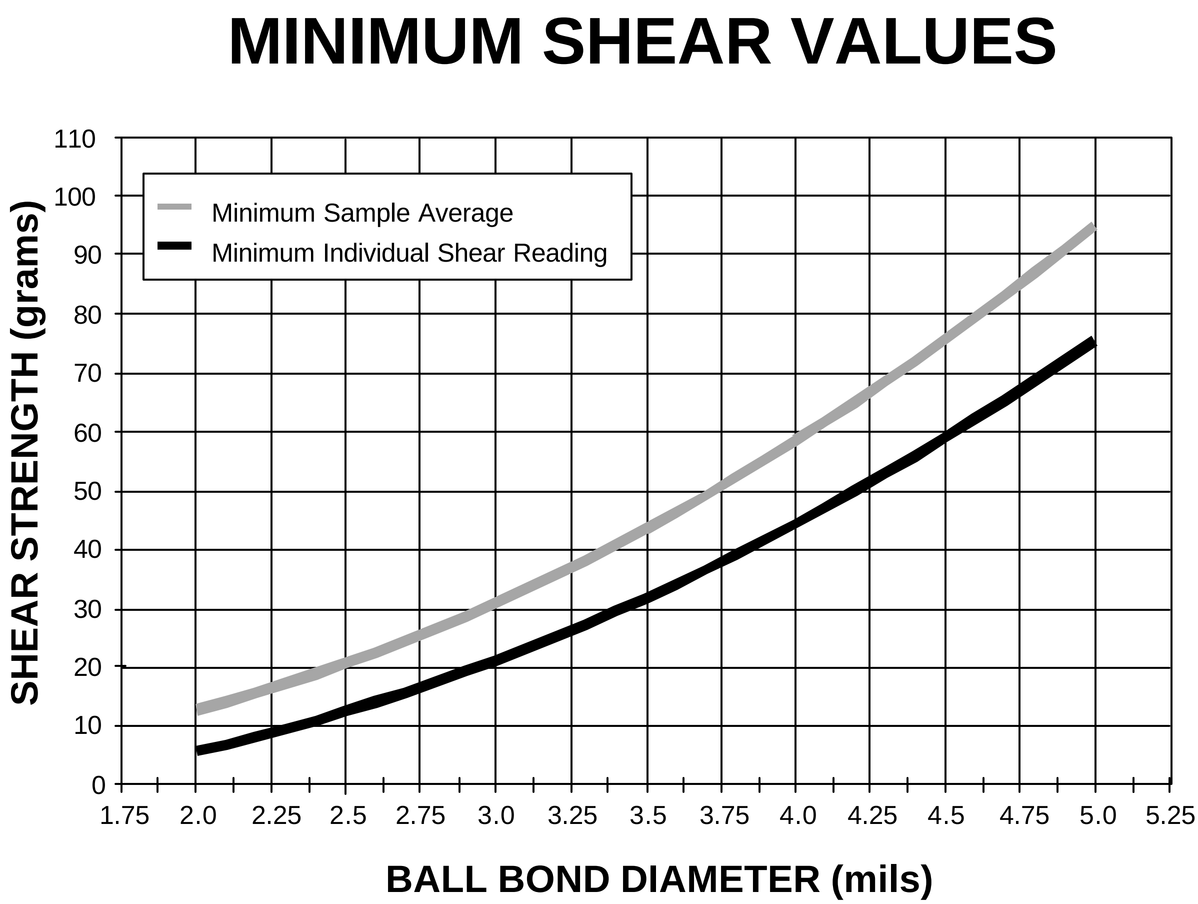


Figure 4: Minimum acceptable individual and sample average ball bond shear values *, see Table 1 for exact ball bond shear values *

*** (Shear values are applicable for gold wire ball bonds on aluminum alloy bonding surfaces)**

Table 1: Minimum acceptable individual and sample average ball bond shear values *

*** (Shear values are applicable for gold wire ball bonds on aluminum alloy bonding surfaces)**

Ball Bond Diameter (mils)	Minimum Sample Average (grams)	Minimum Individual Shear Reading (grams)
2.0	12.6	5.7
2.1	14.0	6.8
2.2	15.5	8.1
2.3	17.1	9.5
2.4	18.8	10.9
2.5	20.6	12.4
2.6	22.4	14.0
2.7	24.4	15.6
2.8	26.5	17.4
2.9	28.6	19.2
3.0	30.8	21.1
3.1	33.2	23.1
3.2	35.6	25.1
3.3	38.1	27.2
3.4	40.7	29.4
3.5	43.4	31.7
3.6	46.2	34.1
3.7	49.1	36.5
3.8	52.1	39.1
3.9	55.2	41.7
4.0	58.3	44.3
4.1	61.6	47.1
4.2	65.0	50.0
4.3	68.4	52.9
4.4	71.9	55.8
4.5	75.6	59.0
4.6	79.3	62.1
4.7	83.1	65.3
4.8	87.0	68.6
4.9	91.0	72.0
5.0	95.1	75.5

Revision History

Rev #	Date of change	Brief summary listing affected sections
-	June 9, 1994	Initial Release.
A	May 19, 1995	Added copyright statement.
B	Sept. 6, 1996	Deleted old Sections 1.3.4, 1.3.5, 3.3, 3.9, and 5.0. Added new Sections 1.3.1, 1.3.2, 1.3.6, 3.4 (steps a through g), and 3.6 (steps a through c). Revised the following: Sections 1.1, 1.2, 1.3.1, 1.3.2, 1.3.3, 1.3.4 (1.3.4.1 through 1.3.4.6), 1.3.5, 1.3.6, 2.1, 2.2, 2.4, 2.5, 3.1, 3.2, 3.3, 3.4 (a, b, c, d, e, f, and g), 3.5, 3.6 (a, b, and c), 3.7, 4.0, 4.1, and 4.2; Table 1; Figures 1, 3, and 4.
C	Oct. 8, 1998	Added new Section 1.3.5. Revised the following: Sections 1.1, 1.3.1, 1.3.4.1, 1.3.4.4, 1.3.4.5, 2.2, 2.5, 3.2, 3.5, 3.6 (b), Figure 3.

ATTACHMENT 2

AEC - Q100-002 REV-C

HUMAN BODY MODEL ELECTROSTATIC DISCHARGE TEST

Acknowledgment

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Council would especially like to recognize the following significant contributors to the development of this document:

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Automotive Electronics Council
Component Technical Committee

Change Notification

The following summary details the changes incorporated into AEC-Q100-002 Rev-C:

- **Section 1.2, Reference Documents: Added reference to JEDEC HBM ESD Test specification EIA/JESD22/A114.**

- **Section 2.1 and Figure 1, Test Apparatus: Added wording to reflect a typical equivalent HBM ESD circuit. Figure 1 is shown for guidance only, it does not attempt to represent all associated components, parasitics, etc..**

- **Table 1, HBM Waveform Specification: Corrected the acceptable Ips (Ipeak for short) parameter values to reflect a ±10% tolerance.**

- **Section 3.5, steps d, e, j, and k: Added wording to allow HBM ESD testing using one (1) ESD pulse with a 500 millisecond minimum delay between consecutive ESD pulses. The use of three (3) ESD pulses with a one (1) second minimum delay between consecutive ESD pulses is also acceptable.**

- **Minor wording changes were made to the following: Section 3.1, Table 2, and Figure 1.**

Automotive Electronics Council
Component Technical Committee

METHOD - 002

HUMAN BODY MODEL (HBM) ELECTROSTATIC DISCHARGE (ESD) TEST

Text enhancements and differences made since the last revision of this document are shown as underlined areas. Several figures have also been revised, but changes to these areas have not been underlined.

1. SCOPE

1.1 Description

The purpose of this specification is to establish a reliable and repeatable procedure for determining the HBM ESD sensitivity for electronic devices.

1.2 Reference Documents

EOS/ESD Association Specification S5.1-1998
JEDEC Specification EIA/JESD22/A114

1.3 Terms and Definitions

The terms used in this specification are defined as follows.

1.3.1 Device Failure

A condition in which a device does not meet all the requirements of the acceptance criteria, as specified in section 5, following the ESD test.

1.3.2 DUT

An electronic device being evaluated for its sensitivity to ESD.

1.3.3 Electrostatic Discharge (ESD)

The transfer of electrostatic charge between bodies at different electrostatic potentials.

1.3.4 Electrostatic Discharge Sensitivity

An ESD voltage level resulting in device failure.

Chrysler	Date	Delphi Delco Electronics Systems	Date	Visteon Automotive Systems	Date
[signature]	9/28/98	[signature]	10/1/98	[signature]	9/25/98
Richard A. Chow - Wah		Gerald E. Servais		Douglas Sendelbach	

1.3.5 ESD Simulator

An instrument that simulates the human body model ESD pulse as defined in this specification.

1.3.6 Human Body Model (HBM) ESD

An ESD pulse meeting the waveform criteria specified in this test method.

1.3.7 Non-Supply Pins

All pins including, but not limited to, input, output, bi-directional, Vref, Vpp, clock, and “no connect” pins. These pins do not supply voltage and/or current to the device under test.

1.3.8 Power Pins

All power supply, external voltage source, and ground pins. All power pins that are metallically connected together on the chip or in the package shall be treated as one (1) power pin.

1.3.9 PUT

The pin under test.

1.3.10 Ringing current (IR)

The high frequency current oscillation usually following the pulse rise time.

1.3.11 Withstanding Voltage

The ESD voltage level at which, and below, the device is determined to pass the failure criteria requirements specified in section 4.

1.3.12 Worst Case Pin Pair (WCP)

WCP is the pin pair representing the worst case waveform that is within the limits and closest to the minimum or maximum parameter values as specified in Table 1. The WCP shall be identified for each socket.

2. EQUIPMENT

2.1 Test Apparatus

The apparatus for this test consists of an ESD pulse simulator and DUT socket. Figure 1 shows a typical equivalent HBM ESD circuit. Other equivalent circuits may be used, but the actual simulator must be capable of supplying pulses which meet the waveform requirements of Table 1, Figure 2, and Figure 3.

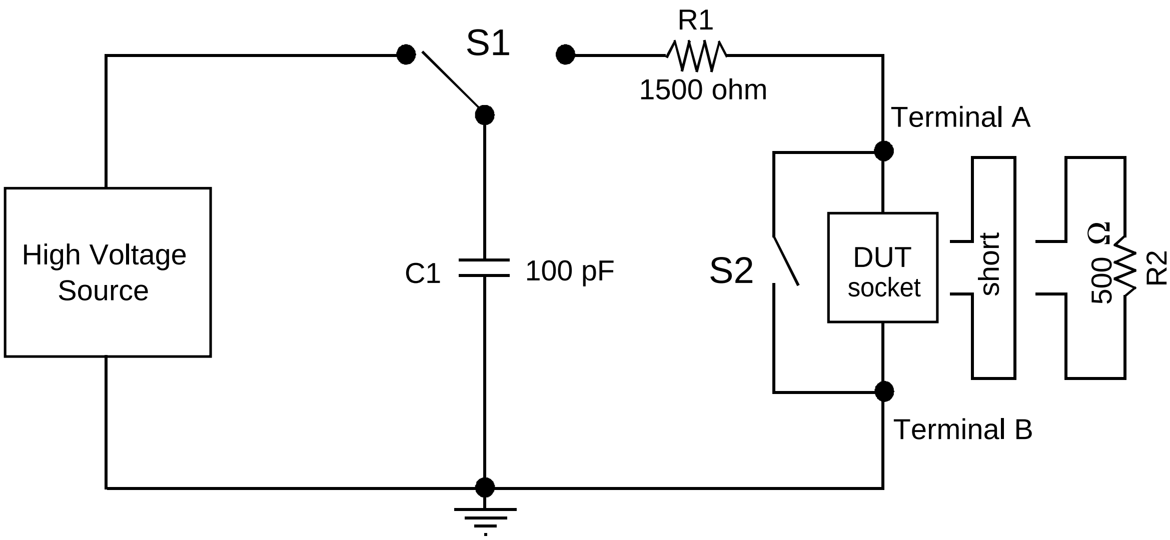


Figure 1: Typical equivalent HBM ESD circuit

Notes:

1. Figure 1 is shown for guidance only; it does not attempt to represent all associated circuit components, parasitics, etc..
2. The performance of any simulator is influenced by its parasitic capacitance and inductance.
3. Precautions must be taken in simulator design to avoid recharge transients and multiple pulses.
4. R2, used for Equipment Qualification as specified in section 2.3, shall be a low inductance, 1000 volt, 500 ohm resistor with ±1% tolerance.
5. Piggybacking of DUT sockets (the insertion of secondary sockets into the main DUT socket) is allowed only if the combined piggyback set (main DUT socket with the secondary DUT socket inserted) waveform meets the requirements of Table 1, Figure 2, and Figure 3.
6. Reversal of terminals A and B to achieve dual polarity is not permitted.
7. S2 should be closed 10 to 100 milliseconds after the pulse delivery period to ensure the DUT socket is not left in a charged state. S2 should be opened at least 10 milliseconds prior to the delivery of the next pulse.

2.2 Measurement Equipment

Equipment shall include an oscilloscope and current probe to verify conformance of the simulator output pulse to the requirements of this document as specified in Table 1, Figure 2, and Figure 3.

2.2.1 Current Probe

The current probe shall have a minimum bandwidth of 350 MHz and maximum cable length of 1 meter (Tektronix CT-1 or equivalent).

2.2.2 Evaluation Loads

The two evaluation loads shall be: 1) a low inductance, 1000 volt, 500 ohm sputtered film resistor with ± 1% tolerance, and 2) an 18 AWG tinned copper shorting wire. The lead length of both the shorting wire and the 500 ohm resistor shall be as short as possible and shall span the maximum distance between the worst case pin pair (WCP) while passing through the current probe as defined in section 2.2.1.

2.2.3 Oscilloscope

The oscilloscope and amplifier combination shall have a minimum bandwidth of 350 MHz, a minimum sensitivity of 100 milliamperes per large division and a minimum visual writing speed of 4 cm per nanosecond.

2.3 Equipment Qualification

Equipment qualification must be performed during initial acceptance testing or after repairs are made to the equipment that may affect the waveform. The simulator must meet the requirements of Table 1 and Figure 2 for five (5) consecutive waveforms at all voltage levels using the worst case pin pair (WCP) on the highest pin count, positive clamp test socket DUT board with the shorting wire per Figure 1. Simulators not capable of producing the maximum voltage level shown in Table 1 shall be qualified to the highest voltage level possible. The simulator must also meet the requirements of Table 1 and Figure 3 for five (5) consecutive waveforms at the 1000 volt level using the worst case pin pair (WCP) on the highest pin count, positive clamp test socket DUT board with the 500 ohm load per Figure 1. Thereafter, the test equipment shall be periodically qualified as described above; a period of one (1) year is the maximum permissible time between full qualification tests.

2.4 Simulator Waveform Verification

The performance of the simulator can be dramatically degraded by parasitics in the discharge path. Therefore, to ensure proper simulation and repeatable ESD results, it is recommended that waveform performance be verified on the worst case pin pair (WCP) using only the shorting wire per section 2.4.1. The worst case pin pair (WCP) for each socket and DUT board shall be identified and documented. The waveform verification shall be performed when a socket/mother board is changed or on a weekly basis (if the equipment is used for at least 20 hours). If at any time the waveforms do not meet the requirements of Table 1 and Figure 2 at either the 1000 or 4000 volt level, the testing shall be halted until waveforms are in compliance.

2.4.1 Waveform Verification Procedure

a. With the required DUT socket installed and with no device in the socket, attach a shorting wire in the DUT socket such that the worst case pin pair (WCP) is connected between terminal A and terminal B as shown in Figure 1. Place the current probe around the shorting wire.

b. Set the horizontal time scale of the oscilloscope at 5 nanoseconds per division or less.

c. Initiate a positive pulse at either the 1000 or 4000 volt level per Table 1. The simulator shall generate only one (1) waveform per pulse applied.

d. Measure and record the rise time, peak current and ringing current. All parameters must meet the limits specified in Table 1 and Figure 2.

e. Initiate a negative pulse at either the 1000 or 4000 volt level per Table 1. The simulator shall generate only one (1) waveform per pulse applied.

f. Measure and record the rise time, peak current and ringing current. All parameters must meet the limits specified in Table 1 and Figure 2.

g. Set the horizontal time scale of the oscilloscope at 100 nanoseconds per division or greater and initiate a positive pulse at either the 1000 or 4000 volt level per Table 1. The simulator shall generate only one (1) waveform per pulse applied.

h. Measure and record the decay time and ringing current. All parameters must meet the limits specified in Table 1 and Figure 2.

i. Initiate a negative pulse at either the 1000 or 4000 volt level per Table 1. The simulator shall generate only one (1) waveform per pulse applied.

j. Measure and record the decay time and ringing current. All parameters must meet the limits specified in Table 1 and Figure 2.

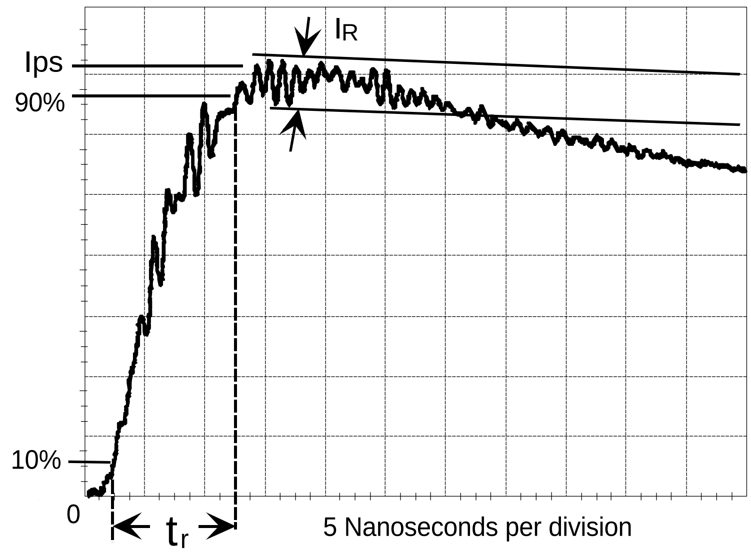
Table 1: HBM Waveform Specification

Voltage Level (V)	Ipeak for Short, I_{ps} (A)	Ipeak for 500 Ohm* I_{pr} (A)	Rise Time for Short, t_r (ns)	Rise Time for 500 Ohm* t_{rr} (ns)	Decay Time for Short, t_d (ns)	Ringing Current I_R (A)
1000	0.60 - 0.74	.375 - .55	2.0 - 10	5.0 - 25	130 - 170	15% of I_{ps} and I_{pr}
2000	1.20 - 1.46	Not Applicable	2.0 - 10	Not Applicable	130 - 170	15% of I_{ps} and I_{pr}
4000	2.40 - 2.94	Not Applicable	2.0 - 10	Not Applicable	130 - 170	15% of I_{ps} and I_{pr}
8000	4.80 - 5.86	Not Applicable	2.0 - 10	Not Applicable	130 - 170	15% of I_{ps} and I_{pr}

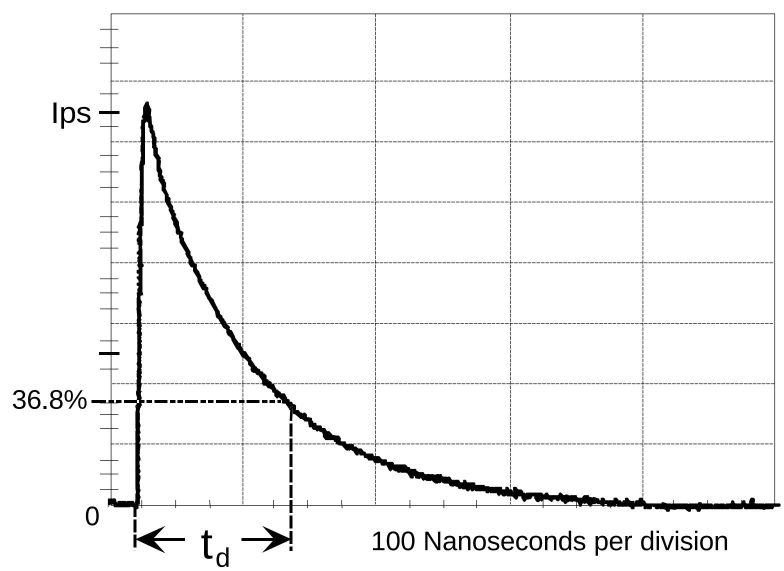
*** The 500 ohm load is used only during Equipment Qualification as specified in section 2.3.**

2.5 Automated ESD Test Equipment Relay Verification

If using automated ESD test equipment, the system diagnostics test shall be performed on all high voltage relays per the equipment manufacturer's instructions. This test normally measures continuity and will identify any open or shorted relays in the test equipment. Relay verification must be performed during initial equipment qualification and on a weekly basis. If the diagnostics test detects relays as failing, all sockets boards using those failed relays shall not be used until the failing relays have been replaced. The test equipment shall be repaired and requalified per section 2.3.

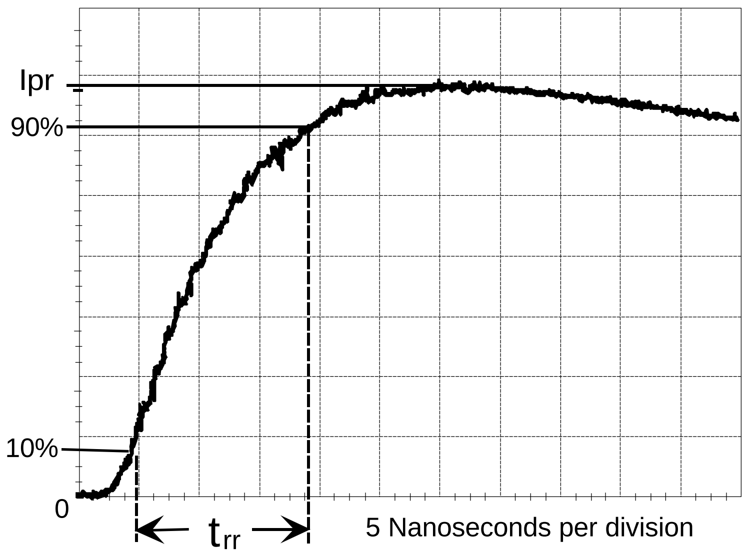


(a) Pulse rise time, (tr)



(b) Pulse decay time, (td)

Figure 2: HBM current waveforms through a shorting wire



(a) Pulse rise time, (t_{rr})

Figure 3: HBM current waveform through a 500 ohm resistor *

*** The 500 ohm load is used only during Equipment Qualification as specified in section 2.3.**

3. PROCEDURE

3.1 Sample Size

Each sample group shall be composed of three (3) units. Each sample group shall be stressed at one (1) voltage level using all pin combinations specified in Table 2. The use of a new sample group for each pin combination specified in Table 2 is also acceptable. It is permitted to use the same sample group for the next pin combination or stress voltage level if all devices in a sample group meet the acceptance criteria requirements specified in section 5 after exposure to a specified voltage level. Therefore the minimum number of devices required for ESD qualification is 3 devices, while the maximum number of devices depends on the number of pin combinations and the number of voltage steps required to achieve the maximum withstanding voltage. For example, a device (1 VCC pin, 1 GND pin, and 2 IO pins) with a maximum withstanding voltage of 2000 volts requires 4 voltage steps of 500 volts each, 3 pin combinations, and 3 devices per pin combination per voltage level for a maximum total of 36 devices.

Maximum # of devices = (# of pin combinations) X (# of voltage steps required) X 3 devices

3.2 Pin Combinations

The pin combinations to be used are given in Table 2. The actual number of pin combinations depends on the number of power pin groups. Power pins of the same name (VCC1, VCC2, VSS1, VSS2, etc.) may be tied together and considered one (1) power pin group if they are connected in the package or on the chip via a metal line. Same name power pins that are resistively connected via the chip substrate or wells, or are electrically isolated from each other, must be treated as a separate power pin group. All pins configured as "no connect" pins shall be considered non-supply pins and included in the pin groups stressed during ESD testing. Integrated Circuits with six (6) pins or less shall be tested using all possible pin pair combinations (one pin connected to terminal A, another pin connected to terminal B) regardless of pin name or function.

Table 2: Pin Combinations for Integrated Circuits

Pin Combination	Connect Individually to Terminal A (Stress)	Connect Individually to Terminal B (Ground)	Floating Pins (unconnected)
1	All pins one at a time, except the pin(s) connected to Terminal B	First power pin(s)	All pins except PUT and first power pin(s)
2	All pins one at a time, except the pin(s) connected to Terminal B	Second power pin(s)	All pins except PUT and second power pin(s)
3	All pins one at a time, except the pin(s) connected to Terminal B	Nth power pin(s)	All pins except PUT and Nth power pin(s)
4	Each Non-supply pin	All other Non-supply pins except PUT	All power pins

3.3 Test Temperature

Each device shall be subjected to ESD pulses at room temperature.

3.4 Measurements

Prior to ESD testing, complete initial DC parametric and functional testing (initial ATE verification) shall be performed on all sample groups and all devices in each sample group per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3.5 Detailed Procedure

The ESD testing procedure shall be per the test flow diagram of Figure 4 and as follows:

a. Set the pulse voltage at 500 volts. Voltage level skipping is not allowed.

b. Connect a power pin group to terminal B. Leave all other power pins unconnected (see Table 2 / pin combination 1).

c. Connect an individual pin to terminal A. Leave all other pins unconnected.

d. Apply one (1) positive pulse at the specified voltage to the PUT. Wait a minimum of 500 milliseconds before applying the next test pulse. The use of three (3) pulses at each stress voltage polarity is also acceptable.

e. Apply one (1) negative pulse at the specified voltage to the PUT. Wait a minimum of 500 milliseconds before applying the next test pulse. The use of three (3) pulses at each stress voltage polarity is also acceptable.

f. Disconnect the PUT from testing and connect the next individual pin to terminal A. Leave all other pins unconnected.

g. Repeat steps (d) through (f) until every pin not connected to terminal B is pulsed at the specified voltage.

h. Repeat steps (b) through (g) until all power pin groups have been stressed (see Table 2 / pin combinations 2 and 3). The use of a new sample group for each pin combination specified in Table 2 is also acceptable.

i. Connect one non-supply pin to terminal A and tie all other non-supply pins to terminal B. Leave all power pins unconnected (see Table 2 / pin combination 4). The use of a new sample group for each pin combination specified in Table 2 is also acceptable.

j. Apply one (1) positive pulse at the specified voltage to the PUT. Wait a minimum of 500 milliseconds before applying the next test pulse. The use of three (3) pulses at each stress voltage polarity is also acceptable.

k. Apply one (1) negative pulse at the specified voltage to the PUT. Wait a minimum of 500 milliseconds before applying the next test pulse. The use of three (3) pulses at each stress voltage polarity is also acceptable.

l. Disconnect the PUT from testing and connect the next non-supply pin to terminal A. Tie all non-supply pins not under test to terminal B. Leave all other pins unconnected (see Table 2 / pin combination 4).

m. Repeat steps (j) through (l) until all non-supply pins have been tested.

n. Test the next device in the sample group and repeat steps (b) through (m) until all devices in the sample group have been tested at the specified voltage level.

o. Submit the device for complete DC parametric and functional testing (final ATE verification) per the device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification, and determine whether the devices pass the failure criteria requirements specified in section 4. The functionality of "E^2PROM" type devices shall be verified by programming random patterns. If a different sample group is tested for each pin combination or stress voltage level, it is permitted to perform the DC parametric and functional testing (final ATE verification) per device specification after all sample groups have been tested.

p. Using the next sample group, increase the pulse voltage by 500 volts and repeat steps (b) through (o). Voltage level skipping is not allowed. It is permitted to use the same sample group for the next pin combination or stress voltage level if all devices in a sample group pass the failure criteria requirements specified in section 4 after exposure to a specified voltage level.

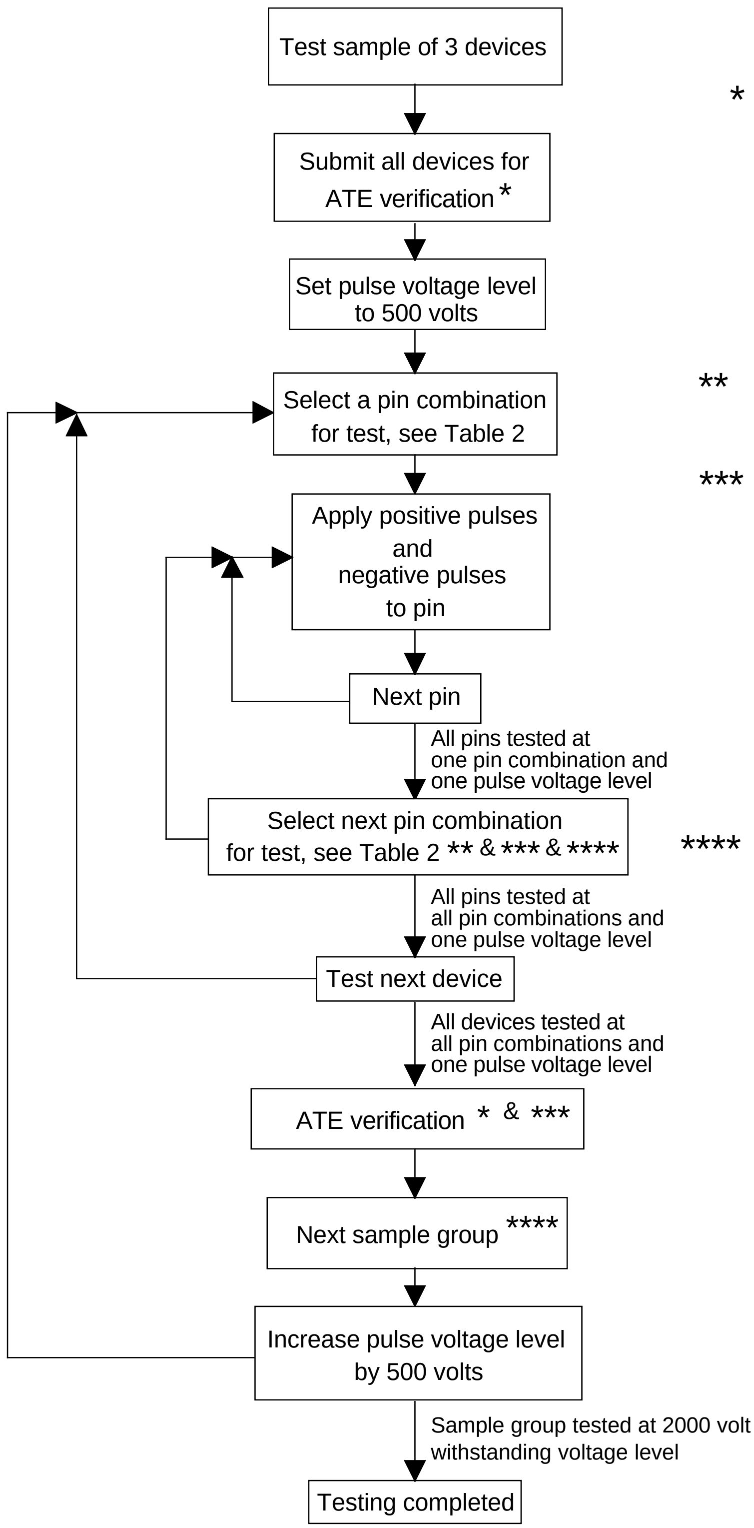
q. Repeat steps (b) through (p) until failure occurs or a 2000 volt withstanding voltage level has been reached.

4. FAILURE CRITERIA

A device will be defined as a failure if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete DC parametric and functional testing (initial and final ATE verification) shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

5. ACCEPTANCE CRITERIA

A device passes a voltage level if all devices in the sample group stressed at that voltage level pass. All the devices and sample groups used must pass the measurement requirements specified in section 3 and the failure criteria requirements specified in section 4 up to a 2000 volt withstanding voltage level in order for the devices to be considered acceptable. The ESD withstanding voltage shall be defined for each device by the supplier.



* For initial ATE verification, all devices shall be tested to complete DC parametric and functional requirements per applicable Device Specification at room temperature followed by hot temperature, unless specified otherwise in the Device Specification.

** The use of a new sample group for each pin combination specified in Table 2 is also acceptable.

*** If a different sample group is tested at each pin combination or stress voltage level, it is permitted to perform complete DC parametric and functional testing (final ATE verification) per applicable Device Specification at room temperature followed by hot temperature, unless specified otherwise in the Device Specification, after all sample groups have completed testing.

**** It is permitted to use the same sample group for the next pin combination or stress voltage level if all devices in the sample group pass the failure criteria requirements specified in section 4 after exposure to a specified pulse voltage level.

Figure 4: Integrated circuit HBM ESD test flow diagram

Revision History

Rev #	Date of change	Brief summary listing affected sections
-	June 9, 1994	Initial Release
A	May 15, 1995	Added copyright statement. Revised the following: Foreword; Sections 2.3, 2.4, 3.1, 3.2, 3.4, 3.5 (g, h, I, o, and p), and 4.0; Tables 1 and 2; Figures 2, 3, and 4.
B	Sept. 6, 1996	Revised the following: Sections 1.3.1, 1.3.7, 1.3.8, 2.1, 2.3, 3.1, 3.2, 3.3, 3.4, 3.5 (o, p, and q), 4.0, and 5.0; Figures 1 and 4.
C	Oct. 8, 1998	Revised the following: Sections 1.2, 2.1, 3.1, 3.5 (d, e, j, and k); Tables 1 and 2; Figure 1. Revision to section 3.5 (d, e, j, and k) reflects a change from three (3) ESD pulses with a one (1) second minimum delay between consecutive ESD pulses at each stress polarity to one (1) ESD pulse with a 500 millisecond minimum delay between consecutive ESD pulses. The use of three (3) ESD pulses with a one (1) second minimum delay between consecutive ESD pulses is also acceptable. Revision to Table 1 reflects a ±10% tolerance applied to all Ips (Ipeak for short) parameter values.

ATTACHMENT 3

AEC - Q100-003 REV-E

MACHINE MODEL ELECTROSTATIC DISCHARGE TEST

Acknowledgment

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Council would especially like to recognize the following significant contributors to the development of this document:

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Automotive Electronics Council
Component Technical Committee

METHOD - 003

MACHINE MODEL (MM) ELECTROSTATIC DISCHARGE (ESD) TEST

Changes since the last revision are double underlined.

It is anticipated that the next revision of Q100 will adopt Q100-011 Charged Device Model (CDM) as a replacement for Q100-003 Machine Model (MM) ESD. Suppliers capable of performing Q100-011 CDM may adopt this change now.

1. SCOPE

1.1 Description

The purpose of this specification is to establish a reliable and repeatable procedure for determining the MM ESD sensitivity for electronic devices.

1.2 Reference Documents

EOS/ESD Association Specification S5.2-1994
JEDEC Specification EIA/JESD22-A115

1.3 Terms and Definitions

The terms used in this specification are defined as follows.

1.3.1 Device Failure

A condition in which a device does not meet all the requirements of the acceptance criteria, as specified in section 5, following the ESD test.

1.3.2 DUT

An electronic device being evaluated for its sensitivity to ESD.

1.3.3 Electrostatic Discharge (ESD)

The transfer of electrostatic charge between bodies at different electrostatic potentials.

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1.3.4 Electrostatic Discharge Sensitivity

An ESD voltage level resulting in device failure.

1.3.5 ESD Simulator

An instrument that simulates the machine model ESD pulse as defined in this specification.

1.3.6 Machine Model (MM) ESD

An ESD pulse meeting the waveform criteria specified in this test method, approximating an ESD pulse from a machine or mechanical equipment.

1.3.7 Major Pulse Period (tpm)

The time (tpm) measured between first and third zero crossing points.

1.3.8 Non-Supply Pins

All pins including, but not limited to, input, output, bi-directional, Vref, Vpp, clock, and "no-connect" pins. These pins do not supply voltage and/or current to the device under test.

1.3.9 Power Pins

All power supplies, external voltage source and ground pins. All power pins that are metallically connected together on the chip or in the package shall be treated as one (1) power pin.

1.3.10 PUT

The pin under test.

1.3.11 Withstanding Voltage

The ESD voltage level at which, and below, the device is determined to pass the failure criteria requirements specified in section 4.

1.3.12 Worst Case Pin Pair (WCP)

WCP is the pin pair representing the worst case waveform that is within the limits and closest to the minimum or maximum parameter values as specified in Table 1. The WCP shall be identified for each socket. It is permissible to use the worst case pin pair that has been previously identified by the HBM ESD method (AEC-Q100-002) when performing the Simulator Waveform Verification as defined in section 2.4.

2. EQUIPMENT

2.1 Test Apparatus

The apparatus for this test consists of an ESD pulse simulator and DUT socket. Figure 1 shows a typical equivalent MM ESD circuit. Other equivalent circuits may be used, but the actual simulator must be capable of supplying pulses that meet the waveform requirements of Table 1, Figure 2, and Figure 3.

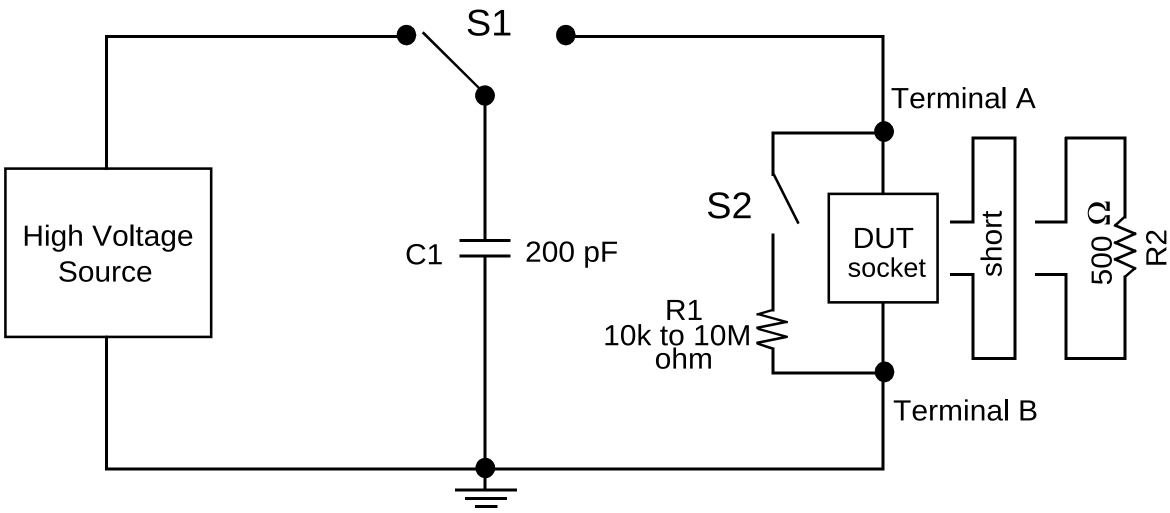


Figure 1 Typical equivalent MM ESD circuit

Notes:

1. Figure 1 is shown for guidance only; it does not attempt to represent all associated circuit components, parasitics, etc..
2. The performance of any simulator is influenced by its parasitic capacitance and inductance.
3. Resistor R1, in series with switch S2, ensures a slow discharge of the device.
4. Precautions must be taken in simulator design to avoid recharge transients and multiple pulses.
5. R2, used for Equipment Qualification as specified in section 2.3, shall be a low inductance, 1000 volt, 500 ohm resistor with ±1% tolerance.
6. Piggybacking of DUT sockets (the insertion of secondary sockets into the main DUT socket) is allowed only if the combined piggyback set (main DUT socket with the secondary DUT socket inserted) waveform meets the requirements of Table 1, Figure 2, and Figure 3.
7. Reversal of terminals A and B to achieve dual polarity is not permitted
8. S2 should be closed 10 to 100 milliseconds after the pulse delivery period to ensure the DUT socket is not left in a charged state. S2 should be opened at least 10 milliseconds prior to the delivery of the next pulse.

2.2 Measurement Equipment

Equipment shall include an oscilloscope and current probe to verify conformance of the simulator output pulse to the requirements of this document as specified in Table 1, Figure 2, and Figure 3.

2.2.1 Current Probe

The current probe shall have a minimum bandwidth of 350 MHz and maximum cable length of 1 meter (Tektronix CT-1, CT-2, or equivalent). A CT-2 probe or equivalent should be used with voltages greater than 800 volts.

2.2.2 Evaluation Loads

The two evaluation loads shall be: 1) a low inductance, 1000 volt, 500 ohm sputtered film resistor with ± 1% tolerance, and 2) an 18 AWG tinned copper shorting wire. The lead length of both the shorting wire and the 500 ohm resistor shall be as short as possible and shall span the maximum distance between the worst case pin pair (WCP) while passing through the current probe as defined in section 2.2.1.

2.2.3 Oscilloscope

The oscilloscope and amplifier combination shall have a minimum bandwidth of 350 MHz, a minimum sensitivity of 100 milliamperes per large division and a minimum visual writing speed of 4 cm per nanosecond.

2.3 Equipment Qualification

Equipment qualification must be performed during initial acceptance testing or after repairs are made to the equipment that may affect the waveform. The simulator must meet the requirements of Table 1 and Figure 2 for five (5) consecutive waveforms at all voltage levels using the worst case pin pair (WCP) on the highest pin count, positive clamp test socket DUT board with the shorting wire per Figure 1. The simulator must also meet the requirements of Table 1 and Figure 3 for five (5) consecutive waveforms at the 400 volt level using the worst case pin pair (WCP) on the highest pin count, positive clamp test socket DUT board with the 500 ohm load per Figure 1. Thereafter, the test equipment shall be periodically qualified as described above; a period of one (1) year is the maximum permissible time between full qualification tests.

2.4 Simulator Waveform Verification

The performance of the simulator can be dramatically degraded by parasitics in the discharge path. Therefore, to ensure proper simulation and repeatable ESD results, it is recommended that waveform performance be verified on the worst case pin pair (WCP) using the shorting wire per section 2.4.1. The worst case pin pair (WCP) for each socket and DUT board shall be identified and documented. The waveform verification shall be performed when a socket/mother board is changed or on a weekly basis (if the equipment is used for at least 20 hours). If at any time the waveforms do not meet the requirements of Table 1 and Figure 2 at the 400 volt level, the testing shall be halted until waveforms are in compliance.

2.4.1 Waveform Verification Procedure

a. With the required DUT socket installed and with no device in the socket, attach a shorting wire in the DUT socket such that the worst case pin pair (WCP) is connected between terminal A and terminal B as shown in Figure 1. Place the current probe around the shorting wire.

b. Set the horizontal time scale of the oscilloscope at 20 nanoseconds per division or greater.

c. Initiate a positive pulse at the 400 volt level per Table 1. The simulator shall generate only one (1) waveform per pulse applied.

d. Measure and record the first peak current, second peak current, and major pulse period. All parameters must meet the limits specified in Table 1 and Figure 2.

e. Initiate a negative pulse at the 400 volt level per Table 1. The simulator shall generate only one (1) waveform per pulse applied.

f. Measure and record the first peak current, second peak current, and major pulse period. All parameters must meet the limits specified in Table 1 and Figure 2.

Table 1 MM Waveform Specification

Voltage Level (V)	Positive First Peak Current for Short, I_{ps1} (A)	Positive Second Peak Current for Short, I_{ps2} (A)	Major Pulse Period for Short, t_{pm} (ns)	Positive First Peak Current for 500 Ohm*, I_{pr} (A)	Current at 100 ns for 500 Ohm*, I_{100} (A)
100	1.5 - 2.0	67% to 90% of I_{ps1}	66 - 90	Not Applicable	Not Applicable
200	3.0 - 4.0	67% to 90% of I_{ps1}	66 - 90	Not Applicable	Not Applicable
400	6.0 - 8.1	67% to 90% of I_{ps1}	66 - 90	0.85 to 1.2	0.29 ± 10%
800	11.9 - 16.1	67% to 90% of I_{ps1}	66 - 90	Not Applicable	Not Applicable

*** The 500 ohm load is used only during Equipment Qualification as specified in section 2.3.**

2.5 Automated ESD Test Equipment Relay Verification

If using automated ESD test equipment, the system diagnostics test shall be performed on all high voltage relays per the equipment manufacturer's instructions. This test normally measures continuity and will identify any open or shorted relays in the test equipment. Relay verification must be performed during initial equipment qualification and on a weekly basis. If the diagnostics test detects relays as failing, all sockets boards using those failed relays shall not be used until the failing relays have been replaced. The test equipment shall be repaired and requalified per section 2.3.

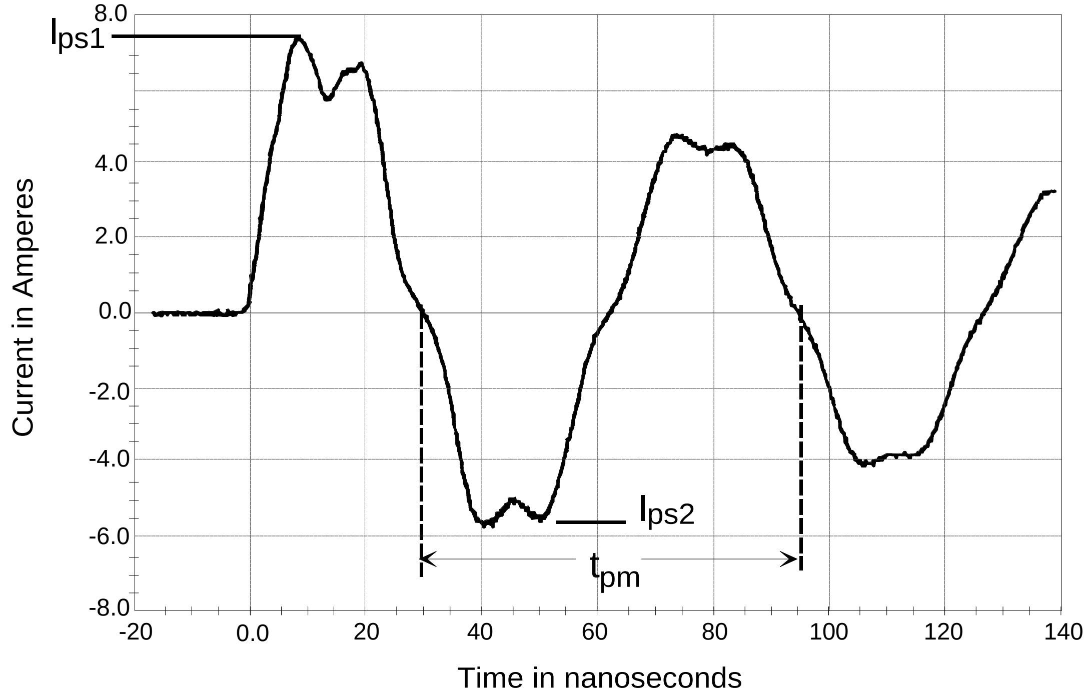


Figure 2 MM current waveform through a shorting wire, 400 volt discharge

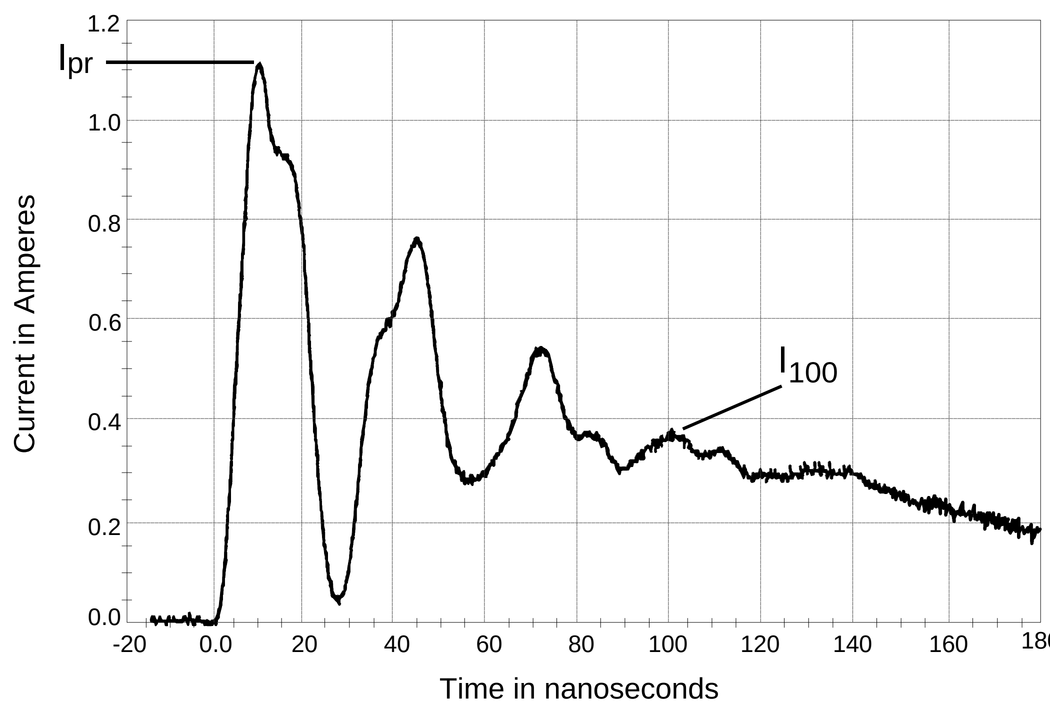


Figure 3 MM current waveform through a 500 ohm resistor *, 400 volt discharge

*** The 500 ohm load is used only during Equipment Qualification as specified in section 2.3.**

3. PROCEDURE

3.1 Sample Size

Each sample group shall be composed of three (3) units. Each sample group shall be stressed at one (1) voltage level using all pin combinations specified in Table 2. The use of a new sample group for each pin combination specified in Table 2 is also acceptable. It is permitted to use the same sample group for the next pin combination or stress voltage level if all devices in a sample group meet the acceptance criteria requirements specified in section 5 after exposure to a specified voltage level. Therefore the minimum number of devices required for ESD qualification is 3 devices, while the maximum number of devices depends on the number of pin combinations and the number of voltage steps required to achieve the maximum withstanding voltage. For example, a device (1 VCC pin, 1 GND pin, and 2 IO pins) with a maximum withstanding voltage of 200 volts requires 2 voltage steps of 100 volts each, 3 pin combinations, and 3 devices per pin combination per voltage level for a maximum total of 18 devices.

Maximum # of devices = (# of pin combinations) X (# of voltage steps required) X 3 devices

3.2 Pin Combinations

The pin combinations to be used are given in Table 2. The actual number of pin combinations depends on the number of power pin groups. Power pins of the same name (VCC1, VCC2, VSS1, VSS2, etc.) may be tied together and considered one (1) power pin group if they are connected in the package or on the chip via a metal line. Same name power pins that are resistively connected via the chip substrate or wells, or are electrically isolated from each other, must be treated as a separate power pin group. All pins configured as "no connect" pins shall be considered non-supply pins and included in the pin groups stressed during ESD testing. Integrated Circuits with six (6) pins or less shall be tested using all possible pin pair combinations (one pin connected to terminal A, another pin connected to terminal B) regardless of pin name or function.

Table 2 Pin Combinations for Integrated Circuits

Pin Combination	Connect Individually to Terminal A (Stress)	Connect Individually to Terminal B (Ground)	Floating Pins (unconnected)
1	All pins one at a time, except the pin(s) connected to Terminal B	First power pin(s)	All pins except PUT and first power pin(s)
2	All pins one at a time, except the pin(s) connected to Terminal B	Second power pin(s)	All pins except PUT and second power pin(s)
3	All pins one at a time, except the pin(s) connected to Terminal B	Nth power pin(s)	All pins except PUT and Nth power pin(s)
4	Each Non-supply pin	All other Non-supply pins except PUT	All power pins

3.3 Test Temperature

Each device shall be subjected to ESD pulses at room temperature.

3.4 Measurements

Prior to ESD testing, complete initial DC parametric and functional testing (initial ATE verification) shall be performed on all sample groups and all devices in each sample group per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3.5 Detailed Procedure

The ESD testing procedure shall be per the test flow diagram of Figure 4 and as follows:

a. Set the pulse voltage at 50 volts. Voltage level skipping is not allowed.

b. Connect a power pin group to terminal B. Leave all other power pins unconnected (see Table 2 / pin combination 1).

c. Connect an individual pin to terminal A. Leave all other pins unconnected.

d. Apply one (1) positive pulse at the specified voltage to the PUT. Wait a minimum of one (1) second before applying the next test pulse. The use of three (3) pulses at each stress voltage polarity is required.

e. Apply one (1) negative pulse at the specified voltage to the PUT. Wait a minimum of one (1) second before applying the next test pulse. The use of three (3) pulses at each stress voltage polarity is required.

f. Disconnect the PUT from testing and connect the next individual pin to terminal A. Leave all other pins unconnected.

g. Repeat steps (d) through (f) until every pin not connected to terminal B is pulsed at the specified voltage.

h. Repeat steps (b) through (g) until all power pin groups have been stressed (see Table 2 / pin combinations 2 and 3). The use of a new sample group for each pin combination specified in Table 2 is also acceptable.

i. Connect one non-supply pin to terminal A and tie all other non-supply pins to terminal B. Leave all power pins unconnected (see Table 2 / pin combination 4). The use of a new sample group for each pin combination specified in Table 2 is also acceptable.

j. Apply one (1) positive pulse at the specified voltage to the PUT. Wait a minimum of one (1) second before applying the next test pulse. The use of three (3) pulses at each stress voltage polarity is required.

k. Apply one (1) negative pulse at the specified voltage to the PUT. Wait a minimum of one (1) second before applying the next test pulse. The use of three (3) pulses at each stress voltage polarity is required.

l. Disconnect the PUT from testing and connect the next non-supply pin to terminal A. Tie all non-supply pins not under test to terminal B. Leave all other pins unconnected (see Table 2 / pin combination 4).

m. Repeat steps (j) through (l) until all non-supply pins have been tested.

n. Test the next device in the sample group and repeat steps (b) through (m) until all devices in the sample group have been tested at the specified voltage level.

o. Submit the device for complete DC parametric and functional testing (final ATE verification) per the device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification, and determine whether the devices pass the failure criteria requirements specified in section 4. The functionality of "E^2PROM" type devices shall be verified by programming random patterns. If a different sample group is tested for each pin combination or stress voltage level, it is permitted to perform the DC parametric and functional testing (final ATE verification) per device specification after all sample groups have been tested.

p. Using the next sample group, increase the pulse voltage by 50 volts and repeat steps (b) through (o). Voltage level skipping is not allowed. It is permitted to use the same sample group for the next pin combination or stress voltage level if all devices in a sample group pass the failure criteria requirements specified in section 4 after exposure to a specified voltage level.

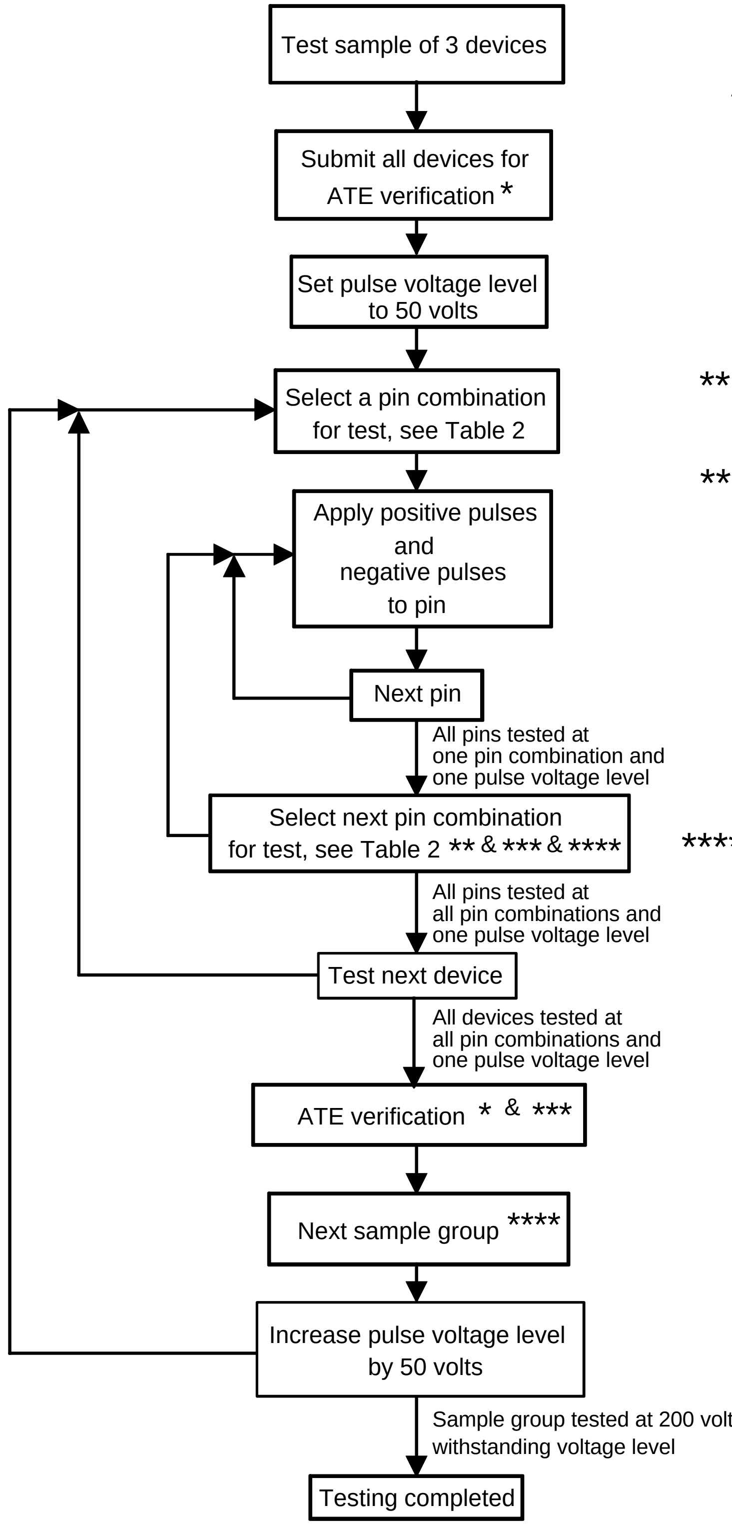
q. Repeat steps (b) through (p) until failure occurs or a 200 volt withstanding voltage level has been reached.

4. FAILURE CRITERIA

A device will be defined as a failure if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete DC parametric and functional testing (initial and final ATE verification) shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

5. ACCEPTANCE CRITERIA

A device passes a voltage level if all devices in the sample group stressed at that voltage level pass. All the devices and sample groups used must pass the measurement requirements specified in section 3 and the failure criteria requirements specified in section 4 up to a 200 volt withstanding voltage level in order for the devices to be considered acceptable. The ESD withstanding voltage shall be defined for each device by the supplier.



* For initial ATE verification, all devices shall be tested to complete DC parametric and functional requirements per applicable Device Specification at room temperature followed by hot temperature, unless specified otherwise in the Device Specification.

** The use of a new sample group for each pin combination specified in Table 2 is also acceptable.

*** If a different sample group is tested at each pin combination or stress voltage level, it is permitted to perform complete DC parametric and functional testing (final ATE verification) per applicable Device Specification at room temperature followed by hot temperature, unless specified otherwise in the Device Specification, after all sample groups have completed testing.

**** It is permitted to use the same sample group for the next pin combination or stress voltage level if all devices in the sample group pass the failure criteria requirements specified in section 4 after exposure to a specified pulse voltage level.

Figure 4 Integrated circuit MM ESD test flow diagram

Revision History

Rev #	Date of change	Brief summary listing affected sections
-	June 9, 1994	Initial Release
A	May 15, 1995	Added Copyright statement. Revised the following: Foreword; Sections 2.3, 2.4, 3.1, 3.2, 3.4, 3.5 (g, h, I, o, and p), and 4.0; Tables 1 and 2; Figures 2, 3, and 4.
B	Sept. 6, 1996	Revised the following: Sections 1.3.1, 1.3.7, 1.3.8, 2.1, 2.4.1 (d and f), 3.1, 3.2, 3.3, 3.4, 3.5 (o, p, and q), 4.0, and 5.0; Table 1; Figures 1 and 4.
C	Oct. 8, 1998	Revised the following: Sections 1.2, 2.1, 3.1, 3.5 (a and p); Tables 1 and 2; Figures 1 and 4. Revision to section 3.5 (a and p) and Figure 4 reflects a change from 100 volt increments to 50 volt increments. Revision to Table 1 reflects the addition of a 100 volt level and a ±15% tolerance applied to all Ips1 (positive first peak current for short) parameter values.
D	Aug.25, 2000	Added note to page 1 concerning optional use of Q100-011 Field Induced Charged Device Model (FCDM) instead of Q100-003 Machine Model.
E	Jan. 31, 2001	Revised note on page 1.

ATTACHMENT 4

AEC - Q100-004 REV-C

IC LATCH-UP TEST

Acknowledgment

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Council would especially like to recognize the following significant contributors to the development of this document:

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Change Notification

The following summary details the changes incorporated into AEC-Q100-004 Rev-C:

- **Replaced CDF-AEC-Q100-004 with the JEDEC IC Latch-up Test specification EIA/JESD78.**
- **Section 1.2, Class II Classification: AEC-Q100 latch-up testing shall be performed at the maximum ambient operating temperature.**
- **Section 1.3, Failure criteria: Device does not pass the test requirements of Table 1 (JEDEC - Level A); or Device no longer meets device specification requirements.**
- **Section 4.1 and Table 1A: The use of a voltage trigger (E-test) Latch-up test is also acceptable. Specific E-test parameters are indicated in Table 1A.**

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METHOD - 004

IC LATCH-UP TEST

All Latch-up testing performed on Integrated Circuit devices to be AEC Q100 qualified shall be per the JEDEC EIA/JESD78 specification with the following requirements (section numbers listed correspond to the JEDEC specification):

1.2 Class II Classification

All AEC Q100-004 qualification testing shall be performed with the device under test at the maximum ambient operating temperature (JEDEC - Class II).

1.3 Level A Failure Criteria

A device failure is defined by either of the following conditions:

1. Device does not pass the test requirements of Table 1 (JEDEC - Level A).

2. Device no longer meets device specification requirements. Complete DC parametric and functional testing (initial and final ATE verification) shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

4.1 General Latch-up Test Procedure

The use of a voltage trigger (E-test) latch-up test is also acceptable. E-test is a latch-up test in which positive and negative pulses are applied to the pin under test. The actual test procedure shall be performed per the I-test procedure, substituting a voltage trigger for the current trigger. Specific E-test parameters are indicated in Table 1A.

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Table 1A: E-test addendum to JEDEC specification Table 1, Test Matrix **[5]**

<table>
<tr><th>TEST TYPE</th><th>TRIGGER POLARITY</th><th>CONDITION OF UNTESTED INPUT PINS</th><th>TEST TEMPERATURE (± 2°C)</th><th>V_{supply} CONDITION</th><th>TRIGGER TEST CONDITIONS</th><th>FAILURE CRITERIA</th></tr>
<tr><td rowspan="4">E-TEST</td><td rowspan="2">POSITIVE see FIGURE 5</td><td>Max. Logic High [1]</td><td rowspan="4">Maximum ambient operating temperature</td><td rowspan="4">Maximum operating voltage for each V_{supply} pin group per device specification</td><td rowspan="2">+1.5X max. Logic High [2]</td><td rowspan="4">(I_{nom} + 10mA) or (1.4 X I_{nom}), whichever is greater [4]</td></tr>
<tr><td>Min. Logic Low [1]</td></tr>
<tr><td rowspan="2">NEGATIVE see FIGURE 6</td><td>Max. Logic High [1]</td><td rowspan="2">-0.5X max. Logic High [3]</td></tr>
<tr><td>Min. Logic Low [1]</td></tr>
</table>

Notes:

[1] Max. logic high and min. logic low shall be per the device specification. When logic levels are used with respect to a non-digital device, it means the maximum high or minimum low voltage that can be supplied to the pin per the device specification.

[2] Current clamped at (I_{nom} + 100 mA) or 1.5X I_{nom}, whichever is greater.

[3] Current clamped at -100 mA or -0.5X I_{nom}, whichever is greater in magnitude.

[4] If the trigger test condition reaches the voltage or current clamp limit and latch-up has not occurred, the pin passes the latch-up test. See section 5 of the JEDEC specification for complete failure definition.

[5] The trigger conditions herein are not indicative of appropriate trigger conditions for all devices. Appropriate trigger conditions may be more or less stringent. When trigger conditions used in testing differ from this table, the trigger conditions used must be defined in the test results.

Revision History

Rev #	Date of change	Brief summary listing affected sections
-	June 9, 1994	Initial Release
A	May 15, 1995	Added copyright statement. Revised the following: Foreword; Sections 2.3, 2.4, 3.1, 3.2, 3.4, 3.5 (g, h, I, o, and p), and 4.0; Tables 1 and 2; Figures 2, 3, and 4.
B	Sept. 6, 1996	Revised the following: Sections 1.3.1, 1.3.7, 1.3.8, 2.1, 2.3, 3.1, 3.2, 3.3, 3.4, 3.5 (o, p, and q), 4.0, and 5.0; Figures 1 and 4.
C	Oct. 8, 1998	Replaced CDF-AEC-Q100-004 with the JEDEC IC Latch-up Test specification EIA/JESD78 with additional requirements. Added the following requirements: Sections 1.2, 1.3, and 4.1 (to correspond with the JEDEC specification section numbers); Table 1A (E-test addendum to JEDEC specification Table 1).

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ATTACHMENT 5

AEC - Q100-005 Rev-A

E^{2}PROM ENDURANCE/DATA RETENTION TEST

Acknowledgment

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Council would especially like to recognize the following significant contributors to the development of this document:

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METHOD - 005

E2PROM WRITE/ERASE ENDURANCE AND DATA RETENTION TEST

1. PURPOSE

This test is intended to determine the ability of the memory cell of an E2PROM integrated circuit or an integrated circuit with an E2PROM module (such as a microprocessor) to sustain repeated data changes without failure and to retain data for the expected life of the E2PROM.

For write/erase endurance, a data change occurs when a stored "1" is changed to a "0", or when a stored "0" is changed to a "1". Endurance failures are caused predominantly by charge trapping occurring in the tunnel dielectric during write/erase cycles. Charge trapping failures are accelerated by hot temperature. Also, this test is intended to determine if the device can withstand constant temperature with an electrical bias applied.

Data retention is a measure of the ability of the floating gate of an E2PROM cell to retain charge in the absence of applied external bias. The failure criteria is a change of state of the E2PROM cell, commonly caused by dielectric defects resulting in charge loss. Failures of these dielectric defects are accelerated by high temperature bake stress.

This test does not replace other stress test qualification requirements.

2. APPARATUS

The apparatus required for this test shall consist of a controlled temperature chamber capable of maintaining the specified temperature conditions. Sockets or other mounting means shall be provided within the chamber so that reliable electrical contact can be made to the device terminals in the specified circuit configuration. Power supplies and biasing networks shall be capable of maintaining the specified operating conditions throughout the test. Also, the test circuitry should be designed so that the existence of abnormal or failed devices will not alter the specified conditions for other units on test. Care should be taken to avoid possible damage from transient voltage spikes or other conditions which might result in electrical, thermal or mechanical overstress.

3. PROCEDURE

It is preferred to run devices through the write/erase endurance followed by the data retention stresses using the same devices. However, for stand-alone E2PROMs, separate samplings for the write/erase endurance and data retention stresses are allowed.

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3.1 WRITE/ERASE ENDURANCE

a) Devices shall be placed in the chamber so there is no substantial obstruction to the flow of air across and around each unit. The power shall be applied and suitable checks made to assure that all devices are properly energized. When special mounting or heat sinking is required, the details shall be specified in the applicable device specification.

b) The data in the memory cells must be cycled continuously from "1" to "0" to "1" to "0" during the test to the maximum number of write/erase cycles specified in the applicable device specification. The specified number of write/erase cycles are to be performed at the maximum write/erase frequency and at the temperature specified in the device specification. All write and erase operations during the endurance test must be verified to have been properly executed.

c) Verification of functional testing to the device specification shall be performed per paragraph 3.4.

3.2 DATA RETENTION

a) After performing write/erase endurance as described in paragraph 3.1, the devices shall be programmed with an appropriate pattern as specified in the device specification. If the device specification does not indicate a required memory pattern, then program the samples with either a checkerboard pattern, where each bit is surrounded by it's complement, or with a pattern where all bits are programmed.

b) Perform pattern verification and full functional testing to the device specification, excluding any E^2PROM write/erase testing.

c) The units are subjected to high temperature storage life test (HTB) per Table 2 of the CDF-AEC-Q100 Specification at 150°C for 1000 hours. This could apply to stand-alone E^2PROM integrated circuits.

d) Perform pattern verification and full functional testing to the device specification.

3.3 PRECAUTIONS

Precautions shall be taken to ensure that no devices can be damaged by thermal runaway and to preclude electrical damage. The test setup should be monitored initially and at the conclusion of a test interval to establish that all devices are being stressed to the specified requirements. The bias voltages and currents on each device shall be noted and corrected prior to further temperature exposure. If a device is not biased properly when checked at the conclusion of a test interval, it must be determined if the device has changed or if the test circuit has changed so that the validity of the data for qualification can be established.

3.4 MEASUREMENTS

3.4.1 Electrical Measurements

The electrical measurements shall be made at intervals per the applicable device specification. Interim and final electrical measurements shall be completed within 48 hours after removal of the devices from the specified test conditions.

3.4.2 Required Measurements

The electrical measurements shall consist of parametric and functional tests specified in the applicable device specification.

3.4.3 Measurement Conditions

Before removing the devices from the chamber, the ambient temperature shall be returned to room temperature while maintaining the specified voltages on the devices. Testing at room (or cold temperature if required per the device specification) shall be performed prior to exposing to any high temperature.

4. FAILURE CRITERIA

A device is defined as a failure if the parametric limits are exceeded or if functionality cannot be demonstrated as specified on the device specification.

5. SUMMARY

The following details shall be specified in the applicable device specification and/or the supplier's internal stress test specification:

a) Special mounting, if applicable.
b) Test condition, alpha-numeric code.
c) Biasing conditions.
d) Measurements before, at intermediate test points, (if applicable) and after test.
e) The maximum number of logic transitions in the memory cell.
f) The period between write cycles.
g) Alternative Write/Erase procedures, requested by the E^2PROM manufacturer, to guarantee the endurance requirement. This proposal must be approved by the user.

Revision History

Rev #	Date of change	Brief summary listing affected paragraphs
-	June 9, 1994	Initial; Release
A	May 19,1995	Merged 005 and 006 into a single spec.

ATTACHMENT 6

AEC - Q100-006 REV-C

ELECTRO-THERMALLY INDUCED PARASITIC GATE LEAKAGE TEST

Acknowledgment

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Council would especially like to recognize the following significant contributors to the development of this document:

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Automotive Electronics Council
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Change Notification

The following summary details the changes incorporated into AEC-Q100-006 Rev-C:

- **Sections 3.4, 3.5.1 (step g), and 5.0: Added wording to reflect a change in the E-field requirement for Gate Leakage (GL) testing. Previous GL requirement of a ±700 volt E-field potential has been changed to a ±400 volt E-field potential.**

Automotive Electronics Council
Component Technical Committee

METHOD - 006

ELECTRO-THERMALLY INDUCED PARASITIC GATE LEAKAGE (GL) TEST

Text enhancements and differences made since the last revision of this document are shown as underlined areas. Several figures have also been revised, but changes to these areas have not been underlined.

1. SCOPE

1.1 Description

The purpose of this specification is to establish a reliable and repeatable procedure for determining surface mount integrated circuit susceptibility to Electro-Thermally Induced Parasitic Gate Leakage (GL). This specification may also be used as an evaluation tool for determining the susceptibility of circuit designs, molding compounds, fabrication processes, and post mold cure processes to GL.

1.2 Reference Documents

Not applicable.

1.3 Terms and Definitions

The terms used in this specification are defined as follows:

1.3.1 Device Failure

A condition in which a device does not meet all the requirements of the acceptance criteria, as specified in section 5, following the GL test.

1.3.2 DUT

An electronic device being evaluated for its sensitivity to GL.

1.3.3 Electro-Thermally Induced Parasitic Gate Leakage (GL)

A trapped-charge phenomenon affecting plastic encapsulated integrated circuits in varying degrees depending upon circuit design, fabrication technology, molding compound, and post mold cure profile. The phenomena occurs at high temperature when an electric field (E-field) is present. GL results in yield losses during high temperature processes, especially those with heated air flow (e.g., high temperature handling and IR reflow solder operations). The phenomena can be detected as an increase in Icc, input leakage, pin parametrics degradation, or functional failure. GL does not cause permanent damage and can be reversed by a 4 hour unbiased bake at a temperature of 125 °C (or 2 hours at 150 °C).

Chrysler	Date	Delphi Delco Electronics Systems	Date	Visteon Automotive Systems	Date
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Richard A. Chow - Wah		Gerald E. Servais		Douglas Sendelbach	

1.3.4 Electro-Thermally Induced Parasitic Gate Leakage (GL) Sensitivity

A GL level resulting in device failure. Sensitivity will vary depending upon the design, layout, process, and materials used.

2. EQUIPMENT

2.1 Test Apparatus

The apparatus required for this test consists of a GL test fixture, high voltage power supply, and thermal chamber. Figure 1 shows an equivalent test setup.

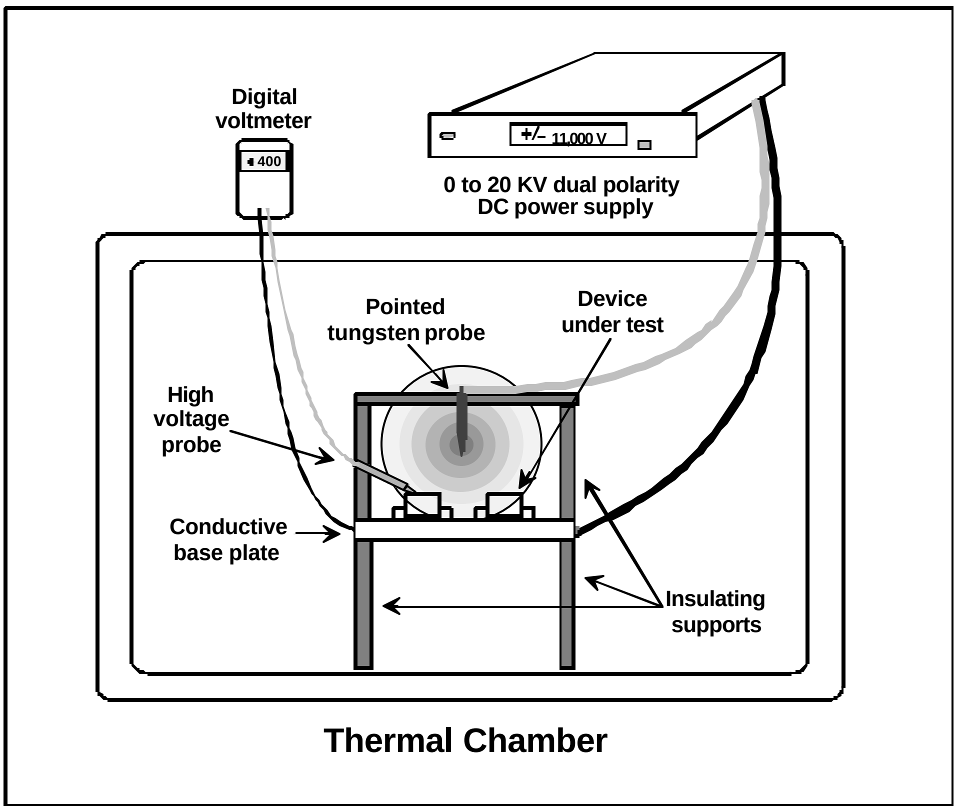

Figure 1: GL test fixture and set-up

2.1.1 GL Test Fixture

A test fixture as illustrated in Figure 1 and Appendix A. Other equivalent test fixture configurations may be used, but the actual fixture must meet the following requirements:

1. The tungsten probe must be at a height of 2.5 ± 0.5 inches above the conductive base plate surface and allow for vertical movement to facilitate voltage adjustment.

2. To ensure consistent test results, all test devices must be able to be repeatably placed with leads in contact with the conductive base plate surface by using milled recesses or equivalent markings and shall be equidistant from the high voltage tungsten probe.

2.1.2 High Voltage Power Supply

A high voltage DC power supply capable of generating 20,000 volts at both positive (+) and negative (-) polarities.

2.1.3 Thermal Chamber

An oven (Thermotron oven Model 51.C-B or equivalent) capable of controlled heating to a temperature of 155 °C and having adequate space to accommodate the GL test fixture.

2.2 Measurement Equipment

Equipment shall include a digital voltmeter and high voltage probe to verify conformance of the GL test fixture and resulting electric field (E-field) to the requirements of this document as specified in Figure 2, section 3.4, and Appendix A.

2.2.1 Digital Voltmeter

Digital voltmeter capable of accurately measuring 0 to 20,000 volts DC with a minimum sensitivity of ± 1 mV.

2.2.2 High Voltage Probe

High voltage probe capable of accurately measuring 0 to 20,000 volts DC with input resistance of 1000 MΩ and ± 2% accuracy (Fluke Model 80 K-40 or equivalent).

3. TEST PROCEDURE

3.1 Sample Size

A total of six (6) devices shall be evaluated for GL sensitivity: a sample of three (3) devices shall be stressed at a positive (+) GL exposure and a new sample of three (3) devices shall be stressed at a negative (-) GL exposure. The use of a new sample group of three (3) devices for each GL exposure polarity is required. Test samples must be representative of the normal process for deliverable devices; samples shall not be subjected to any additional testing or preconditioning (e.g., burn-in, etc.). Devices used for GL testing shall be discarded and shall not be retested or considered as deliverable product. GL is typically a non-destructive phenomena; however, the process of GL testing and the post-test bake, used to verify recovery, often results in changes to the molding compound and/or lead solderability characteristics rendering the devices unsatisfactory for shipment.

3.2 Test Temperature

Each sample group shall be subjected to a GL exposure at 155 °C.

3.3 Measurements

Prior to GL testing, complete initial DC parametric and functional testing (initial ATE verification) shall be performed per applicable device specification. If the applicable part drawing specifies an allowable parametric shift as failure criteria, a data log of each device shall be made listing the applicable parameter measurement values (e.g., supply current, pin leakages, etc.). The data log will be compared to the parameters measured during final ATE verification to determine the failure criteria of section 4.

3.4 GL Stress Conditions

Each sample shall be subjected to an E-field voltage potential of positive (+) or negative (-) 400 volts. A new sample of three (3) devices shall be used for each E-field voltage polarity.

3.5 Detailed Procedure

3.5.1 Fixture preparation

a. Place the GL test fixture in the thermal chamber and verify both are at room temperature (see Figure 1 and Appendix A).

b Ensure the high voltage power supply is OFF and connect the positive lead to the high voltage tungsten probe. Set the height of the tungsten probe to a level of 2.5 ± 0.5 inches above the conductive base plate surface.

c. Connect the negative lead of the high voltage power supply to the conductive base plate.

d. Place a setup device in the fixture (located where the actual test samples will be placed) such that the device leads are in contact with the conductive base plate surface.

e. Make sure the voltage control is set to the minimum level. Turn the high voltage power supply to the ON position.

f. Place the positive lead of the high voltage probe at the center of, and in direct contact with, the top surface of the setup device. Connect the negative lead of the high voltage probe to the conductive base plate. The high voltage probe body should extend at a 45° ± 5° angle away from the conductive base plate surface (as depicted in Figure 2). This angle is critical to the measuring of the E-field voltage potential. As the high voltage probe body is raised (exceeding the 45° angle requirement) or lowered (falling below the 45° angle requirement), the measured E-field voltage potential will vary significantly.

g. Monitor the setup device's E-field voltage potential using the digital voltmeter. Adjust the voltage setting on the high voltage power supply to provide a positive (+) 400 volt E-field voltage potential, or negative (-) 400 volt E-field voltage potential depending on the desired GL exposure, measured at the center of the setup device's top surface.

h. Turn the high voltage power supply switch to the OFF position.

i. Verify that the high voltage power supply is at zero (0) volts before touching the GL test fixture.

j. Remove the setup device from the GL test fixture.

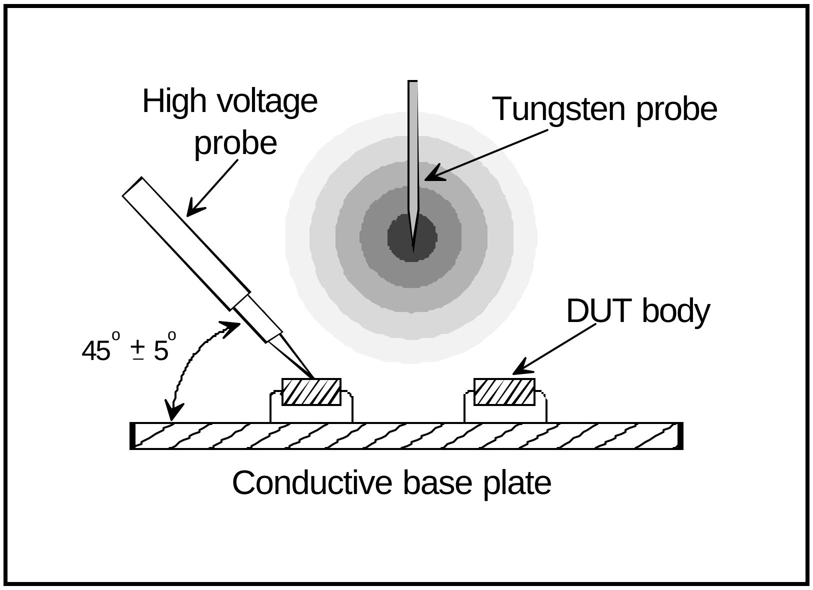

Figure 2: Measurement angle used to monitor E-field voltage

3.5.2 Detailed Test Procedure

a. Ensure the high voltage power supply is OFF. Place a sample group of three (3) devices in the GL test fixture such that the device leads are in contact with the conductive base plate surface. All devices must be at the same distance from the high voltage tungsten probe as the setup device used in section 3.5.1.

b. Set the thermal chamber temperature to 155 °C. The use of a thermocouple placed in direct contact with the GL test fixture conductive base plate surface may be used to monitor the temperature of the sample group devices.

c. Verify the test sample devices are at the specified temperature. Allow the test fixture and sample group of three (3) devices to stabilize at the specified temperature for 15 minutes.

d. Turn the high voltage power supply switch to the ON position.

e. Allow the devices and GL test fixture (with the E Field voltage applied) to soak for a 2 minute dwell time as indicated in Figure 3.

f. After 2 minutes of the total dwell time have elapsed, begin reducing the thermal chamber temperature to 100 °C or less with the E-field voltage still applied. This can be accomplished by opening the thermal chamber door while the circulating fans are operating. Thermal chamber heating and cooling times will vary and a longer ramp-down time may be required when reducing the thermal chamber temperature. The total ramp-down time (155 °C to 100 °C) shall not exceed 10 minutes (see Figure 3).

g. Once the sample group of three (3) devices reaches a temperature of 100 °C, turn the high voltage power supply switch to the OFF position. A thermocouple placed in direct contact with the GL test fixture conductive base plate surface may be used to monitor the temperature of the sample group devices.

h. Verify the high voltage power supply is at zero (0) volts before touching the GL test fixture.

i. After cooling to room temperature, remove the sample group of three (3) devices from the GL test fixture.

j. Submit the devices for complete DC parametric and functional testing (final ATE verification) per applicable device specification within 96 hours of GL exposure and determine whether the devices meets the acceptance criteria requirements specified in section 5. The storage temperature between GL exposure and final ATE verification shall not exceed 30 °C.

k. Subject all failing devices to an unbiased bake of 4 hours at a temperature of 125 °C (or 2 hours at 150 °C) and then submit for complete DC parametric and functional testing (ATE re-verification). GL failures will always recover when subjected to a 4 hour unbiased bake at 125 °C (or 2 hours at 150 °C). If the failing devices do not recover following the unbiased bake, then the devices may have been damaged (due to handling, EOS, ESD, etc.). Failing devices that do not recover shall be eliminated from the GL data.

l. Record pass/fail and any other pertinent observations for each device.

m. Reverse the high voltage power supply polarity, verify the E-field voltage potential (as specified in section 3.5.1), and repeat steps (a) through (l) above using a new sample group of three (3) devices.

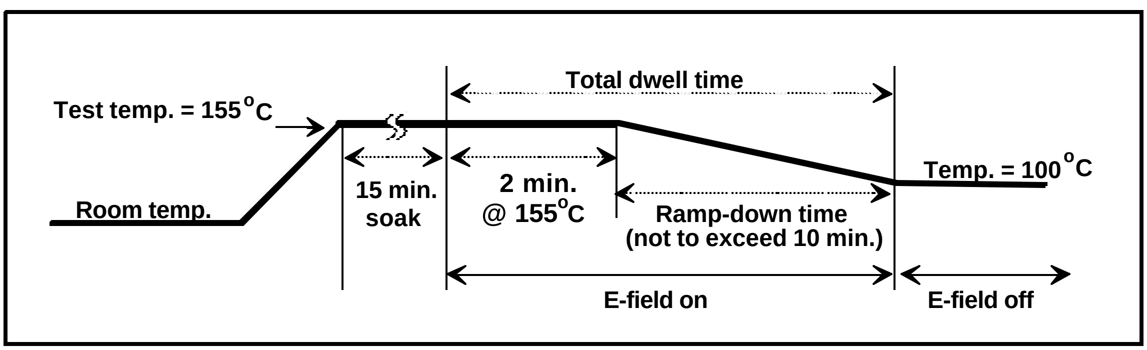

Figure 3: Dwell time and ramp-down time for GL test.

4. FAILURE CRITERIA

A device will be defined as a failure if, after exposure to GL, the device fails any of the following criteria:

1. The device exceeds the allowable shift value. Specific parameters and allowable shift values shall be as defined in the applicable device specification. During initial ATE verification, a data log shall be made for each device listing the applicable parameter measurement values. The data log will be compared to the parameters measured during final ATE verification to determine the shift value. Devices exceeding the allowable shift value will be defined as a failure.

2. The device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification.

5. ACCEPTANCE CRITERIA

A device passes a GL exposure level if all devices in the sample group stressed at that GL level pass. All the devices and sample groups used must pass the measurement requirements specified in section 3 and the failure criteria requirements specified in section 4 following both positive (+) and negative (-) 400 volt E-field exposures in order for the devices to be considered acceptable.

Appendix A

(suggested GL test fixture)

This appendix provides suggested general construction features of the GL test fixture. Other equivalent test fixture configurations may be used, but the actual fixture must meet the requirements of section 2.1.1. The dimensions shown are approximate and are not critical to the test fixture construction. Figures A1 through A5 illustrate the GL test fixture assembly and major components.

Note:
Attach High Voltage Warning Label to test fixture

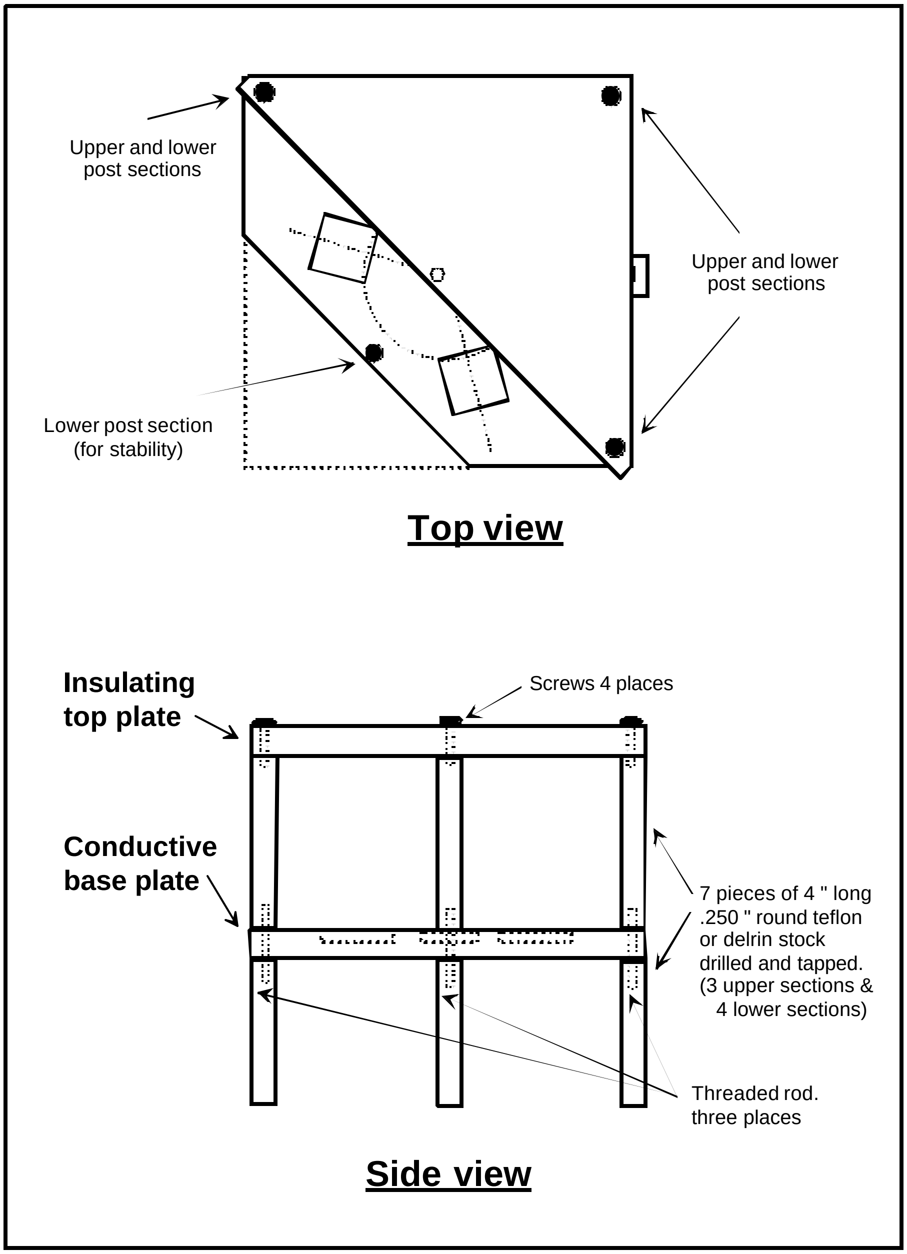

Figure A1: GL test fixture assembly

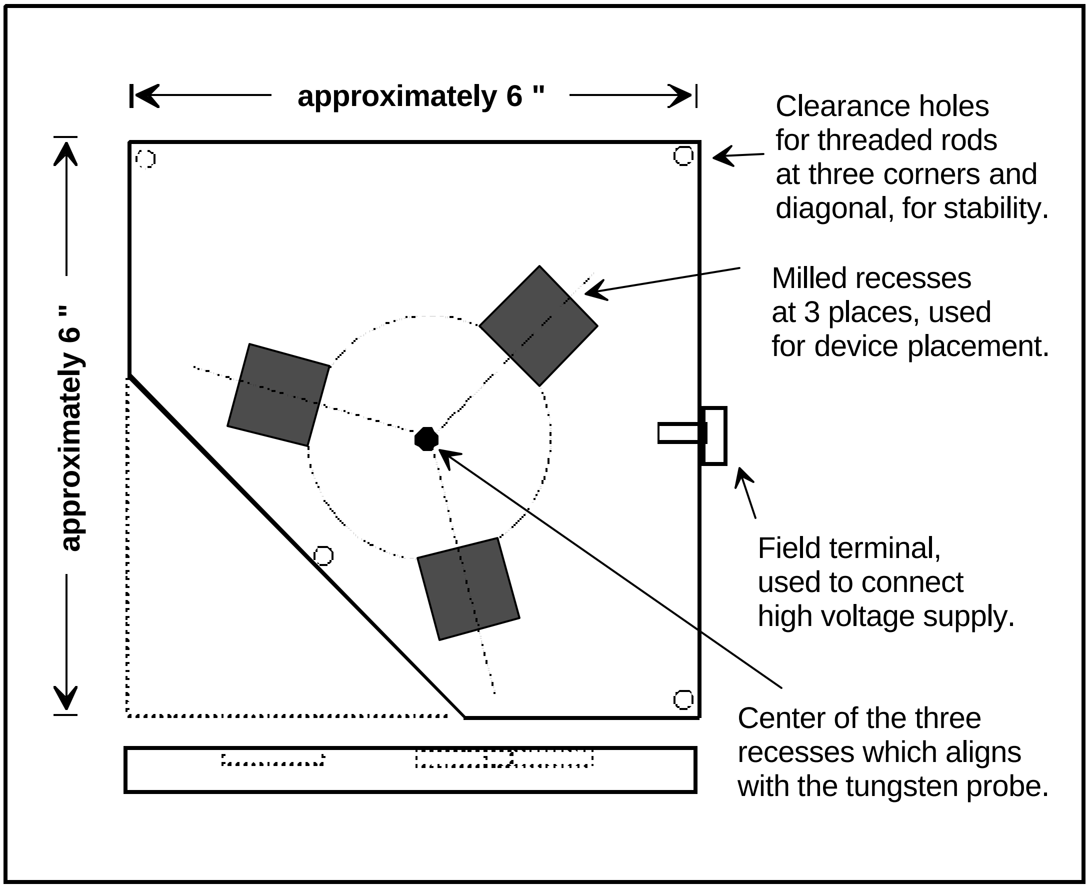

Figure A2: Conductive base plate

The base plate is constructed from electrically conductive material (e.g., .125 - .250 inch aluminum stock). The plate is approximately 6 inches square and serves to support and locate the devices under test and as one pole of the test voltage. Milled recesses may be used for repeatable device placement during GL testing (see Figures A1 and A2). The suggested recesses may be milled directly into the plate to ensure consistent device placement and orientation with respect to the tungsten probe center-line. The recesses, large enough to accommodate the largest device to be tested, are located 120 degrees apart and equidistant from the center of the base plate. The absolute distance from center (approximately one inch) is not critical.

The lower left hand corner (dashed line section) is cut off on a diagonal to facilitate device handling and to reduce thermal mass. A lower post section, or leg, is added to the diagonal side for stability (see Figure A1).

Note: The aluminum plate should be alodine coated for protection against corrosion and to retain electrical quality.

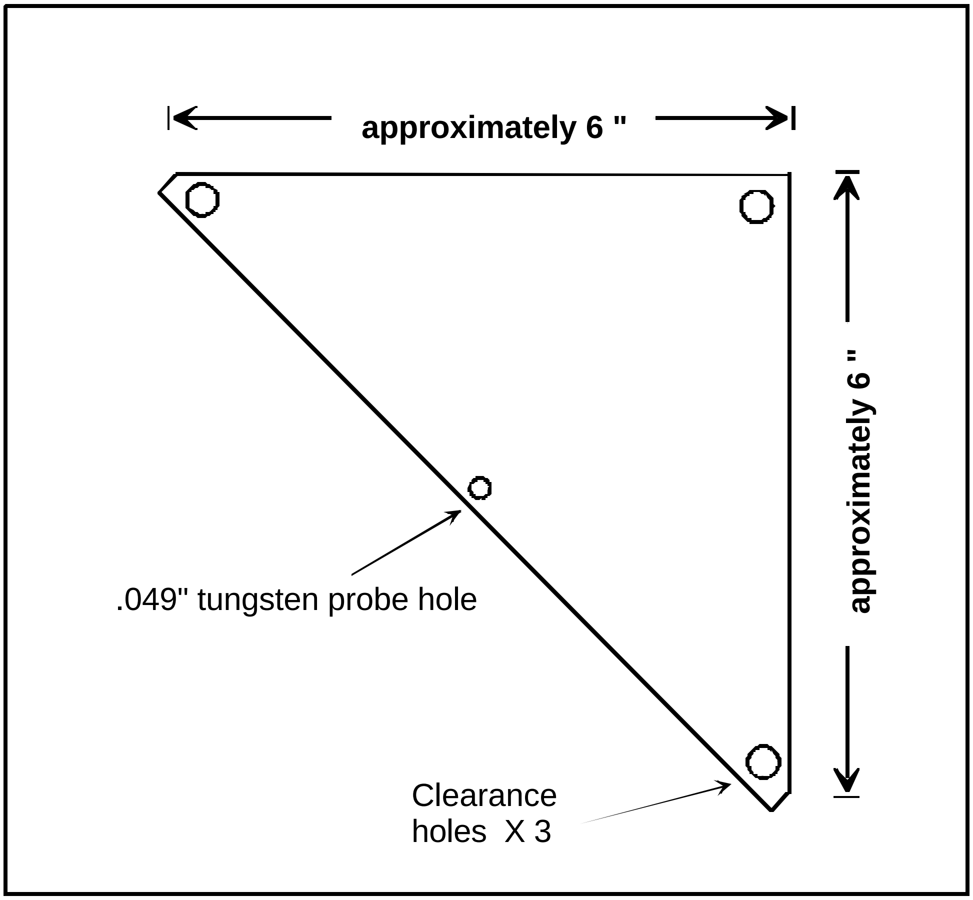

Figure A3: Top insulating plate.

The top insulating plate serves to support and locate the tungsten probe at the center of the GL test fixture. It establishes and maintains the probe to device distance during set-up and test. The top plate is fabricated from a triangular piece of .250 inch Teflon, Delrin, or other insulating material which is capable of withstanding an environment of 200 °C and ± 20,000 volts.

A .049 inch diameter hole, used to position the tungsten probe, is centered on the diagonal side so as to be directly above the base plate center point after assembly. Clearance holes are drilled at each corner for assembly screws.

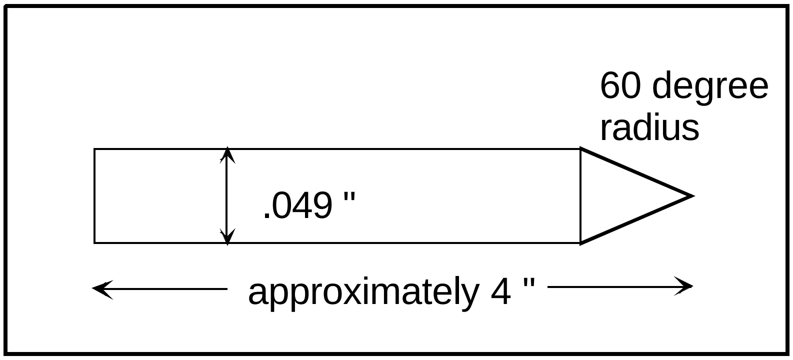

Figure A4: Tungsten probe

Grind a 60 degree point on a 4 inch length of 0.049 inch diameter tungsten wire (or a diameter of tungsten wire that is readily available; the diameter of the wire is not critical). This will provide an E-field potential at the specified test voltage, as measured on the top surface of the device approximately 2 inches from the tungsten probe point.

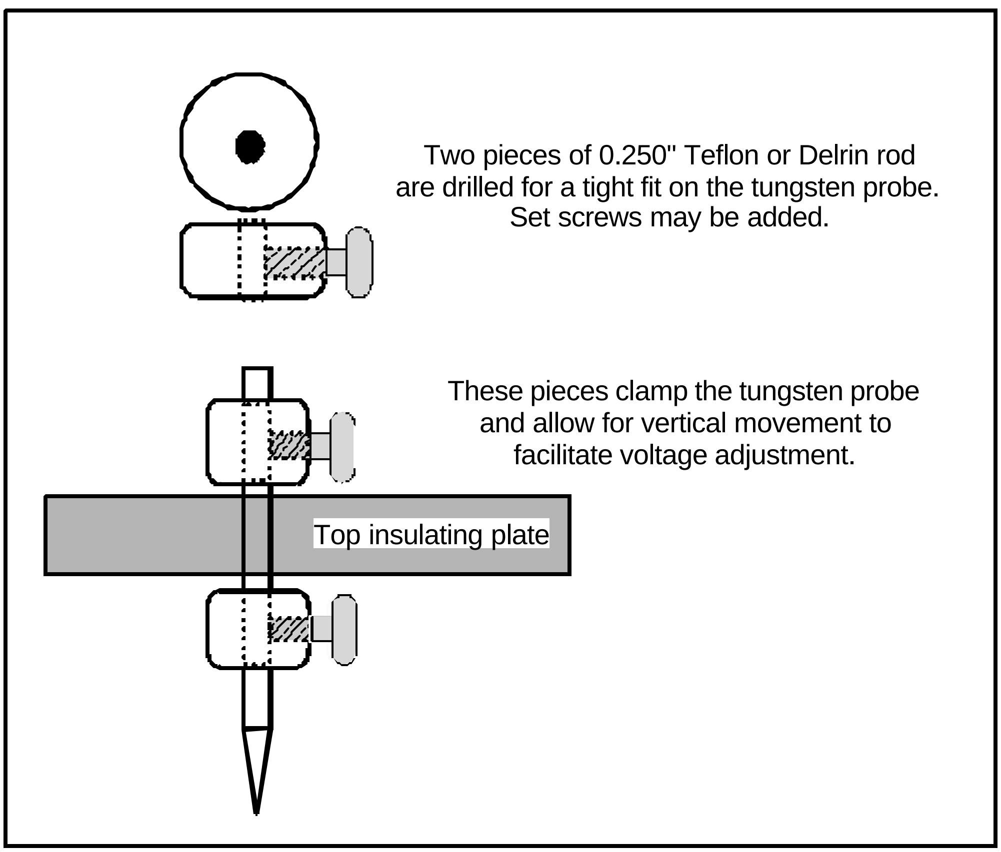

Figure A5: Tungsten probe clamping mechanism.

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Revision History

Rev #	Date of change	Brief summary listing affected sections
-	June 9, 1994	Initial Release
A	May 15, 1995	Added Copyright statement. Revised the following: Foreword; Sections 2.1.2, 3.1, 3.2.2 (d, f, and g), and 3.2.3 (a, b, c, f, g, and l); Figures 1, 2, and 3; Appendix A.
B	Sept. 6, 1996	Deleted old Sections 1.3.3, 1.3.4, 1.3.5, 1.3.6, 1.3.7, 2.1.1, 3.1, 3.2.1, 3.3, 3.4, 3.5, and 3.6. Added new Sections 1.3.1, 1.3.4, 2.2, 2.2.1, 2.2.2, 3.1, 3.2, 3.3, 3.4, and 5.0. Revised the following: Sections 1.1, 1.3, 1.3.2, 1.3.3, 2.1, 2.1.1, 2.1.2, 3.5.1 (a, e, f, g, h, and i), 3.5.2 (a, b, c, e, f, g, h, i, j, k, l, and m), 4.0, and Appendix A; Figures 1, 2, 3, A1, and A2.
C	Oct. 8, 1998	Revised the following: Sections 3.4, 3.5.1 (g), 5; Figure 1. Revisions reflect a change in E-field requirement from ±700 volt to ±400 volt.

ATTACHMENT 7

AEC - Q100-007

FAULT SIMULATION AND TEST GRADING

Acknowledgment

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Council would especially like to recognize the following significant contributors to the development of this document:

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Automotive Electronics Council
Component Technical Committee

METHOD - 007

FAULT SIMULATION AND TEST GRADING

1. PURPOSE

This test method defines test grading procedure and specifies a level to which the manufacturing test program for the device under test must detect faults. Parametric failures are not covered. Another term for test grading is fault simulation. Test grading applies to all digital circuits including the digital portion of mixed signal and linear circuits. Test grading does not apply to the linear portion of the circuits.

Also, this document covers modeling and logic simulation requirements; the assumed fault model and fault simulation requirements; and the procedure that must be followed to evaluate and report fault coverage.

2. PROCEDURE

2.1 Simulation

Simulation is an imitative process used to study relationships between parameters which interact in a Integrated Circuit. The simulator must support at least zero (0), one (1) and unknown (X) logic states. In addition, the simulator must support appropriate “strengths” to enable correct modeling of logic based upon the target technology and design practices.

Simulation employs model which are replica accurate enough to imitate the behavior of the circuit. Integrated circuit can be described at several levels of abstraction:

Behavioral Model - At this level the integrated circuit is described in terms of the algorithm that it performs.
Functional Model - This model describe the flow of data and control signals within and between the functional blocks. These blocks are made of latches, registers, and elements of similar level of complexity.
Logical Model - This model describes a circuit as an interconnection of switching elements (gates and flip-flops) and is also referred to as gate or structural model.
Switch-Level Model - It describes the logical behavior of metal oxide semiconductor circuit. A switch-level model consists of nodes connected by transistors and is also referred to as transistor model.

2.1.1 Simulation Model

A simulation model of the fault free device shall be constructed. Modeling of the device shall be at the Boolean gate level (Logical Model) and include all inputs and outputs. Modeling at the transistor level is allowable. Modeling at the register level is permissible if each register model is analyzed at the internal Boolean gate or transistor level for stuck-at-one and stuck-at-zero fault coverage with the test sequence applied to the external register nodes.

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analyzed at the internal Boolean gate or transistor level for stuck-at-one and stuck-at-zero fault coverage with the test sequence applied to the external register nodes.

2.1.2 Simulation Data Base

The data base used for simulation shall include all gates internal to the device, including memory portions, analog sections, and high impedance buffers to the input/output pins. Behavioral models will be only allowed to model the functionality of RAMs, ROMs, EPROMs, EEPROMs, and analog sections of design. Behavioral models on other modules may be used as long as the module under consideration for fault grading is modeled at the gate level.

2.2 Fault Simulation

Fault simulation is used to measure the effectiveness of a defined ordered set of input test vectors to detect a specified set of modeled faults in a device under test. The only relevant fault models considered in this document are discussed next.

2.2.1 Single Stuck-at Fault Model

A fault is defined as a single, stuck-at one (SA1) or stuck-at-zero (SA0) condition. A fault model is constructed by injecting a fault at time zero (steady-state) into the fault-free simulation. An input stuck-at fault is assumed isolated from any other fanout branches that emanate from the output which drives the input under consideration (see figure 2.1).

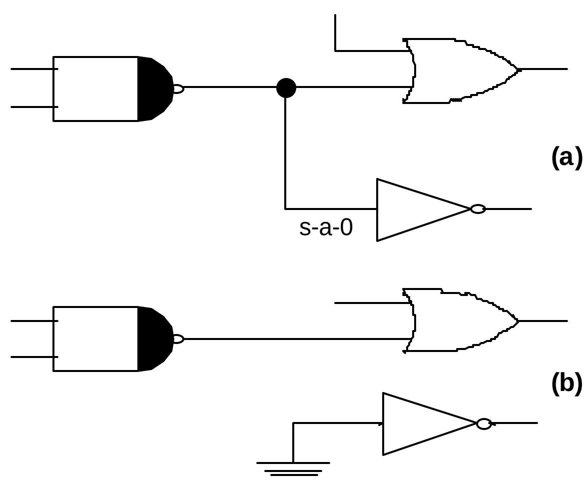


Figure 2.1 (a) fan Out logic. (b) Same logic with s-a-0

Two fault models shall be constructed for each gate input and each gate output, one is simulating each fault type (SA1 and SA0). Each of these fault models must be tested for fault detection.

2.2.2 Functional Fault Model

Functional fault models are used to model defects at a level of abstraction which is much higher than in single stuck-at fault model. Such models should be used only for those parts of designs for which a behavioral model is used.

2.3 Fault Detection

2.3.1 Initial Condition

At the start of fault simulation, the state of every logic line and components containing memory must be X. Any other initial condition, including explicit initialization of any line or memory element to 0 or 1 must be justified and documented. If the same initialization is done in every instance of a specific model, then it is sufficient to document the initialization once. It must, however, be stated that all instances of the model were affected.

2.3.2 Test Sequence

The device test sequence shall be introduced into the fault model and the propagation of signals simulated. The fault shall be steady state, not intermittent in nature, and not include shorts between signals.

2.3.3 Fault Detection

A fault is detected when a logical difference of values at a device output (between a zero and a one) exists between the fault-free model and the fault model. This difference is the result of the induced stuck-at condition.

2.3.4 Fault List

A fault list which refers to the set of all the modeled faults in a circuit must be generated in a deterministic approach. Statistical sampling of modeled faults is not permissible.

2.4 Documentation of Simulator / Tester Differences

Any differences in format or timing of the test vector sequence, between that used by the fault simulator and that applied by the tester, shall be documented in the fault simulation report.

2.5 Modularized Designs

Designs that may be modularized and tested independently of each other, may be test graded separately and may not need to be redone for each design variation, as long as the test pattern for each module is always the graded pattern and each input and output is available when faults are scored.

3. MEASUREMENTS

3.1 Undetectable Faults

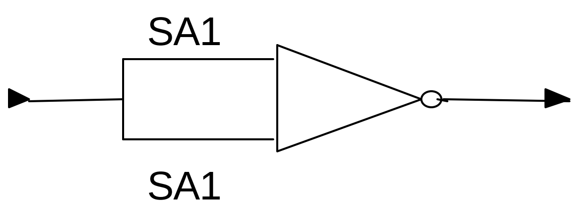
Undetectable faults are those faults which exist in the model and the actual circuit but cannot be verified by propagation to an observable output. Undetectable gate input and output faults may exist in logic circuits and are generally caused by redundancies and internal logic states which are not obtainable. Undetectable faults fall into several categories which should be considered and automatically removed from the fault list at an early state of test grading, when possible. This type of undetectable fault should not reduce the percent of faults detected and should be removed from the total number of faults. Some undetectable faults that could be removed follow, other faults must be considered on a case-by-case basis.

3.1.1 Redundant Logic

If a design contains logical redundancy, the faults associated with the redundant logic are truly undetectable and can be deleted from the fault list. However, it is desirable that the design be modified to remove the redundancy if it is unintentional. We would like to emphasize that in this section we are concerned with true logic redundancy and not the type of redundancy that is often employed to improve circuit performance.

3.1.2. Parallel Gate Inputs

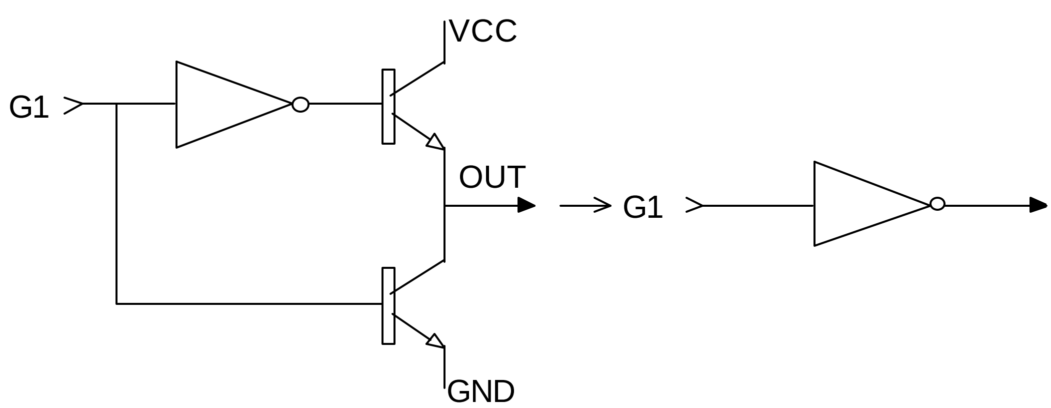
Undetectable fault due to parallel gate inputs may be subtracted from the total number of faults.



(SA1) ON BOTH INPUTS IS UNDETECTABLE

3.1.3 Push-Pull Configurations

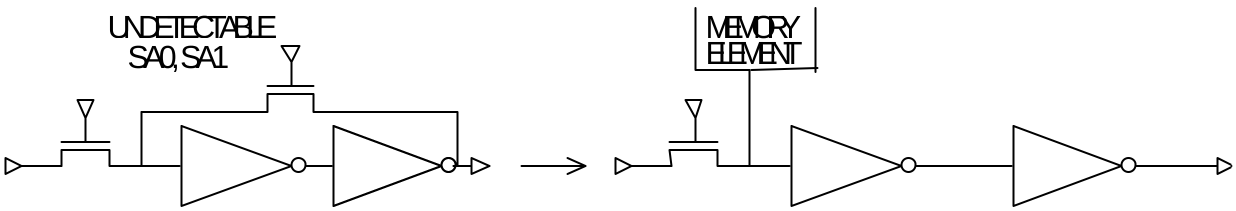
Undetectable faults in a push-pull configuration may be subtracted from the total number of faults or the configuration may be modeled as a buffer or inverter.



PUSH PULL EXAMPLE EQUIVALENT MODEL

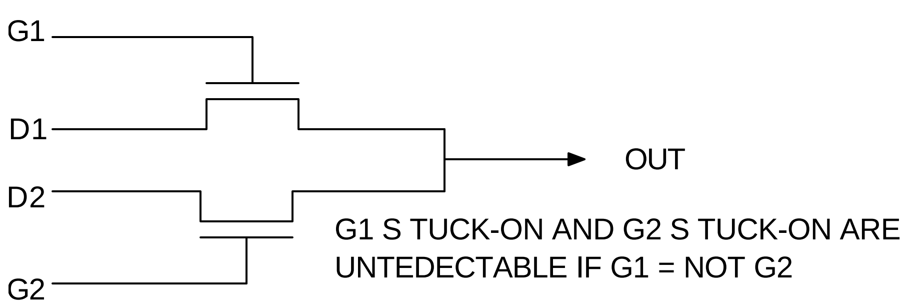
3.1.4 Memory Configuration

Undetectable faults in a memory configuration may be subtracted from the total number of faults or the memory configuration may be modeled as a functional memory element.



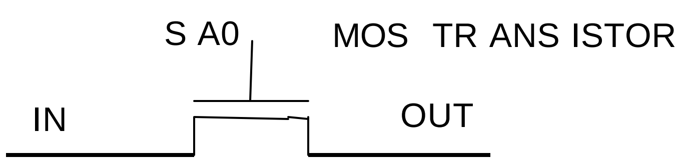
3.1.5 Wired Junction Configuration

Undetectable faults in a wired junction configuration with no dominance may be removed from the total number of faults. However, in many wired junction configurations all stuck-at faults are detectable and are required to be counted in the total number of faults graded.



3.1.6 Implied Faults

If a fault exists on an internal node which cannot be initialized to a known value, but the fault collapses into another dominant fault which can be detected, then the fault is considered detected by implication. Implied faults must be analyzed on a case-by-case basis.



CONTROL SA0 WILL BE DETECTED IF (OUT) SA0 AND SA1 FAULTS ARE DETECTED
WHEN NO OTHER SOURCES FAN-IN TO SIGNAL OUT (IMPLIED FAULT DETECTION)

3.1.7 Control line Faults

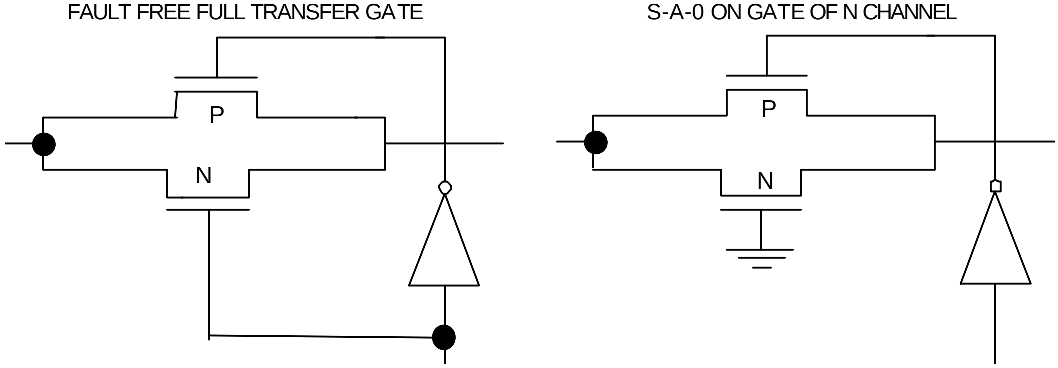
In the absence of initialization circuitry, a fault on a control line will cause the output of the component to be at X. An example is s-a-0 or s-a-1 fault on the Clk input of a D flip-flop which has no set and reset inputs. Therefore, the control line fault can at best be potentially detected. However, if both s-a-0 and s-a-1 faults on the data input are detected, the two faults on the control line can be counted as detected if the X at the output is assumed to be a permanent 0 or a permanent 1. We allow this assumption and require that such faults be documented as having been detected by implication.

DFF EXAMPLE WITHOUT SET OR RESET

CLK faults will be detected if SA0 and SA1 faults are detected on D or Q

3.1.8 TYPE2 Circuit Configurations

The inability of present fault simulators to simulate circuit (in addition to logic) fault effects causes them to report a significant class of faults as undetected (TYPE2, circuit fault effect). An example of this category of faults is illustrated below. A s-a-0 fault on the gate of N transistor has no effect on logic state transmission through the transfer gate despite the N transistor remaining off. Simulation of the parametric effects of the threshold drop are beyond the capabilities of present fault simulators.



Circuit Fault Effect

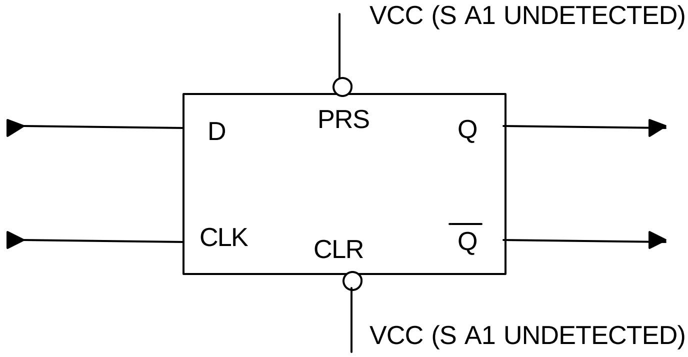
It should be noted that such faults are not necessarily undetectable in the device under test, otherwise at least part of the logic involving these faults could have been deleted from the actual design. However, such faults can not be detected by observing stuck at fault effects, and parametric testing (speed dc drive, etc.) is necessary for covering such faults. It is therefore acceptable to exclude such faults from the fault list because the fault coverage definition pertains to stuck at faults only. A separate measure is used to quantify the coverage of TYPE2 faults by parametric / at-speed tests included in production vectors.

3.2 Deleted Faults

Deleted faults are those which exist in the model, but cannot exist in the actual circuit, or are indistinguishable in the faulty model from the fault-free model.

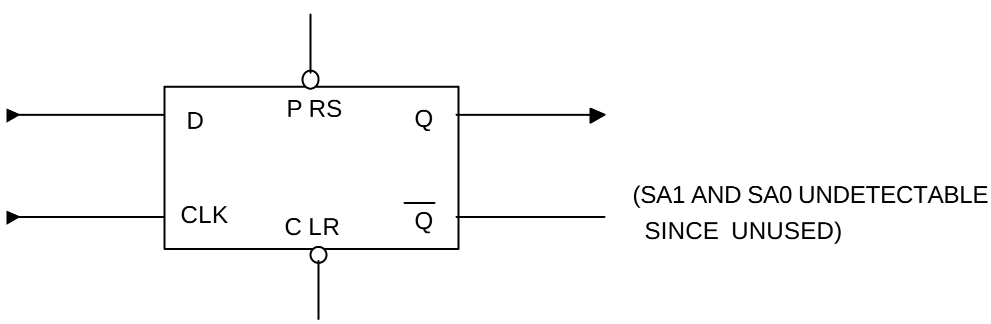
3.2.1 Power Supply and Ground Faults

Stuck-at-one on the power supply and stuck-at-zero on ground faults may be included in deleted faults and removed before or during test grading verification.



3.2.2 Unused Outputs

Unused outputs on any higher level module (flip-flop, counter, etc.) when used to model the actual circuit may be considered as deleted faults and removed from the fault list.



3.3 RAM and ROM Faults

3.3.1 ROM Faults

Read-only-memory is considered fully verified when all locations are read and faults occurring during read out may be propagated to an observable output.

3.3.2 RAM Faults

Random-access-memory is considered fully verified when each location can be detected in a stuck-at-one or stuck-at-zero condition and the address decode circuitry has been fully exercised with faults propagated to an observable output.

3.3.3 Additional RAM and ROM Tests

It should be realized that additional tests for RAM and ROM elements are generally required to detect topological and parametric faults.

3.3.4 Previously Graded Designs

Previously graded designs with only ROM code changes do not require regrading of the entire device as long as the ROM code, in either design, is not utilized in test grading other portions of the circuitry.

3.4 Fault collapsing

A VLSI circuit has a large number of possible faults, one cannot individually test such a large number of faults economically. To facilitate testing, the concept of fault equivalence and dominance is allowed to be used. Fault equivalence and dominance allow us to combine many faults into a single set and a single test vector can detect these faults. The process of reducing the total number of possible faults into a minimal number of necessary faults is called fault collapsing.

3.5 Potentially Detected Faults

A modeled fault is considered potentially detected if during application of the test vectors, a primary output value in the fault-free logic model is a 0 or 1 at a specific simulation time, but goes to X in the corresponding faulted logic model at the same simulation time. A fault which is potentially detected at least 10 times can be considered a detected fault. This is based upon the assumption that the X value will be opposite of the fault-free logic model value at least once if it occurs 10 times or more during the application of test vectors. Most fault simulators allow the user to set a threshold value for this purpose, which must be set to at least 10.

3.6 Fault Coverage

3.6.1 Percent of Faults Detected

The percent of faults detected, or test grade, is equal to the total number of faults detected divided by the total number of possible faults minus undetectable faults, deleted faults, and TYPE2 faults.

$$\text{Fault Coverage (\% Detected)} = \frac{\text{Total \# detected faults}}{\text{Total \# possible} - \text{\# Undetectable} - \text{\# Deleted} - \text{\# TYPE2}} \times 100\%$$

$$\text{Total \# possible} = 2^* (\text{Total \# gate inputs} + \text{Total \# gate outputs})$$

3.6.2 TYPE2 Fault Coverage

Fault Coverage for TYPE2 Faults is determined based upon analyses done outside of the fault simulation environment. Circuit simulation, timing analysis, and experimentation with actual parts may be employed to determine parametric tests for various TYPE2 faults. The various cases of TYPE2 circuit fault effects and a description of the general testing conditions which will be applied to the device that may cause the TYPE2 faults to be detected should be reported per section 5.

3.6.3 Coverage Reporting

Interim fault coverage reporting may be based on a collapsed fault list. The final reported fault coverage however, shall be in terms of the total number of faults in the fault list, not the collapsed fault list.

3.6.4 Algorithm Derived Test Vectors

If an established test algorithm is used to derive test vectors for parts of designs for which a behavioral model is used, the established fault coverage must be reported. References and other relevant material must be documented in support of the effectiveness of the algorithm used. If an established test algorithm is customized or a new test algorithm is developed, its effectiveness must be proved and the fault coverage (so established) should be reported. If a behavioral model contains sub-block(s) which are modeled at structural level (such as decoding logic associated with RAM partitions), justification must be provided in the fault simulation report as to how the stuck-at faults in the embedded structural logic are covered by the test algorithm that was used.

3.6.5 Automatic Test Pattern Generation / Scan Testing

Automatic Test Pattern Generation (ATPG) and/or scan testing may be used to supplement the functional test patterns, and the fault coverage of such testing should be similarly established as in 3.6.4 above. Test patterns entirely based on ATPG and/or Scan methods are not acceptable.

4. ACCEPTANCE CRITERIA

4.1 Statistical Sampling

Statistical sampling of modeled faults is not permissible.

4.2 Qualification Test Requirements

Devices submitted for qualification and approval must be tested using a vector set with stuck at fault coverage greater than or equal to 90% for parts of designs for which a logic model is used. A list of all undetected faults along with plans for improvement must be submitted.

4.2.1 Production Test

The fault coverage of the production test set used for all parts delivered for production must be greater than or equal to 98% if no Iddq testing is employed.

4.2.2 Production Test With Iddq

If acceptable Iddq testing (per Appendix 1) is included in the production test set, the required stuck-at fault coverage for production must be equal to or greater than 95%.

4.2.3 Production Test With Targeted Iddq

If Iddq testing was developed in such a way that undetected stuck-at faults are targeted by selection of Iddq vectors in the production test set, the required stuck-at fault coverage for production must be equal to or greater than 90% and the combined coverage equal to or greater than 95%.

4.3 Production Test TYPE2 Coverage

The fault coverage for TYPE2 faults should be as high as possible in the production test. If this coverage is not 100%, the reasons should be documented and agreed upon prior to delivery of parts for production.

4.4 Test Sequence Alterations

Following the acceptance of test grading, no alternations in the test sequence will be allowed. However, additional tests will be permitted. Should an alternation be required, a new test grading must be performed on the entire test sequence. Also, for every revision of the design the acceptable fault coverage level must be re-established because some of the previously successful tests may get invalidated due to design modifications. Should the supplier have sufficient means to preclude an entire 're-grade' following a change, those results must be provided to the User prior to production deliveries.

4.5 User Audits

The User reserves the right to audit the results of test grading.

4.6 Failure to Meet Production Fault Coverage

If the production fault coverage requirement can not be met, the supplier must submit a full report to the User for approval, explaining the reasons that the requirement can not be meet.

5. DOCUMENTATION

The documentation delivered must include the following in the specified order:

a) Statement of fault coverage which include percent fault coverage, the number of faults detected, the total number of faults, the deleted faults, and the undetectable faults.
b) Breakdown of fault simulation results by logic blocks per a top level description showing:
    1. equitably distributed fault coverage
    2. where behaviorally modeled logic used
c) Description of logic and fault simulation tool used
d) Potential fault detection threshold used (10)
e) Description of faults considered TYPE2 including their analysis and appropriate explanation of the coverage for TYPE2 faults
f) Details of fault coverage (cite references) by Built-In-Self-Test methodologies, if any used

g) Detail any differences in format or timing of the test vector sequence, between that used by the fault simulator and that applied by the tester
h) Iddq transistor-level coverage for the selected Iddq vector subset, if used, and the distribution of measured Iddq values and the upper acceptance limit.

Appendix #1

Iddq Testing

If the supplier elects to use Iddq testing, the following applies:

1. A team consisting of design, product, and reliability engineers shall review the test vectors and select a set of Iddq vectors which provide a minimum of 70% transistor-level coverage (TLC), based upon their best engineering assessment. In all cases, this shall not be less than ten test vectors, unless it can be demonstrated that greater than 90% coverage can be achieved with less than ten test vectors.
2. The test program will be modified to pause on these selected vectors and record the total current from the positive supplies. The current from any analog supplies must not be included in this measurement. Although the IC's clock has been paused during these Iddq test vectors, integrity of the IC's internal data and its outputs shall not be compromised. Iddq readings must also allow for the IC to settle into its quiescent mode.
3. For production material and production-intent material for qualification, the failure criteria shall be calculated from matrix material used for electrical characterization, or the first three qualification lots. For each matrix cell (excluding cells with intentional Leff variation) a minimum of twelve functional devices shall be selected and their Iddq values recorded. This data will then be statistically analyzed for its mean and standard deviation, assuming a normal distribution unless the data suggests otherwise. The upper Iddq acceptance criteria shall be the mean plus seven standard deviations or less.
4. At any time during the product's lifetime, the supplier may submit distribution information, reliability data, and failure analysis supporting a change to the Iddq test limit.
5. Iddq testing may be more effective if employed after a voltage stress test. Any such test combination (voltage stress and Iddq) must have the Iddq test following the voltage stress.
6. Iddq tests will be run at the maximum operating power supply voltage in the electrical specification.
7. All parts shipped for manufacturing shall have Iddq testing included in the wafer test or final test programs. Only room temperature testing is required.

Revision History

Rev #	Date of change	Brief summary listing affected paragraphs
-	Sept. 1996	Initial Release

ATTACHMENT 8

AEC - Q100-008 INITIAL RELEASE

EARLY LIFE FAILURE RATE (ELFR)

Acknowledgment

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Automotive Electronics Council
Component Technical Committee

METHOD - 008

Early Life Failure Rate (ELFR)

1 SCOPE

This test method is applicable to all IC part qualifications. In the case of many parts generic data (see Q100, 2.3) may fulfill the requirements of this test method. If the supplier is qualifying a part for which no generic data is available (unproven technology or design rules) for general usage then the requirements of this test method should be utilized to meet the requirements of Q100. If the supplier is qualifying a part for a single user, that user may optionally designate the implementation of AEC-Q001 as a substitute for ELFR. All parts used for such a qualification must have been evaluated to Q001 tests and limits approved by the user. If AEC-Q001 is utilized the user shall review and approve of the particular tests and the method used to determine test limits. (Note: The failures from ELFR and Q001 do not always show a 1 for 1 correlation.)

1.1 Description:

This specification establishes the testing method for evaluation of early life failure characteristics on parts that are utilizing new or unproven processing technology or design rules where generic data is not available. This would include parts for which there is no prior usage information or generic data. Unsatisfactory results in this evaluation indicate that corrective action is required and the parts may require processing changes, design changes, burn-in, more aggressive burn-in or application of statistical part test limits, see AEC - Q001.

2 REFERENCE DOCUMENTS

1. AEC - Q001 Guidelines For Part Average Testing
2. JESD22-A108 Bias Life

3 PROCEDURE

3.1 Sample Size

The sample size shall be per Table 1 of Q100. In the case of parts that are deemed too expensive, the requirement for use of this test method and the sample size will be based upon agreement between the user and supplier.

3.2 General ELFR Procedure

The parts shall be tested per the High-Temperature Operating Life (HTOL) requirements in

Chrysler	date	Delphi Delco Electronics Systems	date	Visteon Automotive Systems	date
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JESD22-A108 with the following special condition. The ambient test temperature and duration shall be as follows:

48 hours at 125°C or 24 hours at 150°C.

3.3 Acceptance Criteria

The parts shall be electrically tested within 48 hours after completion of high temperature exposure. Testing shall be at room temperature followed by high temperature. Failures during this test are not acceptable and indicate that corrective action must be taken. The supplier shall notify all interested users of this non-conforming condition and the corrective action which has / will take place. The user(s) must approve of the corrective action for the part to be qualified.

3.4 Sample Disposition

Parts which pass electrical testing after this test can be used to populate other non-operating tests. These parts can also be supplied as productive material if agreed to by the user.

Revision History

Rev #	Date of change	Brief summary listing affected sections
-	October 8, 1998	Initial release

ATTACHMENT 9

AEC - Q100-009

ELECTRICAL DISTRIBUTION ASSESSMENT

Acknowledgment

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Council would especially like to recognize the following significant contributors to the development of this document:

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Automotive Electronics Council
Component Technical Committee

METHOD - 009

ELECTRICAL DISTRIBUTIONS ASSESSMENT

1. SCOPE

This specification describes test methods for assessing electrical parameter characterization, distributions (to AC, DC and timing etc.) and parametric shifts of integrated circuits. The results are used to determine the capability to meet the performance requirements of the device specification and as defined in Q100 (Ppk, Cpk, etc.). The results can also be used to set device test limits (LTL and UTL).

2. PURPOSE

The purpose of this test method is to define methods for obtaining characterization, electrical distribution and parametric shift data for electrical parameters on integrated circuits. The intent of this method is to assess the part's capability to function within the specification parameters over normal process variations, time, and application environment (operating temperature range, voltage etc.).

3. DEFINITIONS

3.1 Characterization

The statistical distribution of electrical parameters when one or more processing limits are taken to their process control extremes. The purpose of this procedure is to determine the functional robustness (the effect of one parameter on another, etc.) of the part. These parameters usually involve measurement of electrical parameters with the device at operating extremes with respect to voltage, frequency and temperature, but could also include various loading conditions and other inputted AC and DC parameters.

3.2 Electrical Distribution

The statistical distribution of an electrical parameter taken from a random sample of parts in a normal production population (i.e. wafer lots) at a given temperature, frequency and voltage for the purpose of determining the capability of the part meeting the application parametric requirements.

3.3 Lower Test Limit (LTL)

Lower test limit is tighter than the lower spec limit (LSL) to guardband for measurement error.

3.4 Parametric Drift

The change of an electrical parameter from it's original value because of time and environmental conditions. The form of the change may be a shift from the original value of a

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Richard A. Chow - Wah	9/28/98	Gerald E. Servais	10/1/98	Douglas Sendelbach	9/25/98

device or in the statistical distribution of a group of devices. When changes are to be studied on individual device basis the study is called Parametric Drift of individuals (serialization of individual units is required). When changes are studied on a group of devices the study is referred to as Parametric Drift of distributions (serialization of individual units is not required). The cause of the change may be time and/or environmental conditions (during real life application or as simulated by accelerated stress testing).

3.5 Upper Test Limit (UTL)

Upper test limit is tighter than the upper spec limit (USL) to guardband for measurement error.

4. PROCEDURE

4.1 Requirements

The performance of Electrical Distributions for each user part qualification is required by Q100. The use of generic data is not allowed. The performance of Characterization and Parametric Drift is not required but should be available based on the suppliers own evaluations or determined by mutual agreement between the user and supplier based on need.

4.2 Parameters

The supplier is not required to perform Electrical Distributions on every electrical parameter detailed in the supplier's data sheet. The parameters tested should be those whose variation may impact outgoing quality and/or reliability, or those essential to the successful operation of the device. This list of parameters is usually called key electrical parameters. This list of parameters may be established by the supplier based on knowledge of the technology, process and design or could be negotiated between the user and supplier, usually through a user device specification.

4.3 Procedure

4.3.1 Sample Size

Select a random set of parts from a given population, the sample size of which is specified in AEC-Q100. These parts must come from the production process and be manufactured on production tooling, with all processing as product to be delivered to the user (i.e. Burn In if used etc.). If parametric drift is to be determined on individuals, serialize each part. This will enable determining the absolute part-specific drift as well as the sample (Distribution) drift.

4.3.2 Testing of Samples

Run these parts through the production tester using a program that enables variables data to be taken on each part or a group of parts for each parameter. Begin the first run at room temperature, with subsequent runs at hot and cold temperature extremes as detailed in the device specification. If Characterization is to be performed, repeat this step as many times as there are changed parameters.

Note: Before testing samples the standard deviation of the measurement error shall be determined. At least 20 parts shall be tested at least twice per tester per temperature to estimate the standard deviation of the measurement (stdevm) error.

4.3.3 Data Analysis

Once the data is collected, it should be tabulated in a format where capability can be easily analyzed. The data fields should include parameter, mean, standard deviation, minimum and maximum values, minimum and maximum specification limits, and Ppk for each temperature. The supplier has the option of including the detailed part data in any report to the user, but the data should be available upon request.

The software DE Histogram (Q001 - Appendix 3) is recommended so that all values will be calculated using the same statistics.

4.3.4 Setting LTL and UTL

The LTL and UTL maybe arrived at as follows:

LTL = LSL + 3(stdevm)
UTL = USL – 3(stdevm)
where stdevm = the standard deviation of the measurement error.

4.3.5 Parametric Drift Testing

If Parametric Drift is to be performed, repeat the above steps after stress testing (usually HTOL) is completed on the parts under consideration (If the study is on individuals on the serialized parts).

5. FAILURE CRITERIA

A parameter is deemed incapable if it fails the requirements of the device specification or the acceptance criteria for the test in Q100.

For any electrical parameters that do not meet the Ppk requirements detailed in Q100 versus the agreed specification limits, the supplier is required to develop a containment and corrective action (e.g. redesign) to address the discrepancy, then verify the fix through retesting.

6. SUMMARY

The following details shall be specified in the applicable procurement document:

1) The type of study, characterization, Electrical Distributions, Parametric shift (individuals or distributions)
2) List of Key electrical parameters as agreed upon by the user and supplier.
3) minimum and maximum operating voltages.
4) minimum and maximum operating frequencies or at the specified frequency of the IC.
5) hot, room and cold temperatures.

Revision History

Rev #	Date of change	Brief summary listing affected sections
-	October 8, 1998	Initial release

ATTACHMENT 10

AEC - Q100-010

SOLDER BALL SHEAR TEST

Acknowledgment

Any document involving a complex technology brings together material and skills from many sources. The Automotive Electronics Council would especially like to recognize the following significant contributors to the development of this revision of this document:

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Automotive Electronics Council
Component Technical Committee

METHOD – 010

SOLDER BALL SHEAR TEST

1. SCOPE

This test method is applicable to all solder ball surface mounted packages (PBGA, Chip Scale, and Micro Lead Frame) except flip chip.

2. Purpose

The purpose of this test method is to define the procedure for measuring the shear strength of the interface between the barrier metal and solder ball. This method also establishes the minimum shear strength requirements for this interface.

3. Procedure

3.1 Solder Ball Shear Test Procedure

Solder ball shear shall be used to quantify the integrity of the solder connection to the barrier metallization on the device. Prior to shear testing, the test samples shall be thermally preconditioned. The balls for shear testing shall be chosen randomly throughout the test unit.

3.1.1 Ball Shear Test Procedure

The following procedure shall be used for this test:

1. Place the test samples on a clean circuit board or ceramic coupon positioned with the solder ball side up. Thermally precondition the devices with a minimum of two reflows using convection or IR reflow with a peak temperature of 220 +5 /–0°C and a reflow profile as defined in J-STD-020 (moisture exposure is not required).
2. Allow samples to cool to room temperature (22 ± 3°C).
3. Mount the samples on a shear tester, with the shear arm positioned at a height of approximately 1/3 of the ball height and not touching the surface of the substrate, see Figure 1, shear the balls using a constant shear rate of 0.28 to 0.50 mm/sec. Record the shear strength.
4. Using a microscope with a minimum 40X magnification, examine and record the ball separation mode, see Table 1.

DaimlerChrysler	date	Delphi Delco Electronics Systems	date	Visteon Corporation	date
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Peter Voetsch		Gerald E. Servais		William Giffen	

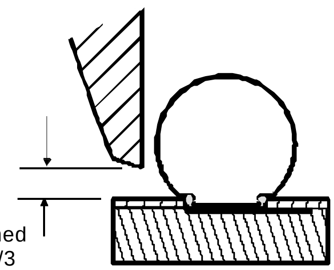


Figure 1 Arm Position During Solder Ball Shearing

4. Failure Criteria

The following failure criteria are not valid for devices that have undergone stress testing (beyond thermal preconditioning) or been desoldered from an assembly.

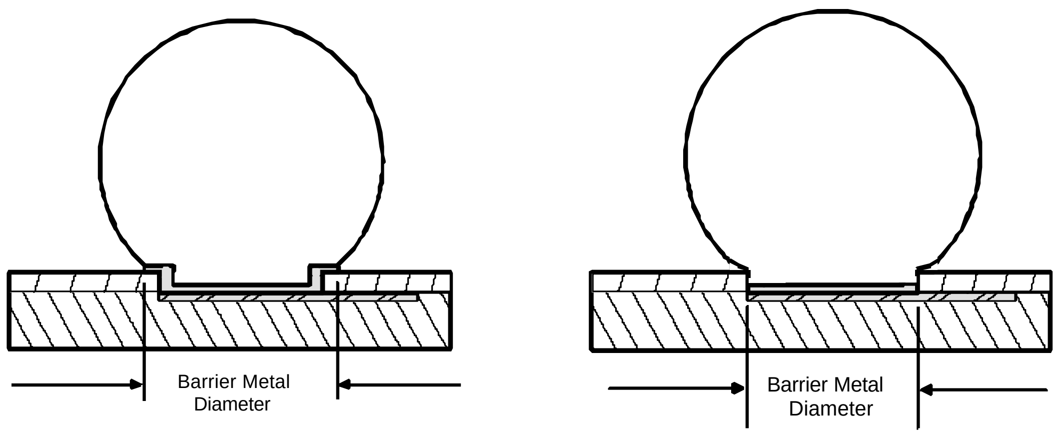
4.1 Solder Ball Shear Acceptance Criteria

The solder ball shear strength shall be 3200 grams/mm^2 minimum (see Table 2) ***in conjunction with acceptable separation modes***. Separation modes are defined in Table 1. Separation modes 1 and 4 are acceptable. Separation modes 2 shall not exceed 5% of the shear interface. Separation mode 3 and 5 are not acceptable. Evidence that the shear arm has contacted the substrate during the shearing process invalids the ball shear value for that ball.

Table 1 Definition of Solder Ball Separation Modes

Separation Mode Designation	Separation Mode Definition
1	Separation occurs through the bulk solder. Characterized by solder remaining on entire solder pad.
2	Separation occurs as a fracture through the metal to metal brittle intermetallic layer (typically through the nickel-tin or gold-tin intermetallic). The pad typically appears flat in these areas.
3	Separation occurs between the barrier metal layers under the bump (typically as a loss of adhesion between the copper and nickel). The pad typically appears flat in these areas.
4	Separation occurs in the PBGA substrate material beneath the solder pad causing the pad to rip out or peel from the substrate. The solder ball remains attached to the pad.
5	Separation with the bulk of the solder separating from the solder pad, but with the plating remaining on the solder pad. This condition is typically due to improper wetting.

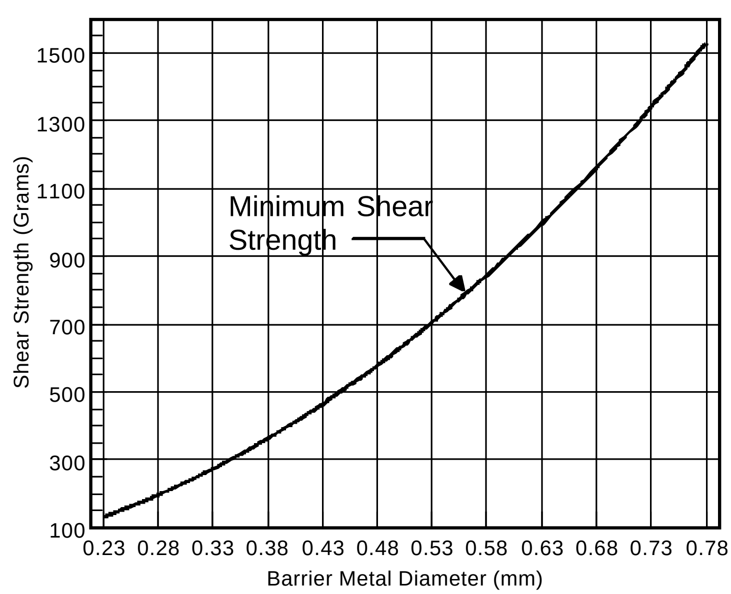
Table 2 Solder Ball Shear Strength



Solder Ball Barrier Metal Diameter

Solder Ball Barrier Metal Diameter

Barrier Metal Diameter (mm)	Ball Shear Minimum Strength (grams)
0.23	133
0.28	197
0.33	274
0.38	363
0.43	465
0.48	579
0.53	706
0.58	845
0.63	998
0.68	1162
0.73	1339
0.78	1529



Revision History

Rev #	Date of change	Brief summary listing affected sections
-	Aug. 25, 2000	Initial release

Automotive Electronics Council
Component Technical Committee

ATTACHMENT 11

AEC - Q100-011 Rev A

CHARGED DEVICE MODEL

ELECTROSTATIC DISCHARGE TEST

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Automotive Electronics Council
Component Technical Committee

METHOD – 011

CHARGED DEVICE MODEL (CDM) ELECTROSTATIC DISCHARGE (ESD) TEST

CHANGES THAT HAVE OCCURRED IN THIS REVISION ARE DOUBLE UNDERLINED

It is anticipated that a future revision of Q100 will adopt Q100-011 Charged Device Model (CDM) as a replacement for Q100-003 Machine Model (MM) ESD. Suppliers capable of performing Q100-011 CDM may adopt this change now.

1. SCOPE

1.1 Description

The purpose of this specification is to establish a reliable and repeatable procedure for determining the CDM ESD sensitivity for electronic devices. This test method does not include socketed CDM.

1.2 Reference Documents

ESD Association Specification ESD-STM5.3.1-1999
JEDEC Specification EIA/JESD22/C101

1.3 Terms and Definitions

The terms used in this specification are defined as follows.

1.3.1 Charged Device Model (CDM) ESD

An ESD pulse meeting the waveform criteria specified in this test method, approximating an ESD event that occurs when a device becomes charged (e.g., triboelectric) and discharges to a conductive object or surface.

1.3.2 Device Failure

A condition in which a device does not meet all the requirements of the acceptance criteria, as specified in section 5, following the ESD test.

DaimlerChrysler	date	Delphi Delco Electronics Systems	date	Visteon Corporation	date
Peter Voetsch	1/18/01	Gerald E. Servais	1/09/01	William Giffen	1/19/01

1.3.3 Device Under Test (DUT)

An electronic device being evaluated for its sensitivity to ESD.

1.3.4 Electrostatic Discharge (ESD)

The transfer of electrostatic charge between bodies at different electrostatic potentials.

1.3.5 Electrostatic Discharge Sensitivity

An ESD voltage level resulting in device failure.

1.3.6 ESD Simulator

An instrument that simulates the charged device model ESD pulse as defined in this specification.

1.3.7 Pin Under Test (PUT)

The pin under test; this includes all power supply and ground pins.

1.3.8 Withstanding Voltage

The ESD voltage level at which, and below, the device is determined to pass the failure criteria requirements specified in section 4.

2. EQUIPMENT

2.1 Test Apparatus

The apparatus for this test consists of an ESD pulse simulator; Figure 1 shows a typical equivalent CDM ESD circuit. Other equivalent circuits may be used, but the actual simulator must be capable of supplying pulses that meet the waveform requirements of Table 2, Table 3, and Figure 3.

2.2 Measurement Equipment

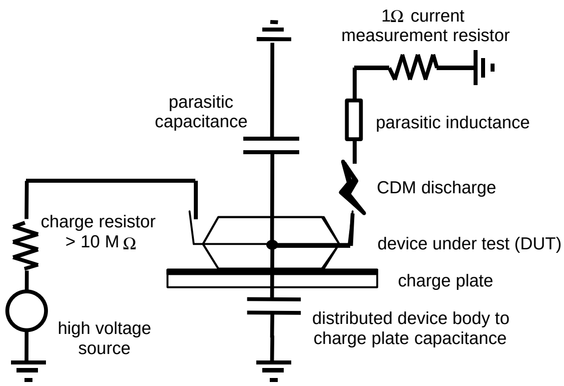
Equipment shall include an oscilloscope/digitizer, current probe, attenuators, and cable/connector assemblies to verify conformance of the simulator output pulse to the requirements of this document as specified in Table 2, Table 3, and Figure 3.

2.2.1 Oscilloscope/Digitizer

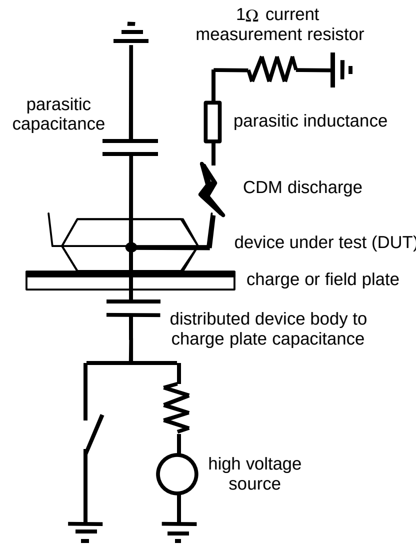
The oscilloscope/digitizer shall have a minimum bandwidth of 1.0GHz and nominal input impedance of 50Ω (Tektronix SCD1000, HP 7104, or equivalent).

2.2.2 Current Probe

The current probe shall be an inductive current transducer or coaxial resistive probe with a minimum bandwidth of 5GHz.



(a) Direct charge CDM



(b) Field induced charge CDM

Note: Parasitics in the charge and discharge path of the test equipment can greatly affect test results.

Figure 1: Charged Device Model ESD typical equivalent circuit for (a) direct charge and (b) field induced charge

2.2.3 Attenuator

The attentuator, if required, shall be high precision (+0.1dB precision at 1.0GHz) with impedance of 50Ω.

2.2.4 Cable/Connector Assembly

The cable/connector assembly, if required, shall be low loss (less than 0.4dB loss up to 1GHz) with impedance of 50Ω.

2.2.5 Verification Modules

The two verification modules shall be gold-plated or nickel-plated etched copper disks on single sided FR-4 material (thickness = 0.8mm). The disks shall be: 1) a small disk (diameter approximately = 9 mm) configuration with a capacitance value of 4pF ±5% measured at 1MHz, and 2) a large disk (diameter approximately = 26mm) configuration with a capacitance of 30pF ±5% measured at 1MHz. Each disk shall be created using an etching process and centered on FR-4 material measuring at least 30mm by 30mm. Capacitance shall be measured with the non-metallized and non-disk side of the verification module in direct contact with the metal surface of a ground plane. Verification module parameters and illustrations are shown in Table 1 and Figure 2.

Table 1: Verification module parameters

Verification Module	Parameter	Accepted Value
4pF	Capacitance	3.8pF to 4.2pF
	Disk diameter	~ 9mm
	FR-4 material size	≥ 30mm by 30mm
	FR-4 thickness	0.8mm
30pF	Capacitance	28.5pF to 31.5pF
	Disk diameter	~ 26mm
	FR-4 material size	≥ 30mm by 30mm
	FR-4 thickness	0.8mm

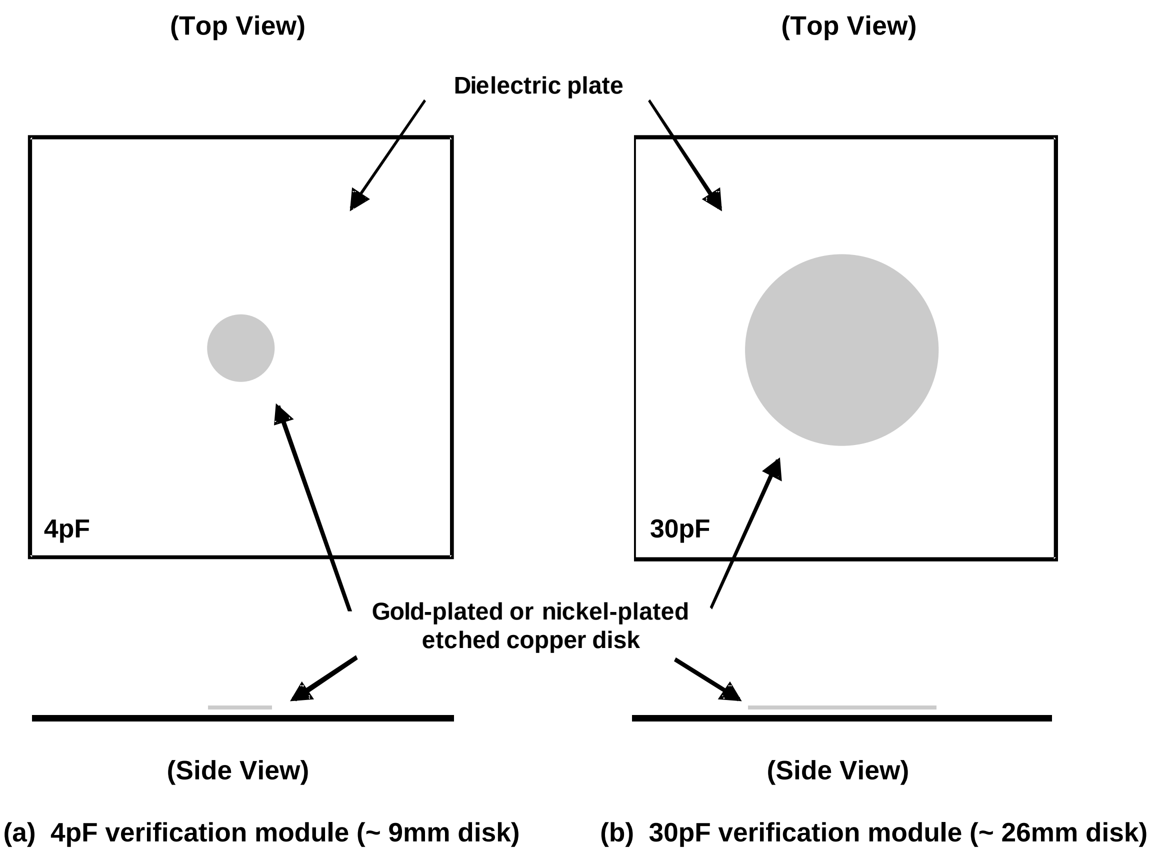


Figure 2: Verification module illustrations, (a) 4pF and (b) 30pF

2.2.6 Capacitance Meter

The capacitance meter shall have a resolution of 0.2pF when measured at 1.0MHz with 3% accuracy.

2.3 Equipment Calibration and Qualification

All peripheral equipment (including but not limited to the oscilloscope/digitizer, current probe, attenuators, cable/connector assemblies, verification modules, and capacitance meter) shall be periodically calibrated according to manufacturer's recommendations. A period of one (1) year is the maximum permissible time between full calibration tests. Qualification of the CDM simulator must be performed during initial acceptance testing or after repairs to the equipment that may affect the waveform. The simulator must meet the requirements of Table 2 and Figure 3 for five (5) consecutive waveforms at all voltage levels using the 4pF verification module shown in Figure 2. Simulators not capable of producing the maximum voltage level shown in Table 2 shall be qualified to the highest voltage level possible. The simulator must also meet the requirements of Table 3 and Figure 3 for five (5) consecutive waveforms at the 500 volt level using the 30pF verification module shown in Figure 2. Thereafter, the test equipment shall be periodically qualified as described above; a period of one (1) year is the maximum permissible time between full qualification tests.

2.4 Verification Module Calibration

The capacitance value of verification modules can be dramatically degraded by excessive use (indentations due to repetitive pogo pin contact, cracks in metallization, warping, etc.). Therefore, to ensure proper capacitance values, it is recommended that module capacitance be verified per section 2.4.1. When modules are degraded to the point they no longer meet the specified capacitance requirements shown in Table 1, they must be replaced.

2.4.1 Verification Module Capacitance Measurement Procedure

a. Using the 4pF verification module, place the non-metallic side of the module in direct contact with the metallic surface of a ground plane. Capacitance measurements can be affected by air gaps between the module and the ground plane (e.g., due to warping of the FR-4 material, etc.). Therefore, the air space between the module and the ground plane must be minimized. This can be accomplished by applying slight pressure using the capacitance meter probes; care must be taken to avoid damaging the disk metallization.

b. Using the capacitance meter defined in section 2.2.6, measure the capacitance of the verification module to the ground plane. The capacitance value shall meet the requirements defined in Table 1.

c. Repeat steps (a) and (b) using the 30pF verification module.

2.5 Simulator Waveform Verification

The performance of the simulator can be dramatically degraded by parasitics in the discharge path. Therefore, to ensure proper simulation and repeatable ESD results, it is recommended that waveform performance be verified using the 4pF verification module. The waveform verification shall be performed prior to performing CDM testing. If at any time the waveforms do not meet the requirements of Table 2 and Figure 3 at the 500 volt level, the testing shall be halted until waveforms are in compliance.

2.5.1 Waveform Verification Procedure

a. Prior to performing waveform verification, verification modules and tester components (e.g., pogo pin, charge plate, etc.) must be cleaned with isoproponal (isopropyl alcohol) using a procedure approved by the user's internal safety organization. Once clean, avoid direct skin contact. If handling is required, the use of vacuum tweezers or personnel finger cots is strongly recommended.

b. Place the 4pF verification module in direct contact with the charge plate of the CDM simulator. If a dielectric film is used during device testing, it shall be less than 130 microns thick and must be in place during the waveform verification procedure.

c. Set the horizontal time scale of the oscilloscope at 0.5 nanoseconds per division or less.

d. Raise the charge plate potential to positive 500 volts. With the discharge pin centered within the 4pF metallic disk, bring the discharge pin in direct contact with the verification module and initiate a discharge.

e. Measure and record the rise time, first peak current, second peak current, third peak current, and full width at half height. All parameters must meet the limits specified in Table 2 and Figure 3.

f. Raise the charge plate potential to negative 500 volts. With the discharge pin centered within the 4pF metallic disk, bring the discharge pin in direct contact with the verification module and initiate a discharge.

g. Measure and record the rise time, first peak current, second peak current, third peak current, and full width at half height. All parameters must meet the limits specified in Table 2 and Figure 3.

Table 2: CDM Waveform Specification for 4pF Verification Module

Voltage Level (V)	1st peak current for 4pF I_{p1}(A) (±20%)	2nd peak current for 4pF I_{p2} (A)	3rd peak current for 4pF I_{p3} (A)	Rise Time t_r (ps)	Full width at half height for 4pF FW_{hh} (ps)
250	2.25	< 50% of I_{p1}	< 25% of I_{p1}	< 400	< 600
500	4.50	< 50% of I_{p1}	< 25% of I_{p1}	< 400	< 600
1000	9.00	< 50% of I_{p1}	< 25% of I_{p1}	< 400	< 600
2000	18.00	< 50% of I_{p1}	< 25% of I_{p1}	< 400	< 600

Table 3: CDM Waveform Specification for 30pF Verification Module

Voltage Level (V)	1st peak current for 30pF * Ip1 (A) (±20%)	2nd peak current for 30pF * Ip2 (A)	3rd peak current for 30pF * Ip3 (A)	Rise Time tr for 30pF * (ps)	Full width at half height for 30pF * FWhh (ps)
500	14.00	< 50% of Ip1	< 25% of Ip1	< 400	≤ 1000

- **The 30pF verification module is used only during Equipment Qualification as specified in section 2.3.**

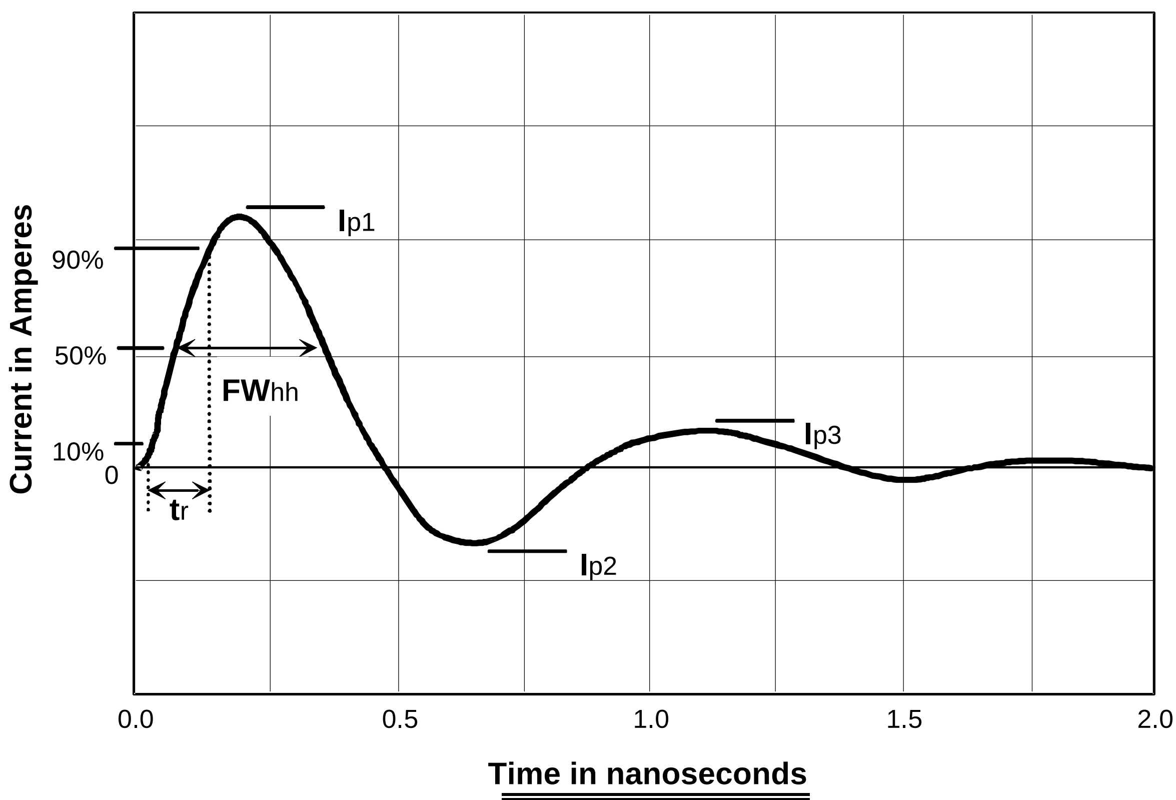


Figure 3: Typical CDM current waveform

3. PROCEDURE

3.1 Sample Size

Each sample group shall be composed of three (3) units. Each sample group shall be stressed at one (1) voltage level. It is permitted to use the same sample group for the next higher stress voltage level if all devices in a sample group meet the acceptance criteria requirements specified in section 5 after exposure to a specified voltage level. Therefore, the minimum number of devices required for ESD qualification is three (3) devices, while the maximum number of devices depends on the number of voltage steps required to achieve the maximum withstanding voltage. For example, a device with a maximum withstanding voltage of 500 volts requires 2 voltage steps of 250 volts each and 3 devices per voltage level for a maximum total of 6 devices.

Maximum # of devices = (# of voltage steps required) X 3 devices

3.2 Charging and Discharging methods

There are two acceptable methods of charging a DUT: Direct Charging and Field-induced Charging. Either method may be used to perform CDM ESD testing and must be recorded. While several methods exist for discharging a DUT, the direct contact discharge method is the only acceptable method to discharge a DUT for this test method.

3.2.1 Direct Charging Method

The DUT is placed “dead-bug” (upside down with pins pointing up) with device body in direct contact with the charge plate and charged either through the pin(s) providing the best ohmic connection to the substrate of the DUT or through all DUT pins simultaneously (see Figure 1). To prevent damaging the DUT, ensure both the device and charging mechanism are at ground potential prior to initiating the CDM test. Contact to the charging pin(s) must be made prior to raising the charge potential. Once the DUT is charged, a pin under test (PUT) is discharged (except any pin(s) directly connected to the substrate of the DUT). It is permissible to leave the charging probe in direct contact with the charging pin during the discharge event provided the discharge waveform meets the requirements of Table 2, Table 3, and Figure 3. After discharging the PUT, the DUT shall be re-charged and the process is repeated for each pin to be tested. Special devices (such as multi-chip modules, hybrids, and sub-assemblies) must be charged through a common power supply/ground pin or a sufficient number of device pins to ensure the charging potential is reached. All charge pins must be recorded.

3.2.2 Field-induced Charging Method

The DUT is placed “dead-bug” (upside down with pins pointing up) with device body in direct contact with the field charging plate and charged by raising the potential of the charge plate (see Figure 1). To prevent damaging the DUT, ensure both the device and charge plate are at ground potential prior to initiating the CDM test. Once the DUT is charged, a pin under test (PUT) is discharged. After discharging the PUT, the DUT shall be re-charged and the process is repeated for each pin to be tested. The field charging plate shall be at least seven times (7X) larger in area than the DUT and shall meet the requirements of Table 2, Table 3, and Figure 3. If a dielectric film is used during device testing, it shall be less than 130 microns thick and must be in place during the waveform verification procedure.

3.2.3 Direct Discharging Method

Direct contact discharge is initiated within a relay and can add parasitics to the discharge path (care must be taken to minimize these parasitics). A discharge probe (e.g., pogo pin), connected to the relay, is placed in direct contact with the PUT and produces a very repeatable CDM event.

3.3 Test Temperature

Each device shall be subjected to ESD pulses at room temperature.

3.4 Measurements

Prior to ESD testing, complete initial DC parametric and functional testing (initial ATE verification) shall be performed on all sample groups and all devices in each sample group per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3.5 Cleaning Method

To avoid charge loss during CDM testing, devices should be cleaned with isopropanol (isopropyl alcohol) using a procedure approved by the local safety organization. Devices should then be handled only by vacuum tweezers, personnel wearing finger cots or equivalent, or plastic tweezers which have been neutralized by holding in an ionized air stream. The CDM tester should be cleaned periodically with isopropanol (isopropyl alcohol) to remove any surface contamination that could result in charge loss. Particular attention should be paid to the discharge probe, charging probe, and the charge plate on which the device is placed.

3.6 Detailed Procedure

The ESD testing procedure shall be per the test flow diagram of Figure 4 and as follows:

a. Place clean DUT “dead-bug” (upside down with pins pointing up) with device body in direct contact with the charge plate.

b. Set the charge voltage to + 250 volts. Voltage level skipping is not allowed.

c. Select a charging method and charge the DUT.

d. Select a PUT and discharge the DUT. After discharging, wait a minimum of 1 second and re-charge the DUT. The use of three (3) discharges at each charge voltage polarity is required.

e. Set the charge voltage to - 250 volts. Voltage level skipping is not allowed.

f. Repeat steps (c) through (e) using the same PUT.

g. Repeat steps (b) through (f) until every PUT is discharged at the specified voltage.

h. Test the next device in the sample group and repeat steps (a) through (g) until all devices in the sample group have been tested at the specified voltage level.

i. Submit the devices for complete DC parametric and functional testing (final ATE verification) per applicable device specification within 96 hours of ESD testing and determine whether the devices pass the failure criteria requirements specified in section 4. Complete DC parametric and functional testing shall be performed at room temperature followed by hot temperature, unless specified otherwise in the device specification. The functionality of "E^2PROM" type devices shall be verified by programming random patterns. If a different sample group is tested for each stress voltage level, it is permitted to perform the DC parametric and functional testing (final ATE verification) per device specification after all sample groups have been tested.

j. Using the next sample group, increase the pulse voltage by 250 volts and repeat steps (a) through (i). Voltage level skipping is not allowed. It is permitted to use the same sample group for the next stress voltage level if all devices in a sample group pass the failure criteria requirements specified in section 4 after exposure to a specified voltage level.

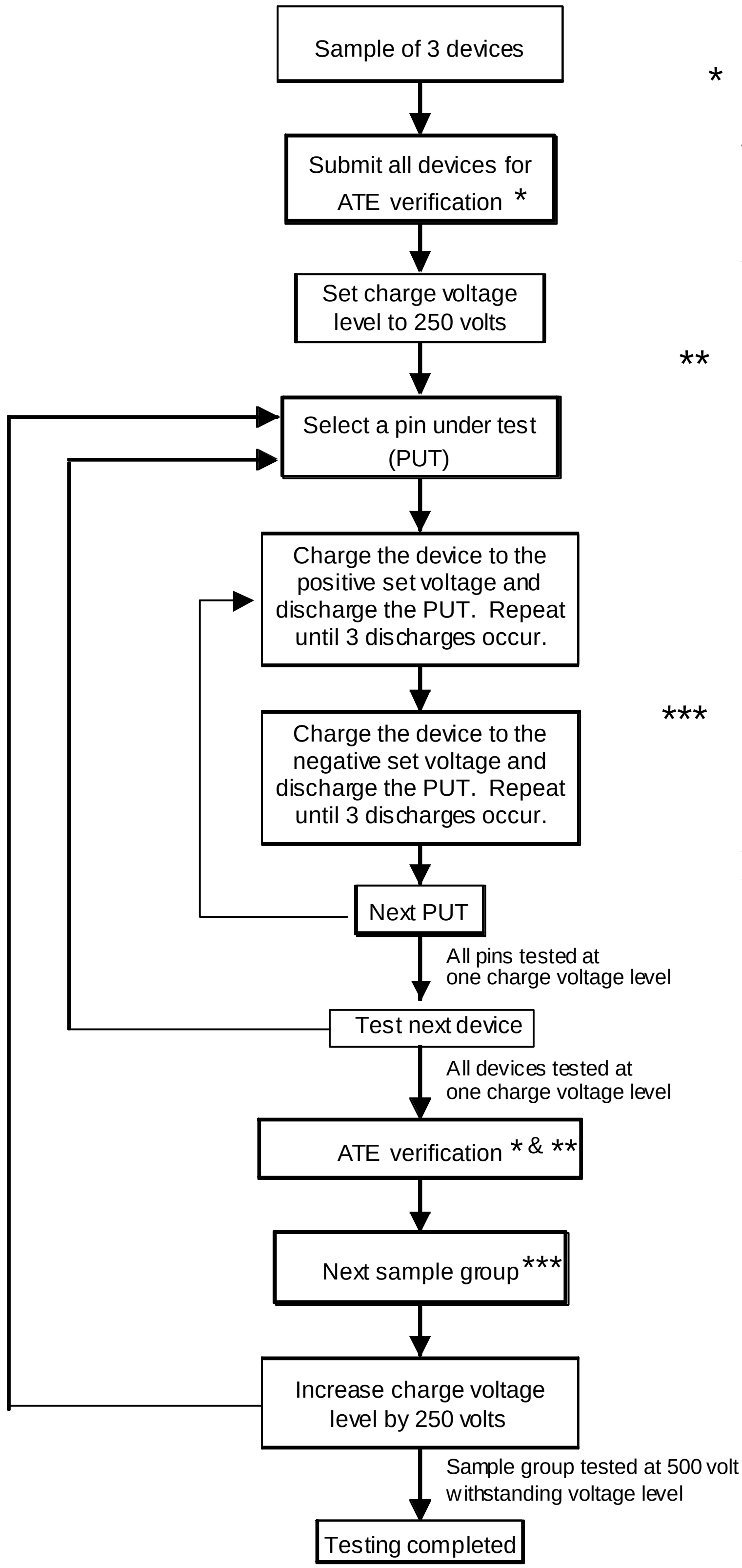
k. Repeat steps (a) through (j) until failure occurs or a 500 volt withstanding voltage level has been reached.

4. FAILURE CRITERIA

A device will be defined as a failure if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete DC parametric and functional testing (initial and final ATE verification) shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification. Complete DC parametric and functional testing immediately following the ESD test provides worst-case data results. For some devices, parametric and functional characteristics may fall outside specified device specification limits when tested immediately after ESD testing, but slowly drift towards acceptable levels over time. If complete DC parametric and functional testing is delayed, the device may be improperly classified at a higher CDM withstanding voltage.

5. ACCEPTANCE CRITERIA

A device passes a voltage level if all devices in the sample group stressed at that voltage level pass. All the devices and sample groups used must pass the measurement requirements specified in section 3 and the failure criteria requirements specified in section 4 up to a 500 volt withstanding voltage level in order for the devices to be considered acceptable. The CDM ESD withstanding voltage shall be defined for each device by the supplier. Due to the complex nature of the CDM event, a change in manufacturing process, design, materials, or device package may require reclassification according to this test method.



* For initial ATE verification, all devices shall be tested to complete DC parametric and functional requirements per applicable Device Specification at room temperature followed by hot temperature, unless specified otherwise in the Device Specification.

** If a different sample group is tested at each charge voltage level, it is permitted to perform complete DC parametric and functional testing (final ATE verification) per applicable Device Specification at room temperature followed by hot temperature, unless specified otherwise in the Device Specification, after all sample groups have completed testing.

*** It is permitted to use the next higher charge voltage level if all devices in the sample group pass the failure criteria requirements specified in section 4 after exposure to a specified charge voltage level.

Figure 4: Integrated circuit CDM ESD test flow diagram

Revision History

Rev #	Date of change	Brief summary listing affected sections
-	DATE, 2000	Initial Release.
A	Jan 31, 2001	Changed title, revised paragraphs 1.1, 1.2, 3.2, 3.2.1, 3.2.2, revised Table 2 & 3, revised Figure 3.