Automotive Electronics Council
Component Technical Committee

ATTACHMENT 5

AEC - Q100-005 - REV-C

NON-VOLATILE MEMORY PROGRAM/ERASE ENDURANCE, DATA RETENTION, AND OPERATING LIFE TEST

Automotive Electronics Council

Component Technical Committee

Acknowledgment

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Change Notification

The following summary details the changes incorporated into AEC-Q100-005 Rev-C:

- **Entire document: All references to "write" replaced with "program.**
- **Section 1, Purpose: Allowance for alternative procedures to this document with approval. Definition of a bit flip.**
- **Section 2, Apparatus: Specified chamber temperature tolerance. All references to "should" replaced with "shall".**
- **Section 3, Procedure: Inserted figure 1 which illustrates the different required test sequences. Allowance for reduction of tested NVM array size with approval.**
- **Section 3.1, step b: Specify use of worst-case conditions during cycling. Requirement to disable error correction code during cycling. Allowance for alternative program/erase algorithms with approval.**
- **Section 3.2, step b: Allowance for alternative test conditions with approval.**
- **Section 3.2, step d & 3.3, step d: Replace 1008 hours with 1000 hours. Allowance for the use of alternative accelerating data retention temperatures with justification. Add reference to applicable AEC-Q100 test method.**
- **Section 3.2, step e & 3.3, step e: Conditions for waiving additional HTSL or HTOL testing.**
- **Section 3.3, High Temperature Operating Life (HTOL) Procedure: Change section title from "Operating Life" to "High Temperature Operating Life (HTOL)".**
- **Section 3.3, step b: Defining requirements for embedded and standalone NVM devices, clarifying when separate HTOL tests need to be run.**
- **Section 3.5.1, Electrical Measurements: Change time limit for electrical measurement after removal from stress to 96 hours to align with industry standards.**
- **Section 3.5.3, Measurement Conditions: Replace "should" with "shall".**
- **Section 5, Summary: Add examples of requested alternative procedures.**

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METHOD - 005

NON-VOLATILE MEMORY PROGRAM/ERASE ENDURANCE, DATA RETENTION, AND OPERATING LIFE TEST

Text enhancements and differences made since the last revision of this document are shown as underlined areas.

1. PURPOSE

This test is intended to evaluate the ability of the memory array of a standalone Non-volatile Memory (NVM) integrated circuit or an integrated circuit with a Non-volatile Memory module (such as a microprocessor Flash Memory) to: sustain repeated data changes without failure (Program/Erase Endurance), retain data for the expected life of the Non-volatile Memory (Data Retention), and withstand constant temperature with an electrical bias applied (Operating Life).

Alternative procedures requested by the NVM supplier, including but not limited to program/erase cycle sequencing, data retention duration and temperature, and checksum testing on stand-alone NVM devices, must be approved by the user.

For Program/Erase Endurance Cycling, a data change occurs when a stored "1" is changed to a "0", or when a stored "0" is changed to a "1". Failure occurs when a write or erase event is not completed in less than the maximum specified time, or when the event completes but the data pattern within the memory array does not correspond to the intended data pattern.

Data Retention is a measure of the ability of a memory cell in an NVM array to retain its charge state in the absence of applied external bias. Data retention failure occurs when a memory cell loses or gains charge to the extent that it is no longer detected to be in its intended data state.

A bit flip is defined as the failure of a bit to retain its data state after a program or erase operation.

Three categories of failure can occur due to Operating Life stress. The Non-volatile Memory may cease to function, it may degrade to the point that the specified performance is not met, or it may fail to retain its intended data state.

2. APPARATUS

The apparatus required for this test shall consist of a controlled temperature chamber capable of maintaining the temperature conditions at or above the specified temperatures (e.g., 125°C -0/+5°C chamber tolerance). Sockets or other mounting means shall be provided within the chamber so that reliable electrical contact can be made to the device terminals in the specified circuit configuration. Power supplies and biasing networks shall be capable of maintaining the specified operating conditions throughout the test. Also, the test circuitry shall be designed so that the existence of abnormal or failed devices will not alter the specified conditions for other units on test. Care shall be taken to avoid possible damage from transient voltage spikes or other conditions which might result in electrical, thermal or mechanical overstress.

3. PROCEDURE

Devices containing NVM shall first be preconditioned (exercised) through the Program/Erase Endurance test before performing Data Retention/High Temperature Storage Life (HTSL) and High Temperature Operating Life (HTOL) testing (see Figure 1).

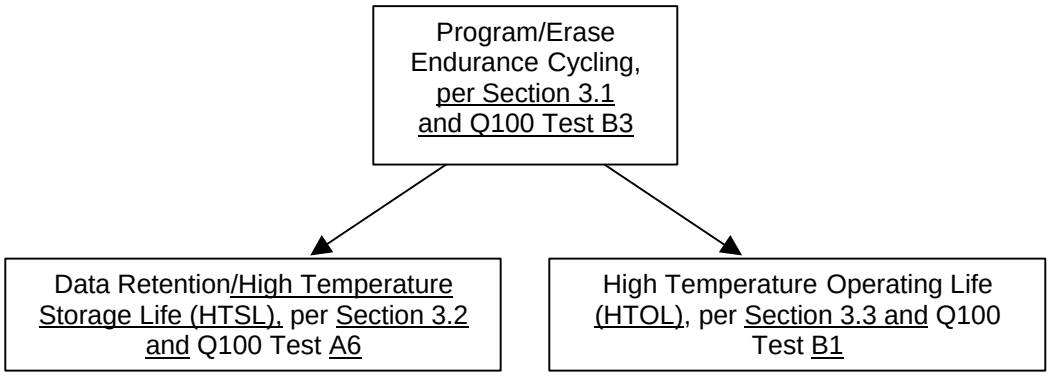

Figure 1: Test Sequence for Devices Containing NVM

With user's approval, the supplier is allowed to reduce the size of the NVM array being preconditioned or endurance tested to reduce qualification time to a reasonable length. In such instances the program/erase cycles applied to the reduced memory must be no less than the maximum specification. The size of the reduced memory array shall represent the amount typically used in high endurance applications. The remaining array segments shall be preconditioned or endurance tested to the maximum number of program/erase cycles possible without adding unreasonable qualification time. Program/erase cycling shall follow the requirements of this document outlined in section 3.1.

3.1 Program/Erase Endurance Cycling Procedure

a. Devices shall be placed in the chamber so there is no substantial obstruction to the flow of air across and around each unit. The power shall be applied and suitable checks made to ensure that all devices are properly energized. When special mounting or heat sinking is required; the details shall be specified in the applicable device specification.

b. Devices shall be tested for Program/Erase Endurance Cycling using the minimum number of cycles stated in the applicable device specification. Endurance testing shall be performed using worst-case conditions with respect to temperature, voltage, and frequency. Cycling is performed continuously, with one cycle being defined as a transition from one state to another and back to the original state (i.e., from “1” to “0” back to “1”; or from “0” to “1” back to “0”) on all bit cells in the memory array. During the endurance test, each write and erase operation must be verified to have successfully completed and the intended data state is to be validated through a read operation. Endurance test cycling is described below.

1. **Odd Cycles:**
   - Program array checkerboard
   - Normal read array checkerboard
   - Program array all “0”
   - Normal read array all “0”
   - Erase array
   - Normal read array all “1”

2. **Even Cycles:**
   - Program array inverse checkerboard
   - Normal read array inverse checkerboard
   - Program array all “0”
   - Normal read array all “0”
   - Erase array
   - Normal read array all “1”

For devices containing memory that uses error correction code (ECC) for fault tolerance, this coding algorithm must be disabled such that all cells in the array can be stressed and tested without the effect of error correction techniques. If this is not possible, the supplier must agree on an alternative stressing procedure with the user.

“Odd” and “Even” cycles are repeated until the sum of the two is no less than the endurance specification. Alternate program/erase algorithms or patterns could be used upon agreement between the supplier and user.

c. Following completion of the specified number of Program/Erase cycles, verification of functionality to the device specification shall be performed per section 3.5.

3.2 Data Retention/High Temperature Storage Life (HTSL) Procedure

a. After completing Program/Erase Endurance Cycling testing as described in section 3.1, the devices shall be programmed with a worst-case pattern for the specific technology, such as topological checkerboard (i.e., where each bit is surrounded by its complement) or all bit cells programmed. Alternative patterns are acceptable when agreed to by the user and supplier.

b. The units are subjected to High Temperature Storage Life test (HTSL) per Table 2 of AEC-Q100 at 150°C for 1000 hours. For new technologies different from the standard floating gate technology, modified test conditions (such as duration and temperature) could be used based on the activating energy for the data retention failure of the new technology. The new test conditions can be used only upon user approval.

c. To preserve the intent of the Data Retention stress, only data pattern verification and non-array altering functional testing is performed at interim read points. This purposely excludes any program or erase testing of the NVM array.

d. At the qualification point (1000 hours), devices are first tested to verify that the data pattern has been retained at temperature(s) justified by the supplier. This is to be followed by full functional testing to the device specification, per AEC-Q100 test A6. At this point, full functional testing consists of array altering program and erase events.

e. If this procedure (section 3.2) is performed, the supplier is not required to perform additional High Temperature Storage Life (HTSL) testing.

3.3 High Temperature Operating Life (HTOL) Procedure

a. After performing Program/Erase Endurance Cycling testing as described in section 3.1, half of the devices under test shall be programmed with a checkerboard pattern and the other half with inverse checkerboard pattern (i.e., where each bit is surrounded by its complement). In some cases, an alternative pattern such as a logical checkerboard may better represent a worst-case condition. Alternative patterns are acceptable when agreed to by user and supplier.

b. Devices with embedded and stand-alone NVM shall be subjected to High Temperature Operating Life (HTOL) testing per Table 2 of AEC-Q100, using temperature and duration conditions meeting or exceeding the HTOL requirement for the device specified operating temperature grade. During this test, all addresses in the NVM array shall be accessed (read) to the maximum possible number of reads (per AEC-Q100 test B3) without impacting the HTOL exercise of the Logic (per AEC-Q100 test B1). Otherwise, separate HTOL tests shall be performed for the NVM and Logic memory blocks. For the duration of the test, full memory array checksum (i.e., "Bit Flip") testing must be continuously performed at speed for embedded flash microprocessors. The stand-alone flash (discrete) could be exempt from this checksum requirement upon supplier-customer agreement.

c. Only data pattern verification and non-array altering functional testing is performed at interim read points. This purposely excludes any program or erase testing of the NVM array.

d. At the qualification point, devices are first tested to verify that the data pattern has been retained at temperature(s) justified by the supplier. This is to be followed by full functional testing to the device specification, per AEC-Q100 test B1. At this point, full functional testing consists of array altering program and erase events.

e. If this procedure (section 3.3) is performed, the supplier is not required to perform additional High Temperature Operating Life (HTOL) testing.

3.4 Test Precautions

Precautions shall be taken to ensure that devices cannot be damaged by thermal runaway of the device or tester and to preclude electrical damage. The test setup shall be monitored initially and at the conclusion of a test interval to establish that all devices are being stressed to the specified requirements. The bias voltages and currents on each device shall be noted and corrected prior to further temperature exposure. If a device is not biased properly when checked at the conclusion of a test interval, it must be determined if the device has changed or if the test circuit has changed so that the validity of the data for qualification can be established.

3.5 Measurements

3.5.1 Electrical Measurements

The electrical measurements shall be made at intervals per the applicable device specification. Interim and final electrical measurements shall be completed within 96 hours after removal of the devices from the specified test conditions.

3.5.2 Required Measurements

The electrical measurements shall consist of parametric and functional tests specified in the applicable device specification.

3.5.3 Measurement Conditions

Before removing the devices from the chamber, the ambient temperature shall be returned to room temperature while maintaining the specified voltages on the devices. Testing shall be conducted per AEC-Q100 temperature ranges (e.g., +25°C, –40°C, and +125°C).

4. FAILURE CRITERIA

A device will be defined as a failure if the parametric limits are exceeded, the device no longer meets the device specification requirements, or if a programmed bit fails to retain its initial data state.

During Program/Erase Endurance Cycling testing, failure occurs when a write or erase event is not completed in less than the maximum specified time or when the event completes but the data pattern within the memory array does not correspond to the intended data pattern.

5. SUMMARY

The following details shall be included in the supplier's stress test specification or the applicable device specification:

a. Special mounting, if applicable.
b. Test condition, alphanumeric code.
c. Biasing conditions.
d. Measurements before, at intermediate test points (if applicable), and after test.
e. Maximum number of logic transitions in the memory cell.
f. Period between write cycles.
g. Alternative procedures requested by the NVM supplier, including but not limited to program/erase cycle sequencing, separate samplings for the test sequence described in Figure 1, data retention duration and temperature, and checksum testing on stand-alone NVM devices, must be approved by the user.

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Revision History

Rev #	Date of change	Brief summary listing affected sections
-	June 9, 1994	Initial Release
A	May 19, 1995	Merged 005 and 006 into single spec.
B	July 18, 2003	Complete revision. Title change to NONVOLATILE MEMORY PROGRAM/ERASE ENDURANCE, DATA RETENTION, AND OPERATIONAL LIFE TEST. All references to EEPROM replaced with Nonvolatile Memory. Added new Figure 1. New section 3.3 added for Operational Life testing.
C	Sept. 7, 2004	Complete revision.