Automotive Electronics Council
Component Technical Committee

ATTACHMENT 4

AEC - Q100-004 REV-C

IC LATCH-UP TEST

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Acknowledgment

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Counsel would especially like to recognize the following significant contributors to the development of this document:

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Change Notification

The following summary details the changes incorporated into AEC-Q100-004 Rev-C:

- **Replaced CDF-AEC-Q100-004 with the JEDEC IC Latch-up Test specification EIA/JESD78.**

- **Section 1.2, Class II Classification: AEC-Q100 latch-up testing shall be performed at the maximum ambient operating temperature.**

- **Section 1.3, Failure criteria: Device does not pass the test requirements of Table 1 (JEDEC - Level A); or Device no longer meets device specification requirements.**

- **Section 4.1 and Table 1A: The use of a voltage trigger (E-test) Latch-up test is also acceptable. Specific E-test parameters are indicated in Table 1A.**

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METHOD - 004

IC LATCH-UP TEST

All Latch-up testing performed on Integrated Circuit devices to be AEC Q100 qualified shall be per the JEDEC EIA/JESD78 specification with the following requirements (section numbers listed correspond to the JEDEC specification):

1.2 Class II Classification

All AEC Q100-004 qualification testing shall be performed with the device under test at the maximum ambient operating temperature (JEDEC - Class II).

1.3 Level A Failure Criteria

A device failure is defined by either of the following conditions:

1. Device does not pass the test requirements of Table 1 (JEDEC - Level A).

2. Device no longer meets device specification requirements. Complete DC parametric and functional testing (initial and final ATE verification) shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

4.1 General Latch-up Test Procedure

The use of a voltage trigger (E-test) latch-up test is also acceptable. E-test is a latch-up test in which positive and negative pulses are applied to the pin under test. The actual test procedure shall be performed per the I-test procedure, substituting a voltage trigger for the current trigger. Specific E-test parameters are indicated in Table 1A.

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Table 1A: E-test addendum to JEDEC specification Table 1, Test Matrix **[5]**

TEST TYPE	TRIGGER POLARITY	CONDITION OF UNTESTED INPUT PINS	TEST TEMPERATURE (± 2°C)	V_{supply} CONDITION	TRIGGER TEST CONDITIONS	FAILURE CRITERIA
E-TEST	POSITIVE see FIGURE 5	Max. Logic High **[1]**	Maximum ambient operating temperature	Maximum operating voltage for each V_{supply} pin group per device specification	+1.5X max. Logic High **[2]**	(I_{nom} + 10mA) or (1.4 X I_{nom}), whichever is greater **[4]**
		Min. Logic Low **[1]**				
	NEGATIVE see FIGURE 6	Max. Logic High **[1]**			-0.5X max. Logic High **[3]**	
		Min. Logic Low **[1]**				

Notes:

[1] Max. logic high and min. logic low shall be per the device specification. When logic levels are used with respect to a non-digital device, it means the maximum high or minimum low voltage that can be supplied to the pin per the device specification.

[2] Current clamped at (I_{nom} + 100 mA) or 1.5X I_{nom}, whichever is greater.

[3] Current clamped at -100 mA or -0.5X I_{nom}, whichever is greater in magnitude.

[4] If the trigger test condition reaches the voltage or current clamp limit and latch-up has not occurred, the pin passes the latch-up test. See section 5 of the JEDEC specification for complete failure definition.

[5] The trigger conditions herein are not indicative of appropriate trigger conditions for all devices. Appropriate trigger conditions may be more or less stringent. When trigger conditions used in testing differ from this table, the trigger conditions used must be defined in the test results.

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Revision History

Rev #	Date of change	Brief summary listing affected sections
-	June 9, 1994	Initial Release
A	May 15, 1995	Added copyright statement. Revised the following: Foreword; Sections 2.3, 2.4, 3.1, 3.2, 3.4, 3.5 (g, h, I, o, and p), and 4.0; Tables 1 and 2; Figures 2, 3, and 4.
B	Sept. 6, 1996	Revised the following: Sections 1.3.1, 1.3.7, 1.3.8, 2.1, 2.3, 3.1, 3.2, 3.3, 3.4, 3.5 (o, p, and q), 4.0, and 5.0; Figures 1 and 4.
C	Oct. 8, 1998	Replaced CDF-AEC-Q100-004 with the JEDEC IC Latch-up Test specification EIA/JESD78 with additional requirements. Added the following requirements: Sections 1.2, 1.3, and 4.1 (to correspond with the JEDEC specification section numbers); Table 1A (E-test addendum to JEDEC specification Table 1).