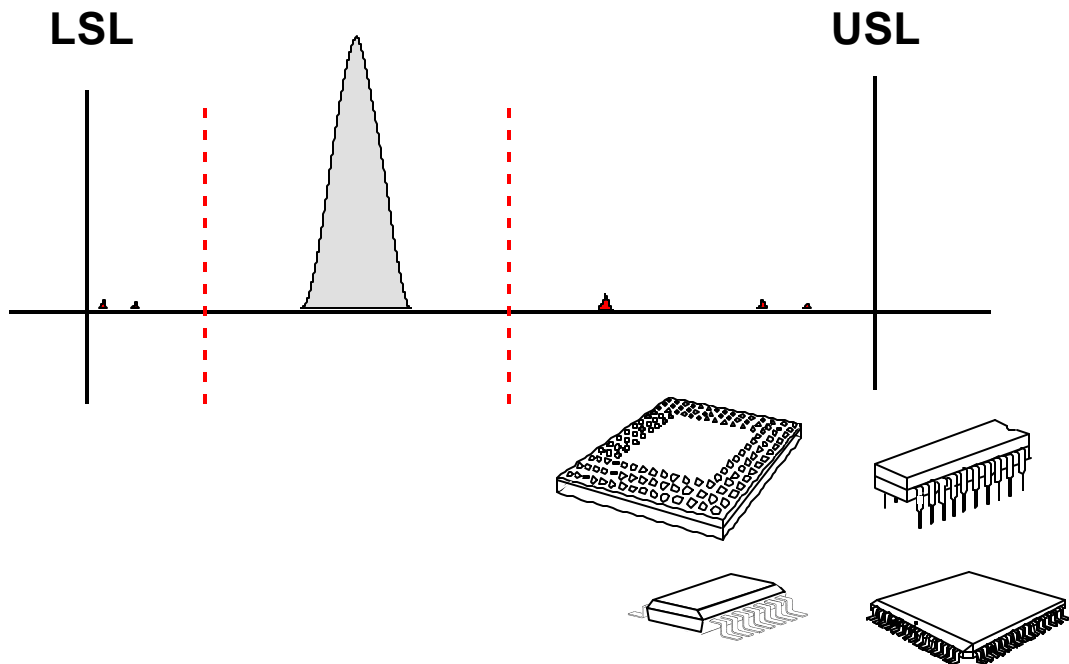


# GUIDELINES FOR PART AVERAGE TESTING



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Component Technical Committee

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**Acknowledgment**

Any document involving a complex technology brings together experience and skills from many sources. The Automotive Electronics Council would especially like to recognize the following significant contributors to the development of this document:

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**GUIDELINES FOR PART AVERAGE TESTING**

*Text enhancements and differences made since the last revision of this document are shown as underlined areas.*

**1. SCOPE**

This guideline presents a statistically based method, called part average testing (PAT), for removing parts with abnormal characteristics (outliers) from the semiconductors supplied per AEC - Q100 and AEC - Q101. The test limits used in PAT are established based on a sample of the electrical test results for that particular part with its unique design and processing. Each part design and its associated processing will show a unique distribution of test results for each test requirement and this data is the basis for establishing PAT limits. The principles described in this guideline are applicable to packaged or unpackaged die. For a further discussion of PAT and its possible use to provide Known Good Die, see Appendix 1.

**1.1 Purpose**

This guideline is intended to provide a general method for removing abnormal parts and thus improve the quality and reliability of parts supplied per AEC - Q100 and AEC - Q101. PAT is not intended to be a requirement, unless specified in the applicable procurement document or specifically approved by the user as a substitute for ELFR. The failures from ELFR and PAT do not always show a 1:1 correlation.

Meeting the intent of this guideline, either by performing this method or some other similar method, is highly recommended. History has shown that parts with abnormal characteristics significantly contribute to quality and reliability problems. Use of this technique will also flag process shifts and provide a source of rapid feedback that should prevent quality accidents.

**1.2 References**

**1.2.1 Automotive**

1. AEC - Q100: Stress Test Qualification For Integrated Circuits
2. AEC - Q101: Stress Test Qualification For Discrete Semiconductors

**1.2.2 Miscellaneous**

Iglewicz, B. and Hoaglin, D.C., ASQC Basic References in Quality Control: Statistical Techniques, Volume 16: How to Detect and Handle Outliers, ASQC Quality Press, 1993, ISBN 0-87389-247-X.

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## 2. DEFINITIONS

### 2.1 Important Characteristics

Device characteristics that could impact product quality and reliability. Characteristics that provide the most significant information about a part's capability of working properly. For examples of important characteristics, see Appendix 2. These characteristics may not necessarily affect the part's ability to operate in the application.

### 2.2 Known Good Die (KGD)

Unpackaged semiconductor devices that are at least as good as an equivalent packaged part.

### 2.3 Lower Specification Limit (LSL)

Lower specification limit specified on the device specification.

### 2.4 Robust Mean and Robust Sigma

Statistics calculated excluding outlying data. Outlying data is generally considered to be data that is more than 6 standard deviations away from the mean of the main distribution.

An example of one generalized method of doing this is as follows:

Exclude outliers by estimating the location and spread of the main distribution of parts. The usual Mean and Sigma can be poor statistics because they are very sensitive to outliers. The use of the term "Robust" is to indicate statistics that are insensitive to outliers.

**Robust Mean = Q2 [the median]**

**Note 1:** Q2 (Quartile 2) is the middle data point, if the sample size is an odd number. If the sample size is an even number, Q2 is the average of the two middle numbers.

**Robust Sigma = (Q3 - Q1) / 1.35**

**Note 2:** The 1.35 number is inexact for sample sizes less than 20. Q1 is the point 1/4 of the way through the ranked data and Q3 is the point 3/4 the way through the ranked data.

### 2.5 Upper Specification Limit (USL)

Upper specification limit specified on the device specification.

## 3. PROCEDURE

### 3.1 Setting The Test Limits

Test limits may be set in either a static or dynamic manner. The static limits are established based on an available amount of test data and used without modification for some period of time. The dynamic test limits are based on the static limits, but are established for each lot (or wafer in a lot) and continually change as each lot (or wafer) is tested. New PAT limits (both static and dynamic) must be established when wafer level design changes, die shrinks or process changes have been made.

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Component Technical Committee

### 3.1.1 Static PAT limits

Collect test data from at least six part lots that have passed the test limits as defined by the device specification. Determine the robust mean and sigma values per test by randomly selecting the test data from a minimum of 30 parts from each lot (see Figure 1). If test data is wafer level data, select data from at least 5 die located in different areas of each wafer (at least 30 die per lot). Early in production of a part, when data from six lots is not available, data from characterization lots may be used. This data shall be updated as soon as production data is available. Set the test limits as follows:

$$\text{Static PAT Limits} = \text{Robust Mean} \pm 6 \text{ Robust Sigma}$$

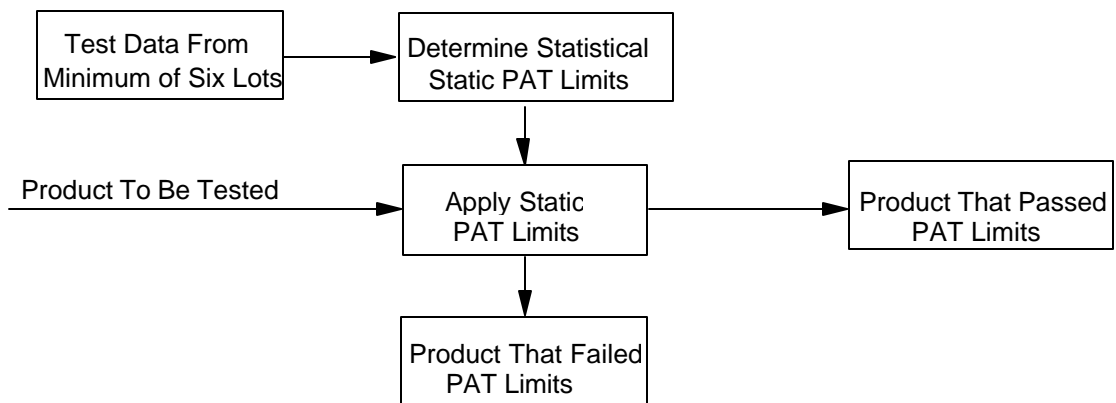


Figure 1: Determining Static PAT Limits

**3.1.1.1** PAT limits should be used for all electrical tests if possible, but shall be established for at least 8 important characteristics (see Appendix 2). PAT test limits shall not exceed the device specification limits and shall be reviewed and updated as required using current data during the first 6 months of production or the last 8 wafer lots, whichever occurs first. Older data shall not be used.

**3.1.1.2** After 6 months the static PAT limits shall be reviewed and updated as needed on a quarterly (every 3 month) basis.

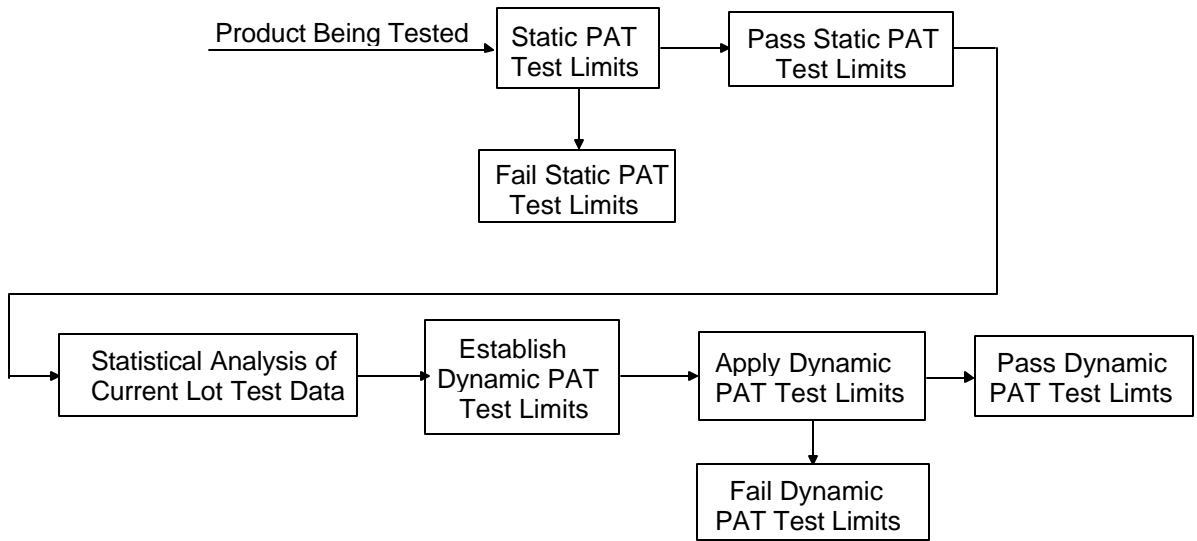
### 3.1.2 Dynamic PAT limits

Dynamic PAT Limits are preferred over Static PAT Limits because the reference population is the same as the parts being tested. Dynamic PAT can provide tighter limits without causing rejection of good parts because it does not have to consider the lot-to-lot variation that is part of Static PAT Limits. Before dynamic limits can be established, static limits, as defined in [section 3.1.1](#), must be established. Dynamic PAT limits are determined in the same manner as static PAT limits except that the limits are established using the data from the current lot (or wafer) of parts under test that have passed the static limits. To use this method, after the lot (or wafer) of parts have been tested to the static limits they must be held in a manner that allows further statistical analysis of the test data. This analysis establishes new tighter test limits for that particular lot (or wafer) and removes additional outliers (see Figure 2). Set the test limits as follows:

$$\text{Dynamic PAT Limits} = \text{Mean} \pm 6 \text{ Sigma}$$

**Note 3** Statistical values calculated for the particular lot (or wafer) after the parts in the lot have passed the static PAT limits.

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**Figure 2: Determining Dynamic PAT Limits**

## APPENDIX 1: PART AVERAGE TEST LIMITS

- A1.** Part Average Test (PAT) Limits represent the application of statistical techniques for the removal of abnormal parts during part level testing (see Figure 3). A device specification defines the requirements needed for the part to work properly in the application. Every part (part as used here refers to a supplier part number) is built with a particular design and SPC controlled process that, if processed correctly, will yield a certain consistent set of characteristic test results. PAT uses statistical techniques to establish the limits on these test results. These test limits are set up to remove outliers (parts whose parameters are statistically different from the typical part) and should have minimal yield impact on correctly processed parts from an SPC controlled process. This test methodology is not limited to the standard device specification tests, but may also include extended operating tests (tests beyond the device specification requirements) to improve the ability to detect special abnormal conditions and increase the sensitivity of this testing technique. The only restriction on extended operating tests is that the test shall not reduce the reliability of the parts that pass the test.
- A1.1** The intent of PAT is to increase the quality and reliability of AEC - Q100 and AEC - Q101 parts by removing abnormal parts as early in the part manufacturing sequence as possible (possibly at wafer test). This should minimize costs related to customer support and failure analysis, and provide early feedback to prevent the occurrence of quality accidents.
- A1.2** This method, if utilized to its full capability (with statistical limits for all part level electrical tests and proper extended operating condition tests), is capable of providing “electrically” Known Good Die for most semiconductor technologies. It should also be remembered that Known Good Die (as defined in [section 2](#)) requires more than part level electrical testing. It requires careful control of all other assembly processes such as wafer sawing, die handling, packaging, ESD, etc.

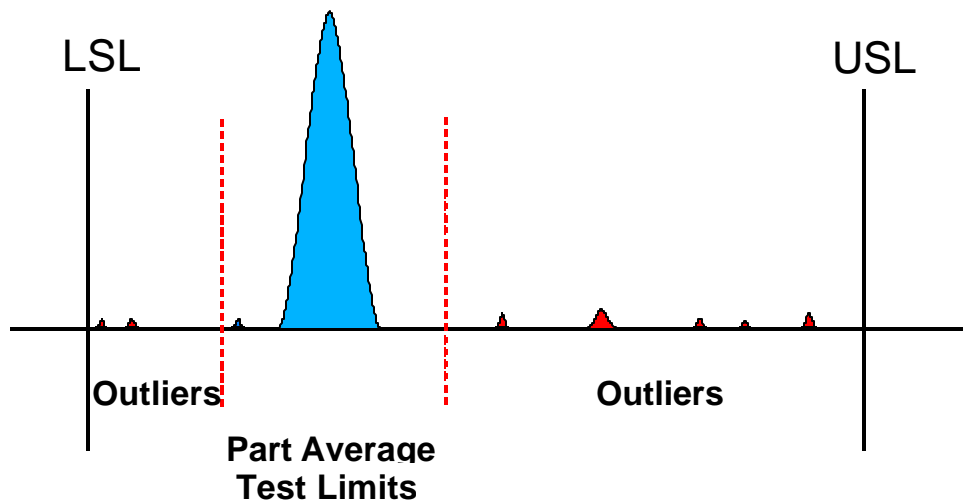


Figure 3: Graphical Representation of Part Average Test Limits and Outliers

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**APPENDIX 2: ELECTRICAL TESTS**

**A2.1 Tests Required For All Devices Types**

To meet the requirements of this procedure, the following tests shall use PAT limits during ATE testing.

**A2.1.1 Pin Leakage Test**

Use the following measurement approach to establish the PAT limits for pin leakage. This test will verify that the device pins have normal junction characteristics with respect to substrate and with respect to  $V_{DD}$  in the case of CMOS components.

- a. With all pins grounded except the pin under test (PUT):
1. Force  $-10\mu\text{A}$  into each pin, measure the forward biased junction voltage ( $V_{F1}$ ).
  2. For CMOS, also force  $+10\mu\text{A}$  into each pin, measure the forward biased junction voltage ( $V_{F1}$ ).
  3. Test  $V_{DD}$  ( $V_{CC}$ ) separately with respect to the substrate using  $-10\mu\text{A}$ , measure the forward biased junction voltage ( $V_{F2}$ ).
  4. Statistically analyze this data to determine the mean for  $V_{F1}$  and  $V_{F2}$ .
- b. With all pins grounded except the pin under test (PUT), and using the  $V_{F1}$  and  $V_{F2}$  values determined above, measure the leakage current:
1. Apply  $-0.8 V_{F1}$  (80% of forward bias voltage) to each pin, measure the leakage current.
  2. For CMOS, also apply  $+0.8 V_{F1}$  to each pin, measure the leakage currents.
  3. Apply  $-0.8 V_{F2}$  to  $V_{DD}$  ( $V_{CC}$ ), measure the leakage current.
  4. Statistically analyze this data to determine the leakage current PAT limits.

**Notes:**

4. After the conclusion of the final ATE test and following powering down, perform this test method to detect any possible damage that could have occurred during testing.
5. This method can utilize gang testing methods if the combination of pins have a PAT leakage limit that does not exceed  $600\eta\text{A}$ .
6. Devices with pins that have pull-up or pull-down loads are excluded from the above test methods. However, their impedance values used for testing must be based on PAT limits.

**A2.1.2 Standby Power Supply Current ( $I_{DD}$  or  $I_{CC}$ )**

**A2.2 Additional Tests Required For Certain Device Types**

**A2.2.1 CMOS Devices**

CMOS devices shall be  $I_{DDQ}$  tested with at least 70% transistor-level coverage (TLC). If the device design is not capable of being  $I_{DDQ}$  tested, then this requirement does not apply.



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### A2.2.2 Linear and BICMOS Devices

- a. Output breakdown voltage ( $BV_{CES}$  or  $BV_{DSS}$ ).
- b. Output leakage ( $I_{CES}$  or  $I_{DSS}$ ), measured at 80% of the breakdown voltage value.
- c. Output current drive ( $I_{OUT}$ ) and output voltage levels ( $V_{OUT}$ ).
- d. The CMOS portion of BICMOS devices shall be tested per section A2.2.1.

### A2.3 Examples of Additional Tests

The following are examples of tests whose parameter variations have shown a correlation to poor component quality and reliability in some integrated circuits. This is not a comprehensive list, and is offered only as a suggested list to be considered. Other tests deemed more important or more relevant to a particular device should also be included in Part Average Testing.

#### A2.3.1 Voltage Stress ( $V_S$ )

This test forces failures in silicon MOS type devices (e.g., NMOS, PMOS, CMOS, and DMOS, etc.) that have gate oxide and other related defects. To force failures that would occur within the power on time ( $t_A$ ) during the test time ( $t_S$ ), the test voltage stress ( $V_S$ ) must be greater than the maximum operating voltage ( $V_A$ ). The supplier is encouraged to use his experience on his processes/designs to determine this voltage. One equation that could be used to determine this voltage is as follows (this equation does not consider temperature, gate-aided drain/source breakdown and other potentially limiting factors):

$$V_S = V_A + (d_{ox} / \gamma) * \log_{10} (t_A / t_S) \text{ volts or} \\ = V_A + 0.5 V_A \text{ whichever is greater (see Note 7)}$$

where:  $d_{ox}$  = nominal gate oxide thickness in Angstroms  
 $\gamma$  = electrical field acceleration coefficient  
= 700 Angstroms •  $\log_{10}$  decade of time / volts  
 $t_A$  = power on time in seconds  
 $V_A$  = maximum operating voltage  
 $t_S$  = test time in seconds

For example if:

$V_A$  = 5 volts (max. operating voltage)

$d_{ox}$  = 400 Angstroms

$t_A$  = 10 years (in seconds) with power on continuously (for an automotive application, 10 years of ignition-on in the field is equal to about 5,000 hours or approximately  $18 \times 10^6$  seconds of power on operation)

$t_S$  = 0.1 second

the suggested stress test voltage  $V_S$  = 10.4 volts

#### Notes:

- 7. This equation is a generalized equation applicable at room temperature and is not corrected for elevated temperatures and other limiting factors.
- 8. Fault coverage must be considered during voltage stress. For example, on CMOS devices the voltage is applied only to the transistors that are "on". Two or more states may be

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necessary to force a stress voltage on a high proportion of gate oxides. The supply voltage should be raised to  $V_S$  for the duration  $t_S$  in each of these states.

9. The voltage stress test  $V_S$  supply current must be limited to insure proper operation of the test (1 ma is generally a good limit).
10. The voltage stress test must be followed by functional and parametric tests using PAT limits to detect the outlier parts.
11. To avoid wear-out  $V_S$  must be less than 5 volts / 100 Angstroms.
12. It must be demonstrated that the stress voltage does not adversely affect the reliability of the part. The reliability of the ICs can be demonstrated by passing the HTOL, ESD and Latch-up testing as specified in AEC - Q100 Tables 1 & 2. The reliability of discrete devices can be demonstrated by passing ESD, and HTGB testing per AEC - Q101.

**A2.3.1.1** The following references provide the basis for the Voltage Stress Test guidelines contained above:

- a. D. L. Crook, "Method of Determining Reliability Screens for Time Dependent Breakdown", Proceedings of The International Reliability Physics Symposium, 1979, pp. 1 - 7.
- b. A. Berman, "Time-Zero Dielectric Reliability Test by a Ramp Method", Proceedings of The International Reliability Physics Symposium, 1980, pp. 204 - 209.
- c. EIA/JEDEC Publication EIA/JEP122 "Failure Mechanisms and Models for Silicon Semiconductor Devices".

### **A2.3.2** Low Level Input Current ( $I_{IL}$ )

### **A2.3.3** High Level Input Current ( $I_{IH}$ )

### **A2.3.4** Propagation Delay or Output Response Time

### **A2.3.5** Rise/Fall Times

### **A2.3.6** Low Level Output Voltage ( $V_{OL}$ )

### **A2.3.7** High Level Output Voltage ( $V_{OH}$ )

### **A2.3.8** Extended Operating Tests

Extended operating tests are tests beyond the device specification requirements intended to increase the effectiveness of PAT. These are the type of tests that, combined with PAT testing of more device characteristics, can make part level testing capable of providing parts with very high quality and reliability (Known Good Die). PAT limits shall be established for each extended operating test. The following are some examples of extended operating tests:

- Low/High temperature
- Low/High voltage operation
- Dwell time at high voltage
- Operating frequencies above/below specification requirements
- For power devices, demonstration of safe operating capability (60% of safe operating limit) followed by leakage testing, etc.

**Note 13:** The only restriction on these tests is that it must be demonstrated that the test does not adversely affect the reliability of the part. The reliability of the part can be demonstrated by passing the electrical qualification tests as specified in AEC - Q100 (for ICs) and AEC - Q101 (for discrete semiconductors).

## Revision History

<u>Rev #</u>	<u>Date of change</u>	<u>Brief summary listing affected sections</u>
-	July 31, 1997	Initial Release.
A	Oct. 8, 1997	Paragraph 2.1 revised, Figure 2 changed, Appendix 2 added new paragraph 2.1, added Appendix 3.
B	Aug. 25, 2000	Revised 1.2.2, 3.1, 3.1.2, Appendix 1, and Appendix 3.
<u>C</u>	<u>July 18, 2003</u>	<u>Corrected formatting errors. Removed Appendix 3 and references to DE Histograms.</u>