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FAILURE MECHANISM BASED TESTING GUIDELINES FOR COMPONENTS MOUNTED TO A PRINTED BOARD

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Automotive Electronics Council
Component Technical Committee

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Automotive Electronics Council
Component Technical Committee

FAILURE MECHANISM BASED TESTING GUIDELINES FOR COMPONENTS MOUNTED TO A PRINTED BOARD

Unless otherwise stated herein, the date of implementation of this standard for new qualifications and re-qualifications is as of the publish date above.

1. SCOPE

This document contains procedures and guidelines to assist in the proper design, implementation and testing of the reliability of electronic components that utilize solder joints to connect onto/with printed boards (PBs) or other substrates. This document provides a framework to be used in support of and in combination with all other applicable AEC documents.

Unique failure-based reliability stress tests can be found as attachments to this base document. Neither the base document nor its attachments should be used indiscriminately. E ach reliability program should be examined for:

a. Any potential new and unique failure mechanisms.
b. Any situation where these test/conditions may induce failures that would not be seen in an application.
c. Any test condition that could result in an acceleration outside the boundaries of the acceleration model (e.g., exceeding material glass transition temperatures).

Use of this document and its attachments does not relieve the supplier of their responsibility to meet their own company's internal reliability program. In this document, "user" is defined as all customers using a device tested per this document. The user is responsible to confirm and validate all test data that substantiate conformance to this document.

Both the base document and the attachments (AEC-Q007-00x series) may be found at: aecouncil.com.

1.1. Purpose

The purpose of this document is to provide a basic test methodology which includes printed board, surface mount assembly, device under test descriptions, etc. for board level reliability failure-based stress tests. Details for each specific stress test method can be found in an attachment to the base document.

1.2. Reference Documents

Current revision of the referenced documents will be in effect at the date of agreement to the test plan. Subsequent qualification plans will follow updated revisions of these referenced documents.

1.2.1. Automotive

AEC-Q007-001	Board-Level Reliability Temperature Cycling Test Method
AEC-Q007-002	BLR Spreadsheets

1.2.2. Industrial

IEC 60068-2-58	Test Td: Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices (SMD)
IEC 60068-3-12	Supporting documentation and guidance - Method to evaluate a possible lead-free solder reflow temperature profile
IEC 60749-20	Resistance of plastic encapsulated SMDs to the combined effect of moisture and soldering heat

IEC 61190-1-1	Requirements for soldering fluxes for high-quality interconnections in electronics assembly
IEC 61190-1-2	Requirements for soldering pastes for high-quality interconnects in electronics assembly
IEC 61190-1-3	Requirements for electronic grade solder alloys and fluxed and non-fluxed solid solder for electronic soldering applications
IEC 61760-1	Standard method for the specification of surface mounting components (SMDs)
IEC 61760-4	Classification, packaging, labeling and handling of moisture sensitive devices
IPC-A-600	Acceptability of Printed Boards
IPC-A-610	Acceptability of Electronic Assemblies
IPC-1602	Standard for Printed Board Handling and Storage (Original), replaces IPC-1601
IPC-2221	Generic Standard on Printed Board Design
IPC-2222	Sectional Design Standard for Rigid Organic Printed Boards
IPC-2226	Sectional Design Standard for High Density Interconnect (HDI) Printed Boards
IPC-6012	Automotive Applications Addendum to IPC-6012E Qualification and Performance Specification for Rigid Printed Boards
IPC-7093	Design and Assembly Process Implementation for Bottom Termination Components (BTCs)
IPC-7095	Design and Assembly Process Implementation for BGAs
IPC-7525	Stencil Design Guidelines
IPC-7527	Requirements for Solder Paste Printing
IPC-7530	Guidelines for Temperature Profiling for Mass Soldering (Reflow & Wave) Processes
IPC-9701	Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments
IPC-9702	Monotonic Bend Characterization of Board-Level Interconnects
IPC-9703	IPC/JEDEC Mechanical Shock Test Guidelines for Solder Joint Reliability
IPC/JEDEC-9704	Printed Circuit Assembly Strain Gage Guideline
IPC-9850	Surface Mount Placement Equipment Characterization
JEDEC JESD-22	Reliability Test Methods for Packaged Devices
JEDEC J-STD-020	Moisture/Reflow Sensitivity Classification for Plastic Integrated Circuit Surface Mount Devices
JEDEC J-STD-075	Classification of Non-IC Electronic Components for Assembly Processes
JEP150.01	Stress-Test Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components
IPC-J-STD-001	Requirements for Soldered Electrical and Electronic Assemblies
IPC-J-STD-001XA/A-610XA G	Automotive Addendum to IPC-J-STD-001G Requirements for Soldered Electrical and Electronic Assemblies and IPC-A-610G Acceptability of Electronic Assemblies
IPC-J-STD-004	Requirements for Soldering Fluxes
IPC-J-STD-005	Requirements for Soldering Pastes
IPC-J-STD-006	Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications
IPC-SM-785	Guidelines for Accelerated Reliability Testing of Surface Mount Attachments

1.3. Definitions

1.3.1. AEC-Q007 BLR Test Conformance

Performance of the testing in accordance with the test methodology as outlined in this document and in the appropriate BLR attachments allows the supplier to claim that the part has completed the specified testing per AEC-Q007-00x, where x indicates the appropriate BLR test method.

1.3.2. Definitions of Common Terms

Note 1: Use of Shall, Should, Must and May
Shall: A keyword indicating a mandatory requirement
Should: A keyword indicating flexibility of choice with a preferred alternative
Must: The same as shall
May: A keyword that indicates flexibility of choice with no implied preference

Note 2: A reference to a definition (e.g., IPC-9701) can indicate the complete usage from the source or a modified usage from the source.

Accelerated Reliability Test: A test in which the degradation mechanism(s) of concern for operational use is (are) accelerated to cause failures in less time than in service. The test acceleration results from shorter cycle periods and/or more severe loading conditions; however, the introduction of extraneous degradation mechanisms must be avoided. The service life can be estimated by application of appropriate acceleration factors. (IPC-9701)

Area Array Component: A component that has terminations arranged in a grid on the bottom of the package and contained within the component outline. (IPC-JEDEC-9704)

Baseline Resistance: The resistance for the complete DUT measurement loop including the PB, cabling, instrumentation, etc.

Ball Grid Array (BGA): An array of solder balls that are attached to a component.

Board-Level Reliability Test (BLRT): Board-level reliability testing is the deliberate testing to determine how long solder joints and other interconnects survive for a component mounted to a printed board.

Board-Level Reliability (BLR): The reliability of solder joints and other interconnects of electronic components attached to printed (circuit) boards.

Catastrophic Failure: A worst-case event where a change in state from good to bad (failed) is permanent.

Coefficient of Thermal Expansion (CTE): Coefficient of Thermal Expansion (CTE) is the rate of linear physical size changes from temperature changes. CTE differences between a test vehicle and a printed board are the primary solder connection aging mechanism during BLRT. CTE for a test vehicle or PB may be a complex composite CTE. (Sometimes known as TCE.)

Daisy Chain: A conductive link that can be connected in series with other conductive links (like a chain of daisies) to form a continuous electrical circuit or “net”. A single link is a conductive path inside the DUT from one solder joint to another solder joint. A loop is multiple single links where each single link is typically connected by a link on a PB.

Device Under Test (DUT): The production worthy part or a specialized test vehicle (i.e., daisy chain part, etc.) used within the testing as specified herein.

Die Shadow: The volume under the die which can include the die attach/underfill epoxy, substrate/leadframe, and solder joints.

Digital Twin: A numerical representation in a computer (digital) format for the assembly under test. It is intended for numerical simulation of altered parameters including those unique to the user production intent.

Event: The occurrence of a measurement that meets the failure criteria

Event Detector: Instrumentation that responds to experimental signals and sets an output to, e.g., High for a preset event threshold.

Flip-Chip Ball Grid Array (FCBGA): A component package where the die is joined to a substrate surface by flipping the silicon active surface to face the substrate. The other substrate surface uses a BGA for joining to a PB. Without solder balls the package would be a flip-chip land grid array (FCLGA). Sometimes called a flip-chip plastic ball grid array (FC-PBGA).

Front End (FE): A term to designate wafer fabrication for a product.

Glass Transition Temperature (Tg): The temperature at which a material changes phase.

Glitch: A short in time measurement or event reading or set of readings different from the normal (expected) readings.

In-Situ Measurement: Measurement conducted during a test, i.e., in place, rather than during an interruption of a test condition. (IPC-JEDEC-9702)

Interconnect: Conductive element used for electrical interconnection, e.g., solder ball, lead, wirebond, PB, etc. (IPC-JEDEC-9702)

Land Grid Array (LGA): A solderable surface scheme where the surfaces are in an array pattern. Sometimes LGA components are BGA components without the solder balls.

Model: A formula or set of formulas that represent mechanical or thermo-mechanical behavior for BLR. Numerical simulation is one type of modeling.

Non-Area Array Component: A component that has terminations arranged around the periphery of the package in either a leaded or leadless configuration. This includes components with end cap terminations such as chip capacitors and resistors. (IPC-JEDEC-9704)

Printed Board (PB): A printed board is the planar structure to which electronic components are attached to complete a functional electrical circuit. Also known as a printed circuit board (PCB) and printed wiring board (PWB). (IPC-JEDEC-9701)

Reliability: The ability of a product (surface mount solder attachments) to function under given conditions and for a specified period of time without exceeding acceptable failure levels. (IPC-9701)

Second Level Assembly: The attachment of a component to the next level of assembly packaging (e.g., printed board). (JEP150-01)

Solder Joint: A solder connection between two separate metal surfaces.

Solder-Joint Reliability: The life of solder-joint interconnects between a printed board and an electronic component.

Surface Mount Technology (SMT): Components and systems that allow assembly to a printed board surface (no through hole components).

Test Vehicle: Test vehicles for BLRT may be specially designed electrical connections (daisy chains) in standard packaging, live product, or failed live product. (See DUT.)

Transient: An intermittent event of elevated electrical resistance or other changed electrical or physical parameter.

Warpage: The bow or twist of a surface out of a uniform planar flatness. Frequently caused by temperature (e.g., reflow) and humidity.

Young's Modulus: A measure of a material's stiffness in compression or tension. Important for BLRT since organic materials can have an abrupt change when crossing the glass transition temperature (Tg).

1.4. Roles and Responsibilities

Appendix 6 provides an illustration separating whether the Tier 2, supplier, or the Tier 1, user, are responsible for a specific reliability effort. BLR includes a cross-over in responsibility.

2. GENERAL METHODOLOGY

2.1. Objective

The objective of this document is to establish a board-level reliability (BLR) test methodology that defines procedures and guidelines to perform an assessment of thermo-mechanical or mechanical robustness of a component when mounted on a printed board (PB) and subjected to the specified stress test conditions. The procedures and guidelines to complete this assessment are divided into this base document that defines the basic methodology for the testing and one or more attachments that defines the procedures and guidelines for a specific stress test to be completed.

2.1.1. Stress Testing

The stress testing to be used with this guideline is contained within the test method attachments of the base document: e.g., AEC-Q007-001. Generally, the stress testing to be applied will continue until a certain level of failures occurs or an extended test duration is reached.

2.2. Precedence of Technical Documents

In the event of conflict in the procedures and guidelines of this document and those of any other documents, the following order of precedence applies:

a. This document and if applicable, its attachments
b. The reference documents in Section 1.2 of this document

2.3. Use of Generic Data to Satisfy Board-Level Reliability

2.3.1. Definition of Generic Data

The use of generic data to simplify board-level reliability (BLR) data gathering is an acceptable method. If the supplier elects to use generic data for any test results, the specific test conditions and results should be available to the user. (Note, the user may not accept the presented generic data if not technically justified by the supplier.)

Appendix 1 (the BLR Product Family definition) defines the factors or criteria by which components are grouped into a BLR Product Family for the purpose of characterizing solder joint and interconnect lifetimes.

2.3.2. Failures in Generic Data

Board-level reliability testing by the specific test methods specified herein deliberately seeks out when a printed board test assembly (PBTA), component and printed board, fails. DUT end-of-life failures (aka events) are necessary to establish the statistical distribution by which correlations to other environmental conditions can be made. Therefore, a failure distribution should be expected as an outcome from the generic data stress test. Generic data should have the same expected failure mode.

2.3.3. Guidelines for the Acceptance of Generic Data

The generic data must come from the same component or a representative component in the same BLR product family, as defined in Appendix 1. Potential sources of data could include any user specific data (withhold user name), process change qualification, and similar occurrences (see Figure 1: Generic Data Time Line). There are no time limits for the acceptability of generic data.

Note: BLR Ongoing Reliability Monitoring (ORM) is not required by this AEC document. Additionally, any supplier-user agreement requiring ORM shall remain in effect.

2.4. Test Samples

2.4.1. Test Sample Guidelines

Test samples shall consist of a representative device from the BLR Product Family. If used for generic data, then the device should be the family member that is expected to exhibit the worst-case BLR test results. The selection of the worst-case family member requires a technical justification and should be based upon the BLR Product Family definition (Appendix 1) and the BLR Change Matrix (Appendix 2). It is the supplier's responsibility to present rationale as to which value for each factor can be considered worst-case or the most sensitive to BLR type stresses.

Note: A representative device can and should be of a specialized type (e.g., a daisy chain, see Section 4) to allow interconnect monitoring.

2.4.2. Production Guidelines

All devices under test should be produced on tooling and processes that represent those at the manufacturing site that will be used to support part deliveries at production volumes. Deviations from production tooling and processes should be described in the final data submission report. Figure 1 provides a timeline for BLR data collection and in that the first supplier BLR effort should use the production processes and materials.

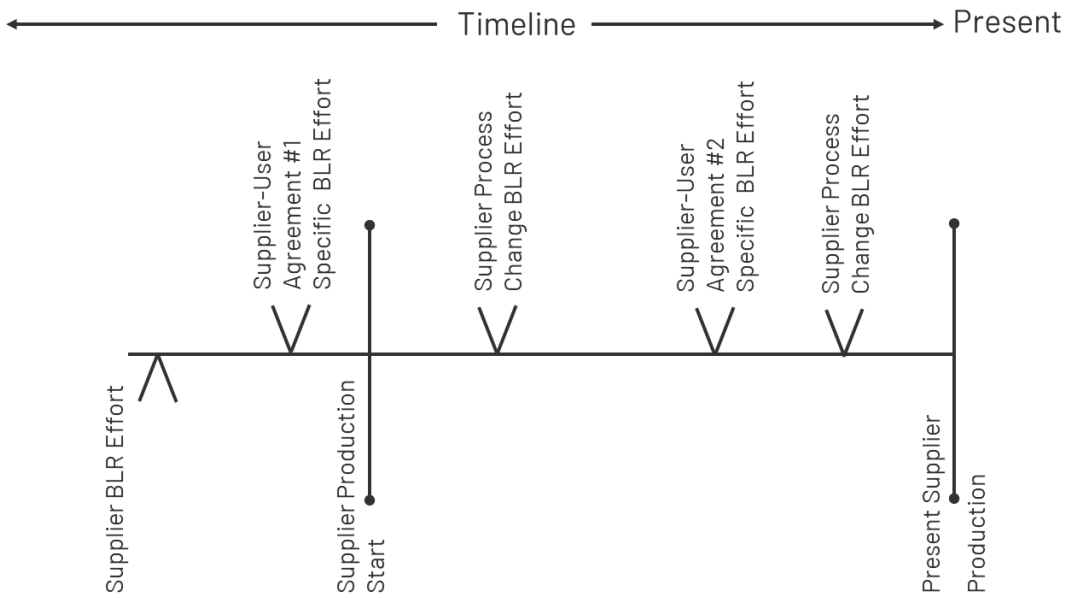


Figure 1: Generic Data Timeline

2.4.3. Reusability of BLR Test Samples

Unless allowed by individual BLR test methods, test samples shall not be reused.

2.4.4. Sample Size

Sample sizes for each individual stress test can be found in the applicable test method attachment (e.g., AEC-Q007-001).

2.4.5. Pre-, Interim- and Post-Stress Test Electrical and Physical Analysis

Preliminary, interim and post-test electrical and physical analysis are defined in each stress test method BLR attachment and in Appendix 4.

2.5. Definition of Test Failure During Stress Testing

Unless specified in an individual BLR test method, test failures are defined as those devices that exhibit a condition, characteristic or event that indicates there is a changed (e.g., elevated) resistance or open circuit in the monitored daisy chain circuitry exceeding a predefined level and/or duration. See Table 1 for a specific definition of a test failure.

Board-level reliability testing is intended to test to failure (end of life, EOL). Other failures including mishandling, electrical overstress (EOS), electrostatic discharge (ESD), etc., may occur. These other failures, when confirmed, may be removed from the EOL distribution.

Table 1: Test Failure Definition

Typical measurements when using event detector type of measuring equipment			Test Vehicle Daisy Chain Level		
	Measurement type	Measurement type details	Substrate	Leadframe	Wafer Level
Electrical Monitoring Type	Continuous glitch event monitoring	1 microsecond for shortest electrical discontinuity detection preferred. (2) 1 minute or shorter spacing between polls per channel.	●	●	●
Electrical Failure Definition	Absolute Threshold	Common values are ≥300 (Ω) and ≥1000 (Ω).	●	●	●
	Event Repeatability	10 events (failures) must occur within 10% of the present cycle count or within a maximum of 100 cycles, whichever is smaller.	●	●	●

Typical measurments when using datalogger type of measuring equipment			Test Vehicle Daisy Chain Level		
	Measurement type	Measurement type details	Substrate	Leadframe	Wafer Level
Electrical Monitoring Type	Continuous electrical resistance monitoring	1 millisecond for shortest electrical discontinuity detection preferred. 1 minute or shorter spacing between polls per channel.	●	●	●
Electrical Failure Definition	Absolute Threshold	Variable resistance settings (1) by analysis software/hardware.	●	●	●
	% Change Threshold	a.) Constant value above hot temperature reference, e.g. 20% rise in resistance (Ω). (3) OR b.) Reference value follows temperature cycling natural variation, e.g. 20% rise in resistance (Ω). (3)	●	●	●
	Event Repeatability	10 events (failures) must occur within 10% of the present cycle count or within a maximum of 100 cycles, whichever is smaller.	●	●	●

Notes:

1. Resistance is used for convenience in Table 1. Current or voltage are possible alternatives.
2. The 1 microsecond for glitch time width source is per IPC-SM-785 and IPC-9701.
3. The 20% rise value source is per IPC-9701.
4. A dot in the right-hand columns means the failure definition applies to the package.
5. See Section 4 for more details on substrate, leadframe and wafer level failure definitions.

3. CHARACTERIZATION AND RECHARACTERIZATION

3.1. Characterization of a New Surface Mount Component

The board-level reliability characterization test methodology of a new device or package is found in the applicable AEC-Q007 test method attachment(s). A characterization is the results from one or more completed test method experiments. For each characterization, the supplier must have applicable data available, whether it is test results on the device to be qualified or an acceptable generic data. A review should also be made of other devices in the same generic product family to ensure that potential failure mechanisms within the family are covered by the DUT. Justification for the use of generic data, whenever it is used, must be demonstrated by the supplier.

For each device characterization, the supplier must provide the following, upon request:

- Certificate of Design and Construction or equivalent
- Stress Test Characterization data
- Report the specific test conditions that were utilized in the testing

3.2. Recharacterization of a Surface Mount Component

Recharacterization should be considered when the supplier makes any change to the product and/or process that impacts (or could impact) the BLR characterization results. Any changes to the product, as defined in Appendices 1 and 2, needs consideration for performing the tests or numerical simulation listed in Table 2A and to determine the appropriate recharacterization test plan. If recharacterization is not performed, this should be technically justified by the supplier.

Note: Other AEC specifications, user specific expectations, and other industry standards (e.g., PCN-Delta-Qualification-Matrix-ZVEI) may have additional comments on when BLR recharacterization is recommended.

4. TEST VEHICLE: DAISY CHAIN DEVICE

This section describes the various possible daisy chain device constructions and some of their advantages and disadvantages. The electrical daisy chain is an electrically conductive path composed of the printed board and the device under test (DUT) that can be connected in series to form a continuous electrical net. Low ohmic conductive nets are preferred.

4.1. General Daisy Chain Recommendations

The daisy chain device is a simplified DUT which should be representative of the production device with respect to the bill of materials (including the construction and supply chain). Appendix 2 Table 2A lists the features that should be considered in the construction of the DUT for the relevant package technology. In any package configuration, a representative semiconductor die should be physically present in the DUT due to its difference in (thermo)-mechanical properties with other materials composing the DUT.

If the targeted device has multiple dies, including stacked dies, or passives, those need to be physically present in the DUT. The possibility to include those die in the electrical daisy chain net should be considered.

The daisy chain should be electrically isolated from any semiconductor [front-end (FE)] and substrate layers that are not intended to be part of the routing of the electrical daisy chain.

4.2. Daisy Chain Levels

The complexity in modern semiconductor devices allows different complexity levels for the DUT. From a daisy chain level 3 to a level 0, the complexity in design and manufacturing of the daisy chain is

increased. Descriptions of daisy chain level can be found below. The effort to validate the daisy chain design and to recover from errors increases while going towards level 0.

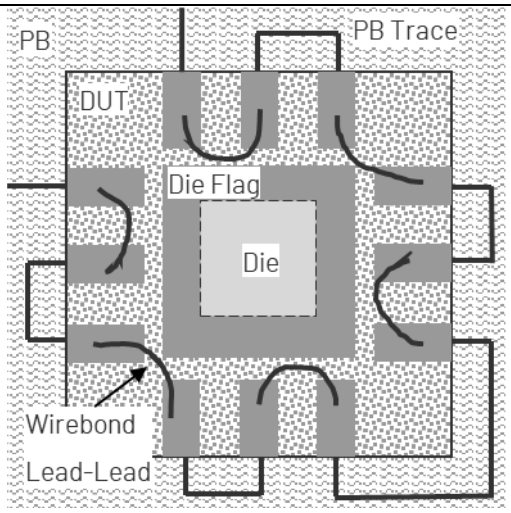
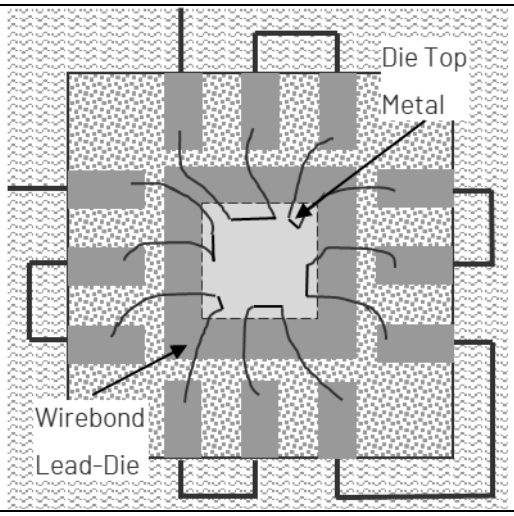
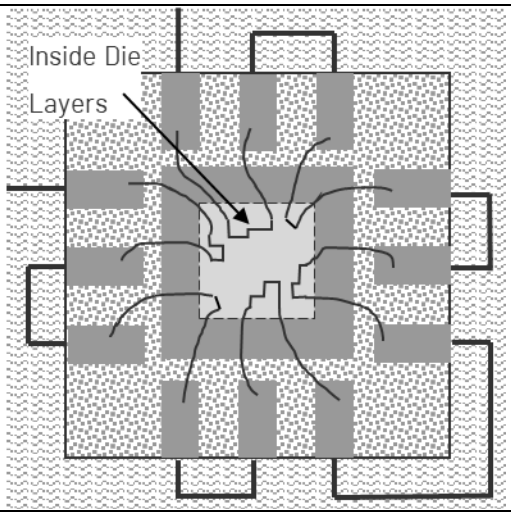
DUTs have been and will continue to be mostly Level 3 (BGA packages) or Level 2 (QFN, QFP and WL-CSP). More complex DUTs exist where internal interconnects are included and therefore, they are Level 1 and 0 daisy chains.

4.2.1. Leadframe Based Packages

Leadframe based packages are packages with one or more semiconductor die mounted on a metal (usually Cu) lead frame, over molded and with terminals protruding from the package body shaped either to a gullwing lead or J-lead, such as SO, QFP and their related types. Leadless leadframe based packages have similar construction with bottom terminated pads (no leads), such as QFN, multi-row QFN, SON, etc. The connections inside the package comprise wire bonds and/or flip-chip bumps depending on the device. For leadframe based packages, several different levels may be used to route the connections in the DUT (see Figure 2).

The leadframe layout for the daisy chain should be as close as possible to the actual device. In case pins are skipped or shorted in the actual device, a similar layout may be used for the daisy chain.

For wire bonded devices, in case of daisy chain level 2, double wire bonds may be considered to ensure robustness of the connection in the daisy chain. For daisy chain level 1 and 0, the wire bonds should have ball and stitch bonds representative of the actual manufacturing process. Similarly, flip-chip bumps should be representative of the actual manufacturing process.

<table>
<tr><th>Level 3</th><th>Level 2</th></tr>
<tr><td>Not applicable for these package styles.</td><td> 
</td></tr>
<tr><td></td><td>Solder joints only.</td></tr>
<tr><th>Level 1</th><th>Level 0</th></tr>
<tr><td> 
</td><td> 
</td></tr>
<tr><td>Solder joints and some coverage of interconnects such as wire bonds and/or flip-chip bumps up to the FE top metal.</td><td>Solder joints and some coverage of interconnects such as wire bonds and/or flip-chip bumps and the build-up layers of the FE.</td></tr>
<tr><td colspan="2">Figure 2: Daisy chain levels for leaded and leadless packages: an example top view of a transparent package with wire bonds (Flip-chip bump designs would be similar).</td></tr>
</table>

4.2.2. Substrate Based Packages

Substrate based packages are surface mount packages with one or more semiconductor die mounted on a laminate/organic or ceramic substrate and internally connected with wire bonds and/or flip-chip bumps, with an (area) array of solder balls for external electrical connections, examples BGA, FCBGA, etc. This family also contains packages with no balls attached, such as LGA, FCLGA, etc. For substrate-based packages, several different levels may be used to route the connections in the DUT (see Figure 3).

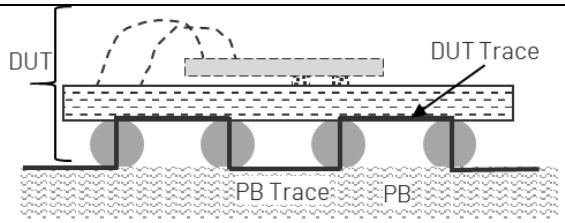
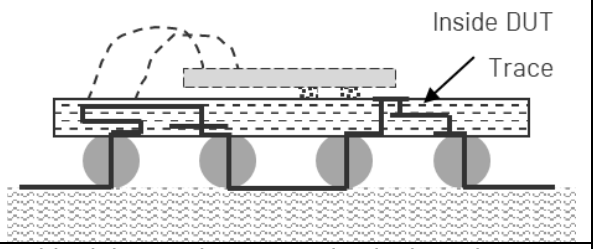
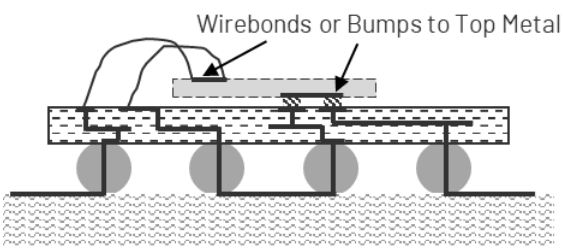
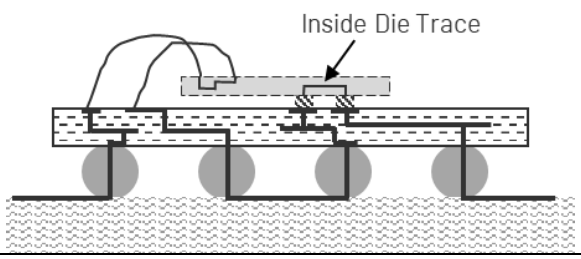
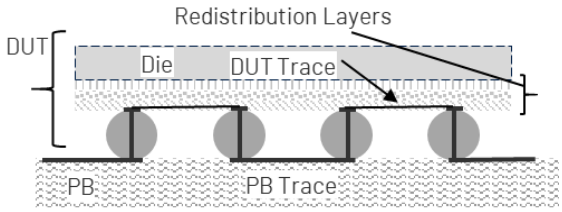
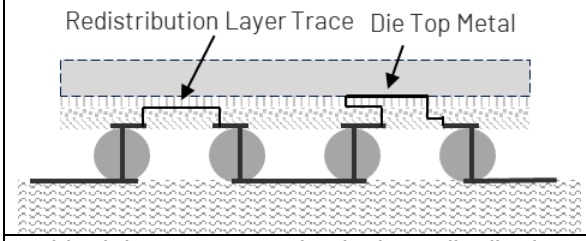
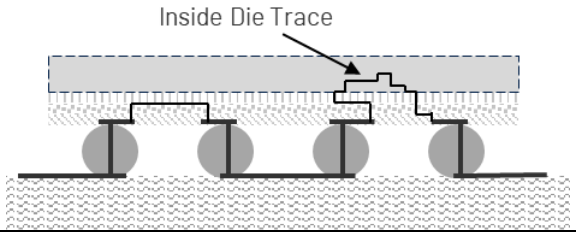
Level 3	Level 2
	
Solder joints only.	Solder joints and some routing in the substrate.
Level 1	**Level 0**
	
Solder joints, some routing in the substrate and the wirebonds and/or flip-chip up to the FE top metal.	Solder joints, some routing in the substrate and the wirebonds and/or flip-chip up to the interaction with the FE build-up layers.

Figure 3: Daisy Chain Levels for Substrate-Based Packages

Note: Both wire bonds and flip-chip bumps are shown in a single image for simplification purpose. For daisy chain level 1 and 0, the wire bonds should have ball and stitch bonds representative of the actual manufacturing process. Similarly, flip-chip bumps should be representative of the actual manufacturing process.

4.2.3. Wafer Level Packages

Example wafer level packages include WLCSP, FOWLP, etc. For wafer level packages, the different levels are described in Figure 4.

<table>
<tr><th>Level 3</th><th>Level 2</th></tr>
<tr><td rowspan="2">Not applicable for these package styles.</td><td> 
</td></tr>
<tr><td>Solder joints and some routing in the redistribution layers</td></tr>
<tr><th>Level 1</th><th>Level 0</th></tr>
<tr><td> 
</td><td> 
</td></tr>
<tr><td>Solder joints, some routing in the redistribution layer and connection to FE top metal.</td><td>Solder joints, some routing in redistribution layer and connection to FE top metal and build up layers.</td></tr>
<tr><td colspan="2">Figure 4: Daisy Chain Levels for Wafer Level Packages</td></tr>
</table>

4.2.4. Risk Coverage for the Different Daisy Chain Levels

For all the daisy chain levels, the board level reliability test assesses the risk of solder-joint failure. The daisy chain levels 2, 1 and 0 allow the experimenter to additionally assess internal interconnect failure modes caused by thermo-mechanical stress transfer from the PB into the package.

Table 2 summarizes the risk coverage for the different daisy chain levels.

For the daisy chain levels 1 or 0, the reuse of the data to cover risks related to the interaction with the semiconductor die (either interaction with top metal or inside the build-up layers) between devices should be justified. Additional complexity in analyzing the test results and failure analysis can result from the use of those levels.

For daisy chains connecting the top metal or the semiconductor build-up layers, the total resistance of the daisy chain device can significantly increase and should be checked against the capability of the in-situ detection method used. For daisy chain level 0, additional precautions can be needed due to potential ESD sensitivity in the daisy chain.

The daisy chain level of a package is defined by its electrical interconnect routing closest to the wafer. For example, daisy chain routing with part of the link in the substrate and in the semiconductor top metal is categorized as level 1.

Table 2: Daisy Chain Level Connections and Risk Coverage

Level	Item	Description
Level 3	Routing inside DUT	Connections are only made at the bottom layer of the substrate.
	Risk covered	Solder joints only. See also Figures A4.1 – A4.3.
Level 2	Routing inside DUT	Connections are made in substrate top layer traces, at a leadframe level (e.g., wire bonds) or in a redistribution layer level
	Risk covered	Includes level 3, and some coverage of connections in the substrate, leadframe or redistribution layer.
Level 1	Routing inside DUT	Connections are made using wire bond or bump interconnects to connect to the die top metal.
	Risk covered	Includes level 2 and some coverage of the interaction with the top metal.
Level 0	Routing inside DUT	Connections are made using all previous levels to connect the build-up layers (e.g., die metal layers, low-k dielectric layers).
	Risk covered	Includes level 1 and some coverage of the interaction with the build-up layers.

4.2.5. Test Failure Definition by Daisy Chain Level

The definition of test failures may differ depending on the daisy chain level used. (See Appendix 3, Table 3A.)

4.3. Daisy Chain Configurations

4.3.1. Critical and Redundant Solder Joints and Other Interconnects

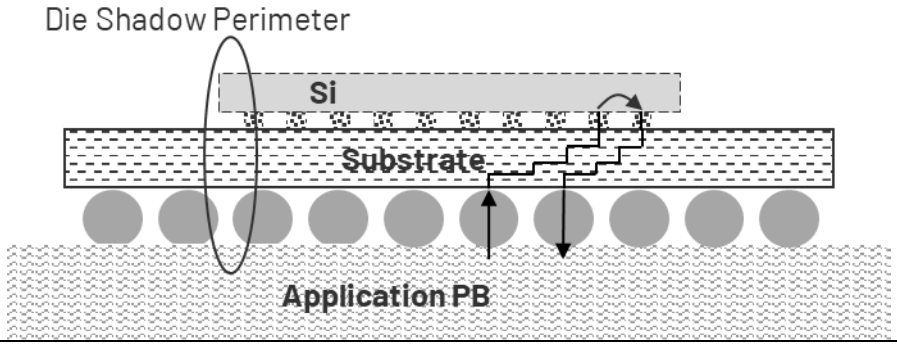
Connections (solder joints and other interconnects) which are redundant with respect to the electrical performance of the device may be omitted from the electrical daisy chain. For example, redundant solder joints can be power or grounds, for which the failure of the solder joint would not impact the electrical functionality of the device. Another example are the pins called No-Connects (NC) or Do-Not-Use (DNU). Those solder joints are often considered sacrificial and typically improve the device solder-joint reliability. In such a case, it is recommended to collect the data of redundant solder joints in a separate net (see Figure 5).

Note: Redundant, No-Connect, Do-Not-Use, etc., solder joints are expected to be soldered to the BLR printed board.

Thermo-mechanically critical interconnects should be in the daisy chain. Examples of critical interconnects include:

- The interconnects that are critical to the electrical functionality of the device pin layout, in a way that the failure of such an interconnect would lead to a failure of the device. Assistance in reviewing the device pin layout from design/application teams can be needed.
- The interconnects that are located at positions which are subjected to higher mechanical or thermo-mechanical stress during stress testing. Examples are solder joints at the corner and in the neighborhood of corners of a package or under the die shadow perimeter, (see examples in Figure 5).

The omission of interconnects in the daisy chain routing based on electrical performance considerations of the device can limit the reuse of data.



Example of routing for daisy chain level 1/0 using solder joints with long life

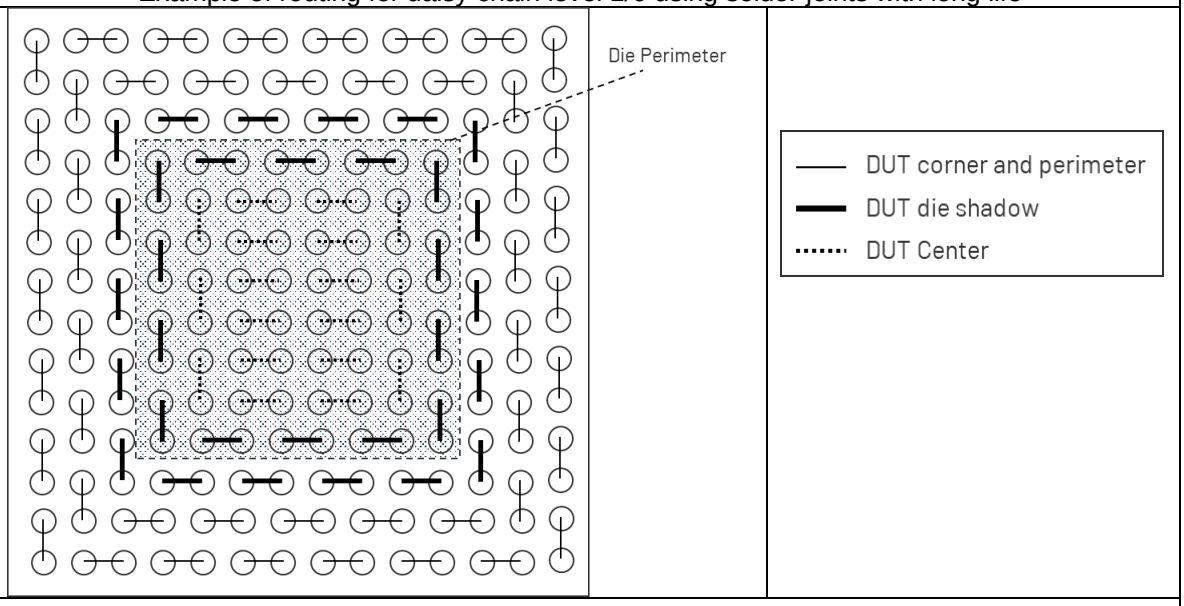


Figure 5. Example of DUT routing with 3 subnets to assess different areas

4.3.2. Usage of Daisy Chain Nets

For all daisy chain levels, the use of subnets can be considered to assess the reliability of specific solder-joint areas under the package such as at the perimeter or center of the package and/or to potentially ease the failure analysis.

For daisy chain levels 1 and 0, in order to monitor the connections inside the DUT, it is recommended to use sub nets of the daisy chain (typically less critical solder joints, with long life), with dedicated printed board test pads. Those test pads help with failure localization and subsequent failure analysis (Figure 9).

Die shadow is the full area under the silicon. Mechanically the solder joints most likely to be impacted by the die shadow are those at the die perimeter where the discontinuity of material properties has a large influence. For BLR, the die perimeter is a critical consideration.

4.3.3. Using Actual Devices

An alternative or supplementary method to assess board level reliability is to use production devices instead of daisy chain devices. The use of such devices should be justified and agreed to between supplier and user in case the data are used to assess BLR. Also, the BLR stress test may not replace any test from the AEC-Q10x and AEC-Q200 specifications unless discussed and agreed to between the supplier and user.

In such a discussion, the advantages and disadvantages of using an actual device mounted on a printed board should be weighed. Typical advantages include the use of final test for the device and the resemblance to the actual device. The disadvantages could be related to the challenges in the stress test execution, the need to test the device while still mounted on a printed board, as well as the use of read point measurement at a fixed ambient temperature instead of continuous monitoring. Electrical test based on the datasheet with PB created limitations should be agreed upon by the supplier and user.

Guidelines related to stress tests on assembled devices can be found in JEP150. For BLRT, the sample size should be 1 lot and equal to or larger than the daisy chain DUT sample size recommendation.

4.3.4. Application to Passive and Discrete Devices

Electrical passive devices belong in three main categories: resistors, capacitors and inductors.

For all these categories, two basic physical descriptions are necessary: total body/package size and expected solder-joint size. As body size increases, the distance from neutral point (DNP) increases, a reduced solder-joint life should be expected. DNP refers to the solder joints and not to the total device package size.

Passives generally do not require designing a unique test vehicle. What follows are suggestions on factors to look for in a production part and how to possibly use them in a board-level reliability experiment. Other considerations can be made and are not limited to the provided examples. The suggestions can be used for in-situ monitoring with proper equipment.

For resistors, the body size and solder-joint size are the mechanical factors of interest. The test vehicles should have low resistance values (e.g., 1 to 100 Ohms) in order to detect a resistance change in the interconnect.

In a direct current setting, inductors can be considered as a resistor where the direct current resistance is the “resistor” value. For an equal body size, picking a low inductance part is preferred. This will keep possible mutual inductance to a minimum. Measurement accuracy can be improved by using a low current level.

Capacitors are high resistance elements. Therefore, an in-situ monitoring test, detecting for a change from low to high resistance may not be applicable. Instead, curve tracing can be considered. With the current being out of phase with the voltage input, a measuring system will have a response circle to monitor. The number of points to be monitored in that circle will depend upon the measurement equipment. Frequency can be used to reduce the circle to an almost vertical line (a large current change with a small voltage change). Alternatively, readpoint measurements may be the easiest technique.

For other types of passives, e.g., frequency devices, suppliers make the determination if in-situ monitoring is feasible. Readpoint monitoring at fixed intervals may be the only technique available.

For discrete devices, there are in general 3 possibilities depending on the device construction. 1.) For the package constructions which are similar to semiconductor die, the guidelines provided in the Sections 4.2.1 – 4.2.4 can be followed. 2.) Schottky diodes or diodes in the forward bias direction with a low breakdown voltage can be used during board-level reliability in combination with in-situ monitoring. 3.) An alternative to the previous two possibilities is to use actual devices. In such a case, some of the guidelines provided in the Section 4.3.3 apply.

For discrete devices with a low and odd number of pins (e.g., 3 pins), it is recommended to create 2 different daisy chain configurations to connect pins alternately. As an example, for a device with 3 pins, a connection between pin 1 and 3 for the first daisy chain and a connection between pin 2 and 3 for the

second daisy chain can be used. In such case, each daisy chain configuration should be stress tested with the original sample size.

Suppliers should optimize the number of pins used in daisy chain packages based upon package construction and anticipated usage. Excluding one or more pins is possible if a technical justification can be documented.

5. PRINTED BOARD DESIGN GUIDELINES

The printed board (PB) design plays a critical role in board-level reliability results. The guidelines provide a reference for factors that are preferably standardized to minimize variability between suppliers. Standardization will help with test result comparisons, with surface mount assembly and to support numerical simulations using finite-element methods (FEM).

5.1. Recommended Printed Board Stackup

Figure 6, PB Cross-Section, shows the schematic representation of an 8 Cu-layer High-Density Interconnect (HDI) PB stackup. The commonly used via types in PB design are included. The AEC-Q007-002 spreadsheet “PB” tab lists design parameters to record.

A 1.6 mm PB thickness is preferred. Assembly lines at users (Tier 1) are frequently optimized for a PB thickness regardless of Cu layer count. Thus, 1.6 mm thick boards on a single assembly line may have 4, 6 and 8 Cu layers by application and yet require no surface mount assembly changes for that difference.

The recommendation of 8 Cu layers provides to the AEC community several advantages. The 8 Cu layer PB provides by industry experience a lower temperature cycle count to solder-joint failure compared to 4 and 6 Cu layer PBs with equal thickness. This comes from the PB CTE and Young’s modulus which are a cumulative effect of layer count, thickness and material properties. These factors also influence, for example, PB bend stiffness. Additionally, the industry is moving to more Cu layers, though 4 and 6 Cu layers will remain in broad use for many years to come.

There is variation in the naming conventions for Cu-layers. Some PB designers will name the layers #1 to #8 while others will use Top, #1-#6 on inner layers and Bottom. Commonly, the 8 Cu-layer board shown in Figure 6 is called 3-2-3. For this reason, a schematic drawing explaining the stack-up and naming convention should illustrate the PB design in the BLR report. The schematic drawings can be found in formal PB fabrication drawings.

The Cu thickness is a key factor and should be targeted at a finished value of 35 microns (1 oz). Alternative Cu thicknesses for an expected automotive market may be considered. It is important to note that the top and bottom Cu-layers 1 and 8 (Figure 6) should be the thickness after final plating and pad shape forming. The surface finish is ignored in the Cu-layer thickness.

The vias are critical for electrical routing in a PB. There are several ways to design/fabricate micro-vias, (Figure 6, A, B, and F). IPC 2221 and IPC 2222 should be referred to when designing standard rigid PBs. IPC 2226 and IPC 7095 should be consulted for information specifically for HDI PBs. Stacked vias should be avoided (Figure 6, F).

For daisy chain routing the AEC recommends that vias be used sparingly. It is not desirable that the vias fail before the daisy chain loop.

Filling vias with epoxies or metal is a consideration. The experimenter is encouraged to inquire with the PB fabrication company and also with the possible users on what choice to make.

Using an HDI style PB will depend upon the routing complexity, the expected market for which the BLR study is intended and also on supplier-user agreements. HDI is realized by smaller Cu-trace lines and smaller spacing between traces, as well as the use of micro-vias (Figure 6, A, B, and F) and buried vias

(Figure 6, D). HDI build-up technology becomes increasingly common as total layer count increases. In case HDI features are not required for daisy chain routing for a particular component, it is considered appropriate to use a non-HDI PB with plated through holes.

The test board material should match the expected PB composition, for example, FR4 epoxy/glass laminate, of the intended automotive application.

For both numerical simulation and for experimental results comparisons, the material properties, Cu thicknesses, laminate thicknesses, total thickness and similar parameters should be thoroughly documented. The recommendation is for direct measurements of PB CTE (X, Y and Z), modulus and Tg. CTE measurements ideally would be over a range of temperatures recommended for the experimental test condition, e.g., BLR-TCC-1 -40 to 125C. If possible, testing to a higher temperature is valuable for assessing reliability margin.

Note: Techniques for CTE measurements include dilatometry, interferometry and thermomechanical analysis.

Numerical simulation representations can be called a “digital twin”. To be a fair representation, correct material properties are necessary. If not correct, then the digital twin cannot provide guidance on whether changes should have recharacterization. If material properties are not available or are known to be incorrect, a full BLR experimental characterization should be obtained for even minor changes.

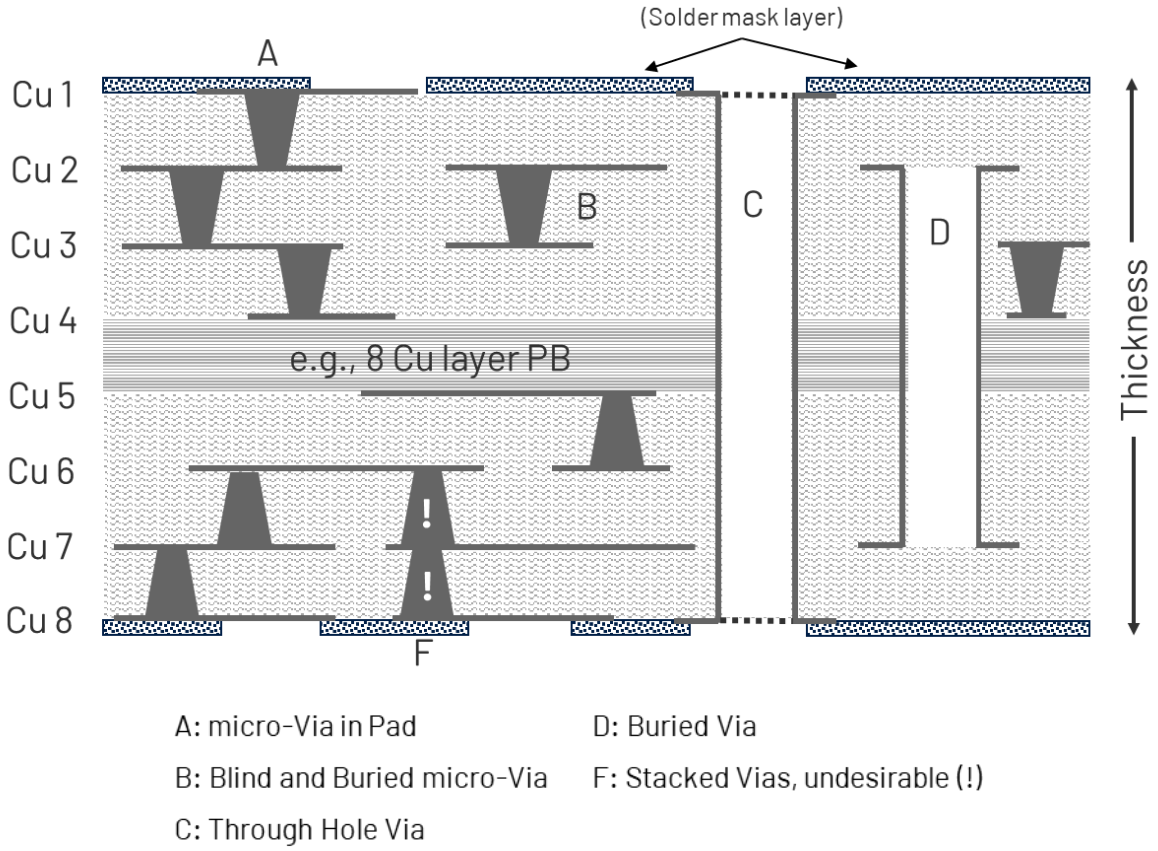


Figure 6: Schematic Printed Board Cross-Section (not to scale)

Suppliers should consider making a single thorough experimental material property measurement set and use those going forward. Examples of changes that could trigger new material characterization include:

- One or more printed board materials change
- One or more printed board laminate layer thickness changes
- Cu thickness on layers change by more than 50%, especially for the top and bottom Cu layers
- Printed board fabrication process changes, especially any deliberately involving heat and/or pressure
- Printed board via density under the DUT and within a 25% distance from the package edge
- Cu fill changes by more than 25% in total area covered (excluding manufacturing keep-out zones)

5.2. Printed Board Pad Style

Choosing the PB pad style has an impact on board-level reliability. There are two styles of pads. These are called NSMD (non-solder mask defined) and SMD (solder mask defined). The NSMD pad has the solder joint soldered to a PB pad that is mostly exposed Cu. SMD has the solder joint shaped by the solder mask that is deliberately on the Cu pad. The two styles are shown in Figure 7 below.

The NSMD pad has a spacing between the SM and solder joint. The SMD pad in contrast has SM contacting the solder joint continuously at the perimeter. Any contact by the SM to the solder joint reshapes the solder joint from spherical to one with a waist.

Failure mode and robustness margin are important factors in choosing between NSMD and SMD. Temperature cycling performance typically benefits with a NSMD pad. In contrast, mechanical tests (e.g., drop) typically benefit from the SMD pad style.

The SMD solder mask opening creates a pinch in the solder-joint shape. In solder-joint interconnect temperature cycling, the pinch is a stress riser leading to a shorter lifetime.

As a starting point, the NSMD pad style is recommended for BLR studies. The expected application, if known, should be considered for the PB pad design. The PB pad design should use the supplier application note if available.

For a BGA, if an application note does not exist the PB (NSMD) pad diameter is recommended to be ≤100% of the component (SMD) pad diameter and typically ranges from 80% to 100%. A supplier has immediate access to the package design files and should use that for defining the PB pad design. More comments may be found in Section 5.6.

Pad design recommendations for leaded and non-leaded packages can be found in reference documents. IPC-7093 Bottom Termination Components, e.g., QFN package style, is an example.

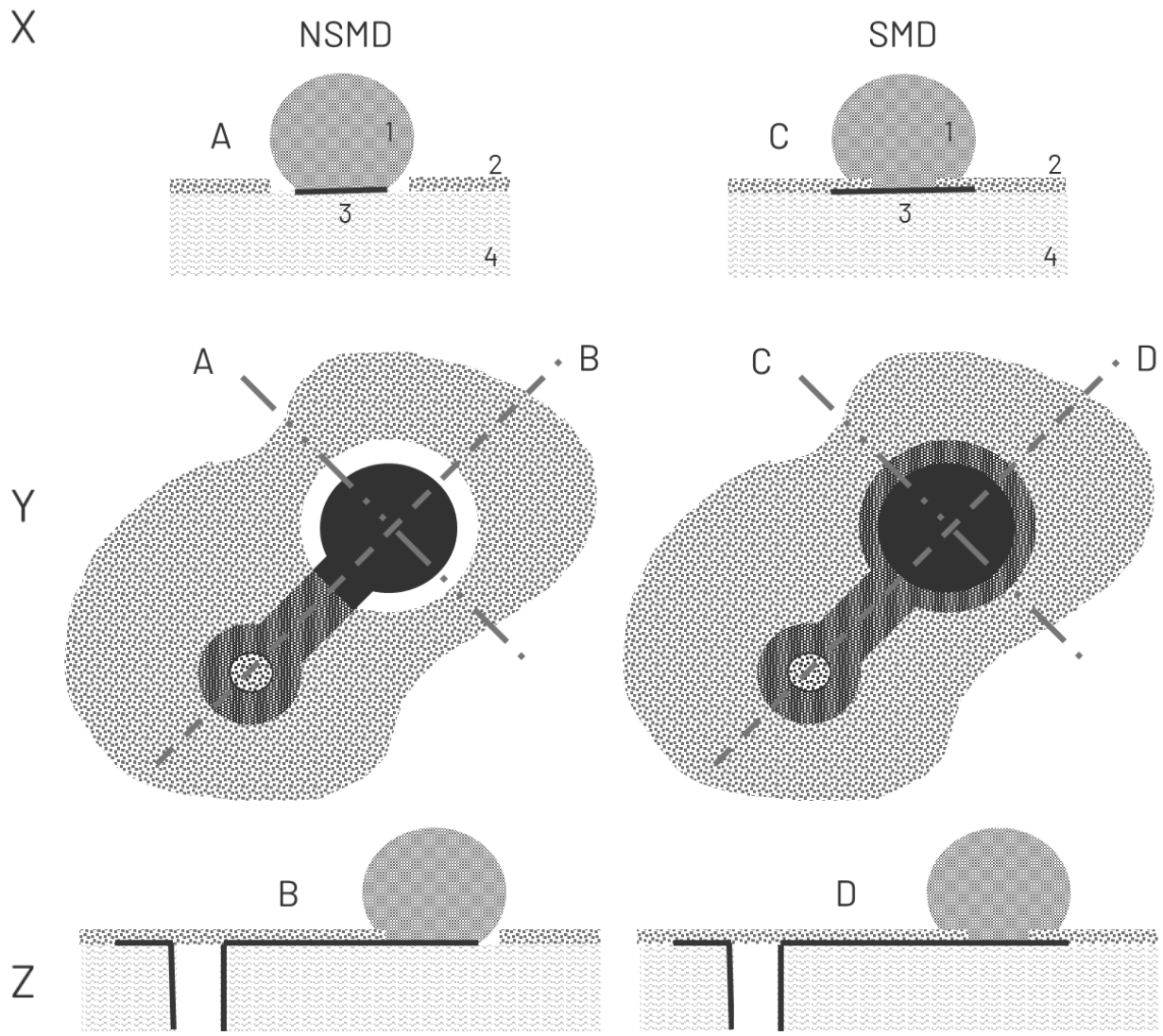


Figure 7: Printed Board Pad Style. The left column of images are for NSMD while the right are for SMD. The middle images, row Y, look down at the PB. The top images, row X, are a cross-section along the line A or C while line B and D views can be found in the bottom images, row Z. Except for where the Cu-trace exits to the via, solder mask is not on the NSMD Cu pad. The package side for the solder joint is not shown. Row X shows the solder joint (1) attached to the PB pad (3) and solder mask (2) covers the PB laminate (4). (Redrawn from IPC-7095.)

5.3. Printed Board Pad Surface Finish

The recommended standardization is to use Organic Solderability Preservative (OSP) to protect the PB pad Cu surface before SMT assembly. For general BLR data collection OSP will provide the broadest acceptance of results. Supplier-user specific agreements can lead to a different choice.

5.4. Cu Fill on Layers

The purpose is to mimic the Cu present in production boards and another purpose is to minimize warpage during both surface mount assembly and also in BLR temperature cycling. The industry references for PB warpage can be found in: IPC-6012DA, IPC-600 and IPC-2221, referring to warpage as 'bow and twist'. It is preferred that the PB warpage before and after reflow does not exceed the requirements given in IPC-6012DA.

Daisy chain PB routing as the only Cu fill layer will not represent a production PB. Additional Cu fill is needed to better match a production PB. The preferred % total Cu coverage on any layer should be 70 to 80% and approximately uniformly distributed across the horizontal plane. In case of high routing density on the top and bottom Cu layers and the recommended 70 to 80% Cu area coverage cannot be reached, it should be documented. Vertically the individual layers should have approximately the same Cu fill. Full Cu planes are also not representative of production PBs. PB designers usually have automated software tools to create Cu fill patterns.

5.5. General Remarks on Printed Board Design

As mentioned, the purpose of a BLR study is to gather general information about solder joint and interconnect life. The BLR test PB should be designed to represent a typical application in terms of pad designs and via structures. To do this the board design should avoid several factors that change, for example, cycles to failure. These factors may exist on a user PB but the supplier cannot be expected to test all possibilities. In fact, the supplier should ensure a semi-infinite area for the part under test that is stress free from forces other than, e.g., CTE mismatch.

There needs to be spacing between the components (Figure 8, U1-U4) under test. It is recommended that components should be at least 12.5 mm (0.5") away from each other. The distance measurement starts at the BGA or QFN package drawing edge. For a QFP, the spacing measurement would start at the lead toe, not the mold compound edge.

Experimenters may have data showing smaller spacings are possible or that larger spacings are needed.

For simplicity, only 4 components are shown in Figure 8. The experimenter can optimize the number of parts on a board. Optimization factors include the number of monitored nets per part, total number of nets that an event detector or datalogger can read, physical space available in a chamber, etc.

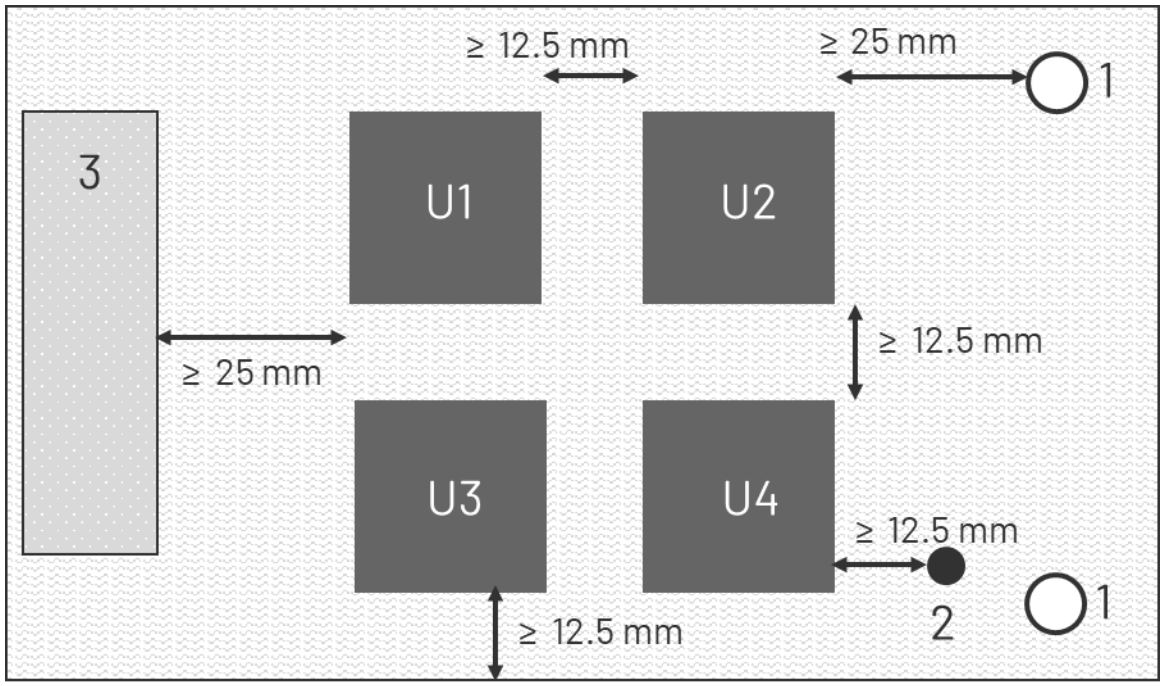


FIGURE 8: Example shows a 4-component test board with spacings between parts (U1-U4), to tooling holes (1), to a plated through hole via (2) and to an electrical connection area (3). Additionally spacing rules may be needed to fulfill printed board manufacturing best practices.

The tooling holes (Figure 8, #1), if any, are recommended to be at least 25 mm (1") away from the nearest component under tests. Tooling holes may disrupt the expansion, contraction and flexing of PBs during stress testing. Putting them close to a component's solder joint will change the experienced stresses. An example for how tooling holes impacted board-level reliability can be found here [*Impact of PCB-housing-interaction on QFN solder-joint reliability, Bart Vandevelde, et al., 21st EuroSimE, 2020*].

Note: The tooling holes (Figure 8, #1) to PB edge will have a distance rule. This rule should be confirmed by the PB designer.

Plated through-hole vias (Figure 8, #2) provide a useful mechanism to add localized test points and rerouting to a PB. These should generally be pulled away from the package. AEC recommends 12.5 mm (0.5") as a spacing rule. The exception would be thermal vias used with thermal pads. These should be present in a PB design but should be avoided for board level reliability monitoring.

Connectors (Figure 8, #3) allow a PB to be joined to a monitoring system but connectors can be very stiff compared to the PB. If space is available a 25 mm (1") spacing from the connector body to the nearest DUT is recommended.

For daisy-chain routing, additional test points (TP) on the PB isolating subnets of the full daisy-chain net can be useful. They help identify failure locations by a manual measurement using test probes. See Figure 9 for a simplified example.

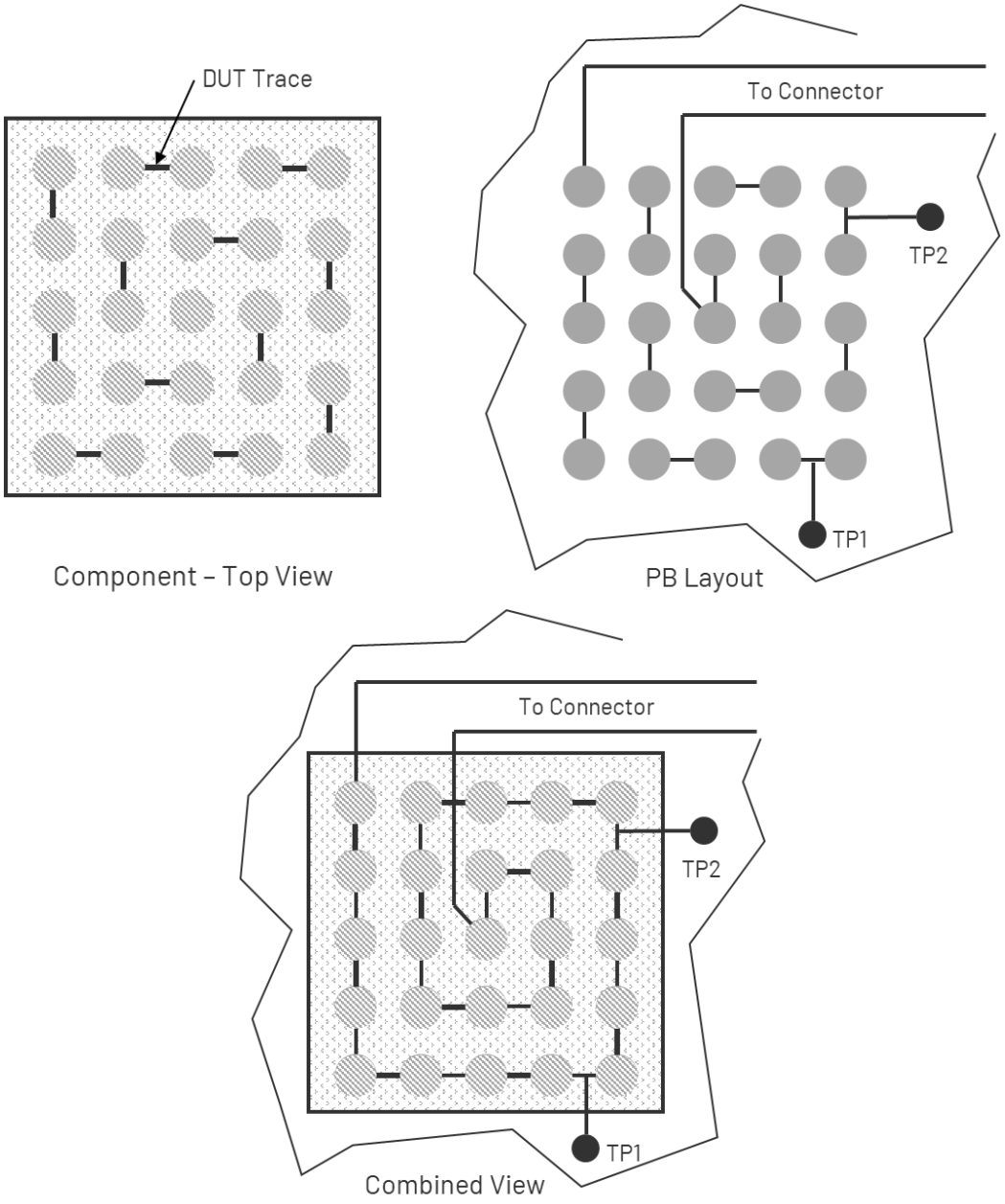


FIGURE 9: Example shows a subnet for manually testing the outer row of a 5x5 BGA using test probes at test points TP1 and TP2. The full daisy chain net is monitored using a connector (not shown). The top images show the component and printed board connections while the bottom image shows the entire daisy chain connection pattern.

Ideally the TP trace should not connect to a PB pad. However, if a trace must come out of the pad, steps should be taken to ensure the trace can survive BLR testing and that the trace does not interfere with the normal pad mechanical behavior. TP traces connected to corner pins in particular need extra caution.

TP's without vias can be placed near a component but should have sufficient spacing so a probe will not touch the DUT. For TP's with a via, spacings described in Figure 8 should be use.

During PB design, the individual DUT areas should be designed to assist failure isolation. The PB design should consider the ease at which an isolated DUT can be cut out without damaging the remaining DUTs.

5.6. Single-Sided and Double-Sided Design and Assembly

PBs can be designed to have the needed test vehicle circuitry on both the top and bottom sides. These designs may be the same or they may be different to allow more variations to be studied.

For BLR testing it is common that only one PB side is assembled and stressed. The single-sided assembly provides the fewest constraints in creating a digital twin for numerical simulation.

The notable exception would be memory components which are intended to be mounted back-to-back (top and bottom). Back-to-back component mounting can be mirrored or offset. If mirrored, the DUTs should be directly opposite each other. The choice of single-sided or double-sided assembly may depend upon the expected application, the supplier application note or the supplier-user agreement.

Part of PB assembly is the reflow process. For a single sided PB assembly only one reflow is necessary. Yet for real products there is a chance that a component would see two reflows. Therefore, two reflows are recommended for single sided assemblies to simulate the real world. The number of reflows used should be documented in the final report (see also Section 6).

5.7. Miscellaneous Printed Board Design Notes

Many BGA package outline drawings do not show the component pad size. Instead, they show the final solder ball diameter. A user conducting their own BLR work must confirm with the component supplier the actual BGA package pad size.

For failure analysis it has been useful to create PB designs where each component sits on an individual coupon. Each coupon is mostly separated from neighbors by both physical spacing and cut out slots in the PB. The few remaining connections at slot corners, e.g., allow the routing to and from the component under test. Slot spacing to an individual component should be at least the spacing for a through hole via and preferably larger (see Figure 8).

The PB design examples use ball grid array component packages for demonstration purposes. Both leaded and non-leaded packages can have similar interactions by the solder mask to the solder-joint shape and hence to expected life.

The Cu-trace connecting the PB pad to the via is drawn as a rectangle shape (Figure 10). Recommended is a tear drop shape leaving the PB pad. The tear drop shape is known to reduce the likelihood of Cu-trace cracking during board-level reliability testing and in final products.

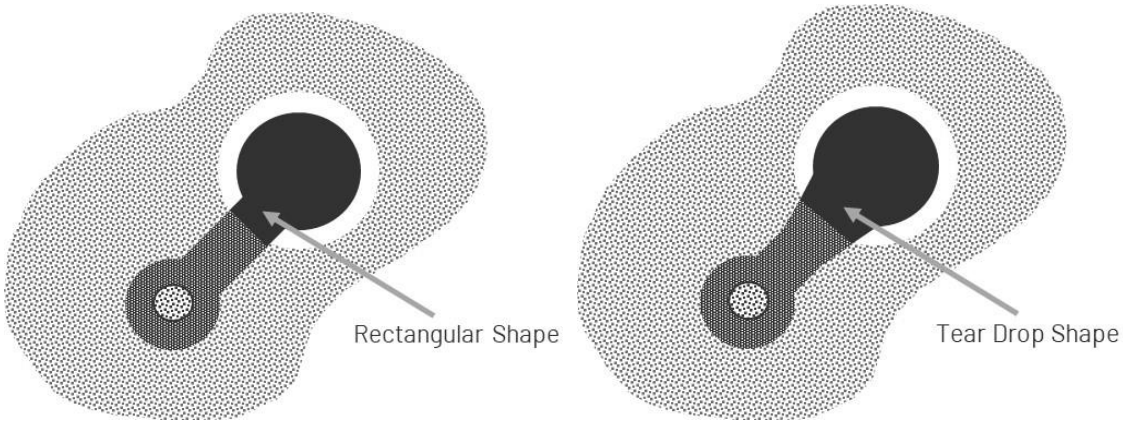


FIGURE 10: The left image is a rectangular shape Cu-trace connecting the via to the Printed Board pad. The right image shows the preferred tear drop shape from the pad that extends part ways under the solder mask.

While the Cu trace is not the test subject, its width is an important consideration in BLR testing. In and near the components Cu-trace widths will depend upon pitch and other factors. Away from the component, the Cu-trace should be widened to 0.2 mm or wider for increased robustness.

5.8. Printed Board Sourcing

The PB manufacturing process can affect BLR. For this reason, it is recommended to purchase BLR PBs from volume suppliers with known automotive electronics experience.

5.9. Printed Board Design Documentation

PB design and fabrication parameters should be documented in the AEC-Q007-002 Spreadsheet “PB” tab.

6. SMT ASSEMBLY PROCESSES

6.1. Remarks on BLR SMT

This section gives guidance on the SMT (surface mount technology) assembly process. In addition to best practices and relevant references to existing standards, a spreadsheet documents essential information about the SMT assembly process (see tab SMT in AEC-Q007-002).

SMT assembly for board-level reliability testing is usually done under low-volume non-serial production conditions. This is acceptable, but a close approximation with series production conditions should be strived for in terms of manufacturing equipment. In terms of process conditions, those should fall within the envelope of typical series production process conditions. Assembly materials (solder paste, flux, etc.) can have a pronounced effect on BLR and those should be selected to be representative of mass-production conditions. Recommendations, guidance and notes of caution are provided in the subsequent sections.

6.2. Pre and Post Assembly Storage of Assembled Printed Boards

IPC-1602 provides suggestions for proper handling, packaging materials and methods, environmental conditions, and storage for printed boards. These guidelines are intended to protect printed boards from contamination, physical damage, solderability degradation, electrostatic discharge (ESD) (when necessary), and moisture uptake. This guideline covers all phases from the manufacture of the bare printed board, through delivery, receiving, stocking and assembly.

6.3. Solder-Paste Printing and Inspection

Solder-paste printing should be accomplished at the panel level using standard stencil printing equipment, as this is commonly used in the automotive electronics industry. IPC-7525 provides guidance for the design and fabrication of SMT stencils.

In particular, guidance on aspect ratio and area ratio in IPC-7525 should be followed, i.e., stencil thickness and aperture size(s) must be matched to assure good printing quality. As an example, apertures too small for a given stencil thickness may result in poor solder paste release from the stencil and thus low or irreproducible solder volumes.

IPC-7527 supports the reader in the visual evaluation of the solder paste printing process, which makes subsequent process optimizing possible.

Misprinted boards should be scrapped.

Double-printing with an intermediate stencil lift is not acceptable as paste-printing results are typically not reproducible, but a double stroke of the stencil is acceptable.

The use of solder-paste inspection after printing using 2D or 3D (preferred) inspection systems is not mandatory but recommended.

6.4. Solder Paste

Solder paste should be in accordance with IEC 61190-1-2, J-STD-005 or equivalent. Solder flux in the solder paste should be in accordance with IEC 61190-1-1, J-STD-004 or equivalent.

Unless specifically agreed to between user and supplier, the lead-free alloy of composition Sn96.5Ag3Cu0.5 should be used with ROL0 type solder flux. Solder alloys should be in accordance with IEC 61190-1-3, J-STD-006 or equivalent. The solder powder particle size should be selected based on stencil design and part pitch, to enable a capable printing process (see Section 6.5).

6.5. Component Placement

Component placement should be accomplished using automated pick-and-place equipment from reels or trays. Manual placement is strongly discouraged due to a lack of placement repeatability and reproducibility. IPC-9850 provides guidance on surface mount equipment characterization.

6.6. Reflow

The solder paste should be reflowed using a modern infrared convection oven compatible with IEC 61760-1. IEC TR 60068-3-12 and IPC-7530 or equivalent provide guidance on determining a suitable reflow oven recipe/program for reflowing the solder paste for a particular populated printed board.

A soldering reflow profile, also known as a thermal profile, is a key variable in the manufacturing process that significantly impacts product yield, quality and reliability. The temperature process window for the actual solder profile is bounded above by the solder-heat resistance of components and printed boards and bounded below by metallurgical and chemical conditions of the assembly materials (e.g., by flux activation versus temperature, liquidus temperature of the solder alloy). The wettability of components terminations and printed board lands may also be impacted by the reflow profile.

Guidance on solderability, resistance to dissolution of metallization and to soldering heat of surface mounted devices is provided by IEC 60068-2-58. Moisture-sensitive components require special attention and guidance for such cases can be obtained by referring to IEC 60749-20, IEC 61760-4, J-STD-020 and J-STD-075.

Temperature profiling on the populated printed board should be made using suitable thermocouples with a datalogger during a reflow. IPC-7530 provides guidance for determining solder-joint temperatures during reflow. Thermocouples should be used in sufficient number and properly placed to profile the hot and cold printed board areas. If possible, a print-out of the results of the thermal profiling (tabular data – preferred – or PDF file) should be made available.

Reflow should be performed in dry air or nitrogen (< 1000 ppm O_2). O_2 levels can be compared/aligned to the solder paste data sheet recommendations. Other atmospheres require agreement between user and supplier.

The use of vapor-phase soldering is not recommended as this method is not commonly used in the mass production of automotive electronics.

6.7. Use of Underfill

If a component is expected to require an epoxy underfill for use in typical automotive applications, BLR testing should be conducted with and without underfill. Underfill material and process should follow recommendations provided in component supplier application notes and datasheets.

6.8. Post-Reflow Inspection

Reflowed panels should be inspected to IPC J-STD-001GA/IPC-A-610GA using visual, automated optical (AOI) or manual X-ray or automated X-ray inspection (AXI) equipment as available. See J-STD-001 for guidance on the use of magnification during visual inspection. Use of assemblies (test printed board and the DUTs) for BLR testing is acceptable only if compliance with the criteria per IPC J-STD-001GA/IPC-A-610GA has been achieved. Assembled printed boards for which criteria per IPC J-STD-001GA/IPC-A-610GA are not met should be scrapped. Rework of post-reflow solder joints not meeting these requirements is not permissible.

For panels intended for electrical testing, a manual verification of test loop integrity using a suitable electrical tester is recommended before starting BLR testing.

6.9. Singulation

If singulation of individual or groups of daughterboards from a panel is required, provisions have to be taken to limit any negative impact on assembly integrity. In particular, strains (in effect bending) during singulation may result in printed board failures such as pad cratering, trace cracks etc. The use of automated routers to properly singulate pre-designed panels is preferred, but other methods based on best industry practices (e.g., punch singulation) are also acceptable. ‘Snap-to-break’ approaches are not acceptable, as strains at the panel level cannot be controlled during such brute-force methods.

Care should be taken in the cleaning process to limit contamination from dust and other foreign-object debris resulting from the singulation operation. Contamination can cause shorts or leakage paths impacting electrical testing. Inspection, including visual, is strongly recommended after singulation.

6.10. Documentation and Traceability Requirements

A SMT spreadsheet (AEC-Q007-002 – Tab SMT) establishes the minimum documentation for important characteristics of the SMT assembly process to be shared.

Full traceability regarding materials, process parameters and equipment is mandatory, but sharing of this information is not required.

7. RECOMMENDED CONTENT IN A BLR REPORT

Typically, the following content should be found in a final report.

- Device under test details (see Section 4)
- Sample size and test conditions
- Failure definition and monitoring scheme (see Appendix 3)
- Results including statistical analysis (see Appendix 5)
- Description of generic data if used
- Items from the test method attachments (e.g., AEC-Q007-001)
- Electrical and physical analysis (see Appendix 4)
- Component production equivalence (see Section 2.4.2)
- AEC-Q007-002 spreadsheets
    - Printed board spreadsheet and printed board schematic (see Section 5)
    - SMT spreadsheet and assembly details (see Section 6)

Appendix 1: Definition of a BLR Product Family

For devices to be categorized in a BLR Product Family, they should belong to the same package family and should have the same package design, materials, assembly process and assembly site. Some elements can differ due to the need to utilize a special “die” element but if so, any differences should be reported to the user. The below list can be used as a guideline for identifying differences.

- Package Type (e.g., DIP, SOIC, PLCC, QFP, PBGA, etc.)
  - Basic design and materials used in the construction are the same
  - Die size/aspect ratio can vary but ideally the worst-case size is used for a test vehicle
  - Lead or ball pitch is the same
  - Ball pattern layout/symmetry is equivalent

- Package Design, Materials and Assembly Process – the following attributes must be the same:
  - Die thickness
  - Die (X-Y) ratio (length vs width)
  - Leadframe base material and thickness
  - Leadframe plating process & material (internal & external to the package)
  - Die attach material
  - Wire bond material & diameter
  - Wire bond method, presence of downbonds, & process
  - Flip-chip bump or pillar materials
  - Lid attach material (e.g., epoxy)
  - Die to lid attach material (e.g., thermal interface material)
  - Plastic mold compound material, organic substrate material, or ceramic package material
  - Underfill epoxy
  - Redistribution layer count and material set
  - Solder Ball metallization system, both solder ball alloy and solder ball pad
  - Solder ball pad style (NSMD or SMD)
  - Heatsink type, material, & dimensions
  - Laminate or ceramic substrate thickness
  - Laminate or ceramic exterior surface plating process and material
  - Laminate substrate Cu thickness by layer
  - Laminate substrate Cu layer count
  - Laminate substrate Cu area coverage

- Package Assembly Site
  - Uses the same assembly site as for production material (any differences to be identified and recorded)

- SMT Assembly Site
  - The SMT assembly processes should follow typical production SMT assembly processes (any differences to be identified and recorded)

Appendix 2: Board-Level Reliability Change Matrix Guidelines

The AEC BLR change matrix allows for numerical simulation for many possible changes. However, the numerical simulation model (digital twin) needs to be based on relevant experimental data. IPC-9301 provides an excellent assist for understanding the potential complexity of numerical simulation.

Table A2: Change Matrix

Component Changes Needing Consideration for a Recharacterization Experiment and/or Numerical Simulation		Substrate Based Components: ex: BGA, LGA, laminate CSP	Leaded Components: ex: QFP, SOIC, TSSOP	Leadless Components: ex: QFN, FC-QFN, DFN, SON	Wafer Level Package Fan-Out: ex: RCP, EWLB	Wafer-Level Package Fan-In: ex: WL-CSP	Multi-Chip Modules with Exterior Surface Solder-Joints
Mechanical Factors	Die Dimensions (x-y)	N	N	N	N	N	
	Die Thickness (z)	N	N	N	N	N	
	Die Location to Package Center	N	N	N	N		
	Die attach thickness	N	N	N			
	Die stacking	N	N	N			
	Spacers and adhesives between stacked die	N	N	N			
	Multiple die on a single substrate plane	N	N	N	N		
	Die attach material property	N	N	N			
	Flip-Chip underfill epoxy material properties	•					
	Molded underfill material properties	N	N	N			
Flip-Chip Bump	Bump tech, e.g. C4 => Cu pillar	•	•	•			
	Bump dimensions (both diameter and height)	N	N	N			
	Bump pitch (including staggered)	N	N	N			
	Bump count	N	N	N			
Package Information	Package Body size (x-y)	N	N	N	N	N	N
	Package Body thickness (z)	N	N	N	N	N	N
	Substrate thickness, layer count, layer thickness, etc.,	N					N
	Substrate material property	N					N
	Substrate supplier	•					•
	Redistribution layer material property				•	•	
	Leadframe thickness		N	N			
	Leadframe material property		N	N			
	Leadframe supplier		•	•			

See Notes and Comments below.

Table A2: Change Matrix Guidelines (Continued)

Component Changes Needing Consideration for a Recharacterization Experiment and/or Numerical Simulation		Substrate Based Components: ex: BGA, LGA, laminate CSP	Leaded Components: ex: QFP, SOIC, TSSOP	Leadless Components: ex: QFN, FC-QFN, DFN, SON	Wafer Level Package Fan-Out: ex: RCP, EWLB	Wafer-Level Package Fan-In: ex: WL-CSP	Multi-Chip Modules with Exterior Surface Solder-Joints
Solder Ball and Package Pad Information	Solder ball diameter (nominal) before ball attach	N			N	N	N
	Wetted solder package pad diameter, if applicable	N			N	N	N
	Surface finish of package side before ball or solder attach	•			•	•	•
	Package pad pitch	•			•	•	•
	Package land pattern type, SMD or NSMD, if applicable	•			•	•	•
	Solder ball or solder alloy	•			•	•	•
	Solder ball or solder paste supplier	•			•	•	•
	Package Pad count	N			N	N	N
	Pad array layouts (square vs rectangular), if applicable	N			N	N	N
Leadframe Information	Leadframe composition and base metal		N	N			
	Leadframe foot size for soldering wetting		N	N			
	Leadframe lead pitch		N	N			
	Leadfame lead stand-off height		N				
	Leadframe lead count		N	N			
	Surface finish of leadframe to the solder		•	•			
	Leadframe lead style (regular or pullback)			•			
Mold Comp.	Mold encapsulant style, Punched or Sawn final package	N		N	N		
	Mold encapsulant material property (including dopants, impurities)	N	N	N	N	N	
	Mold compound thickness above Si	N	N	N	N		
Stiffener	Stiffener and/or heat spreader dimensions if applicable	•	•	•			•
	Stiffener, heat spreader supplier / material property	•	•	•			•
Redistribution Information	Number of redistribution layers				N	N	
	Thickness of each redistribution layer				N	N	
	Material properties of the RDLs				N	N	
	Under bump metalluragy (UBM)				•	•	
	Via interconnect technology				•	•	
Assy	Component/MCM assembly site transfer or addition	•	•	•	•	•	•

See Notes and Comments below.

Table A2: Change Matrix Guidelines (Continued)

Notes and Comments
Two or more changes are possible to include in a single recharacterization consideration. In those cases, a change that recommends an experiment takes precedence.
•, a factor that may need a recharacterization BLR experiment and where numerical simulation is not recommended.
"N", a factor that may need a recharacterization BLR experiment and where numerical simulation is a possible alternative method.
Changes NOT of value are those that remain within the original process window. For instance changing the die size by a change in the saw blade size is not immediately valuable.
Changes of value are those that change the nominal outside the existing tolerance range.
PCN, product change notification, is not covered by this AEC document.
Substrate (carrier) includes but is not limited to: laminate, ceramic, flex, daughter card.
For BGA packages, package changes less than 1/2 the ball pitch are not a change to consider.

Appendix 3: Test Failure Definition and Daisy Chain Level

Table A3: Test Failure Definition for All DUT Levels

Typical measurements when using event detector type of measuring equipment			Test Vehicle Daisy Chain Level											
			Substrate				Leadframe				Wafer Level			
	Measurement type	Measurement type details	Level 3	Level 2	Level 1	Level 0	Level 3	Level 2	Level 1	Level 0	Level 3	Level 2	Level 1	Level 0
Electrical Monitoring Type	Continuous glitch event monitoring	1 microsecond for shortest electrical discontinuity detection preferred (2). 1 minute or shorter spacing between polls per channel.	A	A	A	C	n/a	A	A	C	n/a	A	A	C
Electrical Failure Definition	Absolute Threshold	common values are ≥300 (Ω) and ≥1000 (Ω).	A	B	B	C	n/a	A	B	C	n/a	A	B	C
	Event Repeatability	10 events (failures) must occur within 10% of the present cycle count or within a maximum of 100 cycles, whichever is smaller.	A	A	A	C	n/a	A	A	C	n/a	A	A	C

Typical measurments when using datalogger type of measuring equipment			Test Vehicle Daisy Chain Level											
			Substrate				Leadframe				Wafer Level			
	Measurement type	Measurement type details	Level 3	Level 2	Level 1	Level 0	Level 3	Level 2	Level 1	Level 0	Level 3	Level 2	Level 1	Level 0
Electrical Monitoring Type	Continuous electrical resistance monitoring	1 millisecond for shortest electrical discontinuity detection preferred. 1 minute or shorter spacing between polls per channel.	A	A	A	C	n/a	A	A	C	n/a	A	A	C
Electrical Failure Definition	Absolute Threshold	Variable resistance settings (1) by analysis software/hardware.	A	B	B	C	n/a	A	B	C	n/a	A	B	C
	% Change Threshold	a.) Constant value above hot temperature reference, e.g. 20% rise in resistance (Ω) (3). OR b.) Reference value follows temperature cycling natural variation, e.g. 20% rise in resistance (Ω) (3).	A	B	B	C	n/a	A	B	C	n/a	A	B	C
	Event Repeatability	10 events (failures) must occur within 10% of the present cycle count or within a maximum of 100 cycles, whichever is smaller.	A	A	A	C	n/a	A	A	C	n/a	A	A	C

Notes:

A. Use column “Measurement type details”.
B. Increased channel resistance may lead to a change in Threshold choice.
C. Experimenter to choose electrical verification conditions and threshold values based on equipment and test vehicle.
1. Resistance is used for convenience in the table. Using current or voltage are possible alternatives and other concepts may be developed.
2. The 1 microsecond for glitch time width source is per IPC-SM-785 and IPC-9701.
3. The 20% rise value source is per IPC-9701.

Appendix 4: Electrical and Physical Analysis of Assembly and Components

This section describes the recommended electrical and physical analysis (EPA) methods, tools and information to be obtained from the analysis of the board level reliability (BLR) DUTs (Table A4). The analysis changes whether an experiment is before, during or after stressing. These actual groupings can be found in the appropriate AEC-Q007 test method attachment.

The analysis should start with non-destructive and move to destructive techniques. Depending on the specific BLR test configuration, the preferred destructive analysis method may be cross-section or dye-and-pry.

Reference Figures A4.1 – A4.3 are intended to provide a uniform naming convention for solder-joint failures. These names when appropriate can be used for other interconnects, e.g., wirebonds. (PKG = package, PB = printed board.)

Analysis results should be included in the final BLR test report submitted to the user.

A4.1 Electrical and Physical Analysis Methods

Table A4: Electrical and Physical Analysis Techniques

EPA #	Physical and/or Electrical Analysis Method	Recommended Tools	Possible Information Obtained	Reference/s
EPA-1	Exterior Surface Microscopy and Imaging	Optical microscopy (≥30x)	Solder ball collapse Stand-off height Flux residue Package tilt/warpage	IPC-A-610 and IPC J-STD-001 with automotive addenda
EPA-2	Flatness-Tilt-Warpage Measurement	Confocal microscopy Shadow Moiré Acoustic microscopy	Package tilt Package warpage Package flatness	JESD22-B112
EPA-3	Assessment of PB Assembly Quality	Optical microscopy	Assessment of PB assembly workmanship quality, assessed against the IPC-A-610 Class 3 (See Note 1) requirements	IPC-A-610 and IPC J-STD-001 with automotive addenda
EPA-4	Solder-Joint Visual Inspection after Reflow Process	BGA inspection tool: endoscope Optical microscopy	Solder joint cracking Head-in pillow Non-wets Pad-cratering Pad Lift Flux residue	IPC-7095
EPA-5	X-Ray Inspection of Solder-Joints	2D X-ray imaging	Solder voiding Missing solder-joints Misalignment Open solder-joints	

Table A4: Electrical and Physical Analysis Techniques (continued)

EPA #	Physical and/or Electrical Analysis Method	Recommended Tools	Possible Information Obtained	Reference/s
EPA-6	Advanced X-ray Analysis	Tomographic scans	3-D reconstruction of area of interest, open solder-joints (e.g., head in pillow)	
EPA-7	Acoustic Inspection for Delamination	Acoustic microscopy	Mold compound to die and substrate/leadframe Flip-chip bump to epoxy underfill	1.) IPC/JEDEC J-STD-035 2.) MIL-STD-883 Test Method 2030 3.) SAE AS6171/6
EPA-8	Electrical Measurement of Component Daisy Chain after Reflow Process	Digital multi-meter Electrical probe-test Bench testing In-situ monitoring	Presence of open or discontinuous daisy-chain circuit. Comparison to modeled circuit resistance. Electrical characteristic change in daisy-chain circuit. Validate counts of failed assemblies. Confirm sub-net survivability.	It is recommended to take measurements at two or three temperatures.
EPA-9	Dye and Pry Penetrant Testing (also known as Dye-and-Pry)	Dye and Pry methodology Optical microscopy	Determine the number of open and partially cracked solder joints based on dye intrusion, reference info for crack growth	MIL-STD-1580 and IPC-A-610 for guidance on inspection and microscopy IPC-7095(D) section 7.3.8.2, IPC-TM-650 2.4.53 *IPC-9701 calls out IPC-9241*
EPA-10	Mechanical Cross-Sectional Analysis	Visual inspection - Optical microscopy Ion milling for cleaning up the polishing debris	Metallurgical structures Solder cracking, etc.	

Table A4: Electrical and Physical Analysis Techniques (continued)

EPA #	Physical and/or Electrical Analysis Method	Recommended Tools	Possible Information Obtained	Reference/s
EPA-11	Advanced Cross-Section and Metallographic Analysis	Electron microscopy - SEM	Information on crack initiation/growth and other failure modes. Characterization of solder joint, solder joint collapse/cracks. Solder-bulk failures. Internal package interconnect, height/diameter, solder-joint structure. Interfacial Failures (Package or PB side) Stoichiometry IMC layer differentiation and layer growth.	MIL-STD-750/MIL-STD-883 Method 2018
		EDS or EDX		
		FIB/SEM		
		XPS		
		EPMA - electron probe microanalysis for chemical determination.		

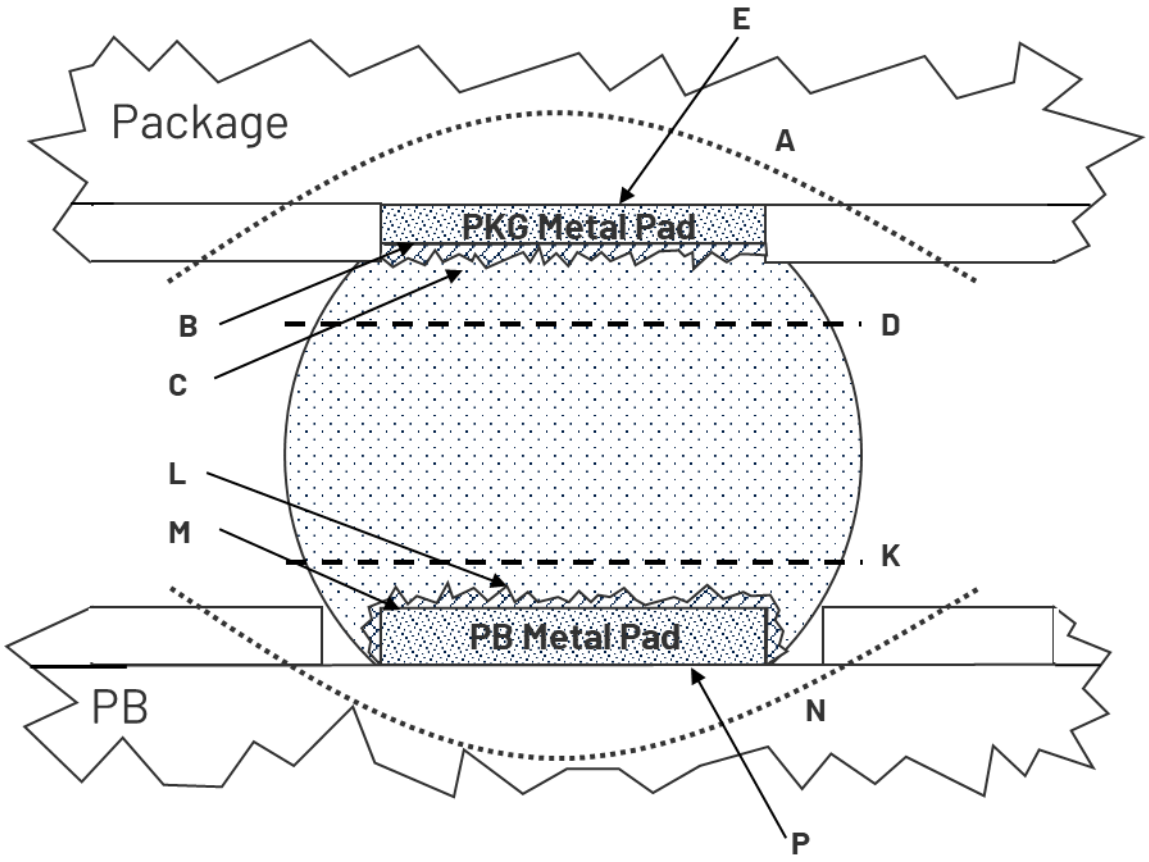
Note 1: A different assembly workmanship requirement may be agreed to between the supplier and user.

Note 2: No physical analysis result interpretation provides complete information. Thus, caution should be exercised in interpreting crack-initiation and crack growth.

Note 3: Dye and Pry can be used to determine % cracked solder horizontal cross-section area. Interpreting the extent of crack growth as an indication of goodness is beyond the scope here.

Note 4: The listed references are starting points for more information. Electrical and physical analysis technology does improve with time.

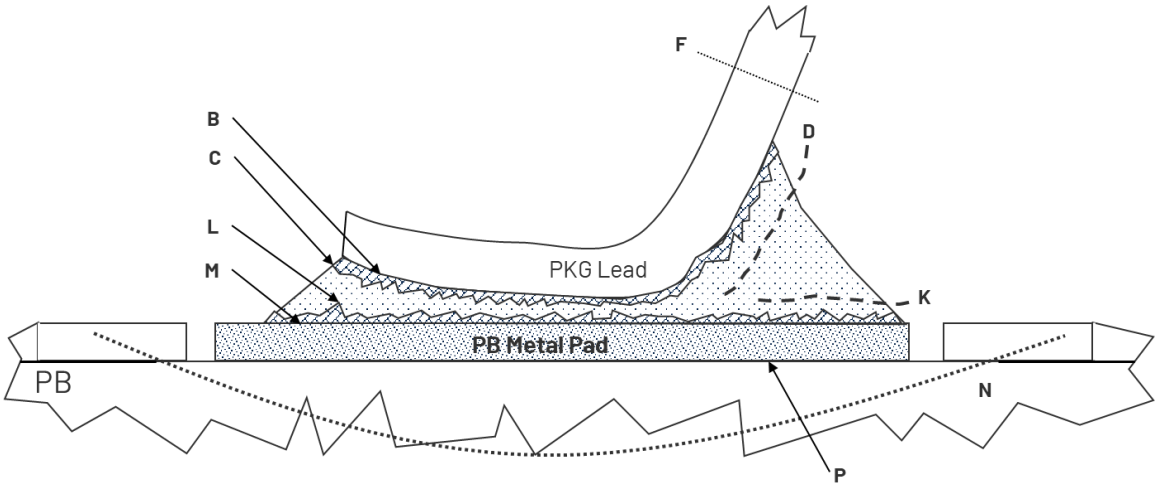
A4.2 Common Ball Grid Array Solder-Joint Failure and Defect Locations



A: PKG Pad cratering	K: PB side solder fracture
B: PKG metal to IMC fracture	L: PB IMC to solder fracture
C: PKG IMC to solder fracture	M: PB metal to IMC fracture
D: PKG side solder fracture	N: PB pad cratering
E: PKG pad to laminate separation	P: PB pad to dielectric separation

Figure A4.1: Solder-Joint Failure Locations for a BGA
(Note that a flip-chip bump will have similar failure locations.)

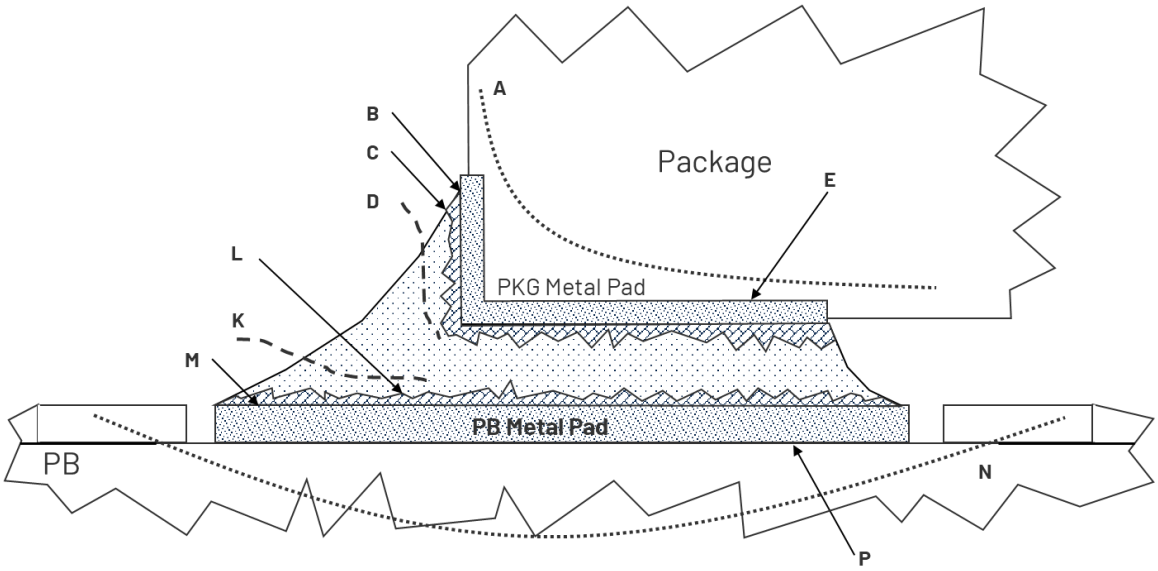
A4.3 Common Leaded Package Solder-Joint Failure and Defect Locations



B: PKG metal to IMC fracture
C: PKG IMC to solder fracture
D: PKG side solder fracture
F: Lead/connection break
K: PB side solder fracture
L: PB IMC to solder fracture
M: PB metal to IMC fracture
N: PB pad cratering
P: PB pad to dielectric separation

Figure A4.2: Leadframe Solder-Joint Failure Locations
Exposed pads for a leadframe device may have similar failure locations.

A4.4 Common Solder-Joint Failure and Defect Locations for Leadless Packages



A: PKG Pad cratering	K: PB side solder fracture
B: PKG metal to IMC fracture	L: PB IMC to solder fracture
C: PKG IMC to solder fracture	M: PB metal to IMC fracture
D: PKG side solder fracture	N: PB pad cratering
E: PKG pad lift	P: PB pad to dielectric separation

Figure A4.3: Solder-Joint Failure Locations for a Leadless Package
Failure locations for exposed pads will be similar.

Appendix 5: Weibull Statistical Analysis

A5.1 End of Life Testing and Statistical Interpretation

The AEC BLR test methods reaching end-of-life (tested to failure) should have a statistical analysis. The analysis provides results allowing users to make decisions and interpolations to unique user conditions.

A variety of statistical distributions and formula derivations can be found in BLR testing literature including log-normal and Weibull (e.g., JEP122). Weibull distributions in particular are very common for temperature cycling BLR data. How to interpret a Weibull plot will be discussed and guidance is provided for how to document BLR test results.

Other distributions are allowed and may be necessary to properly describe test results.

A wide variety of specific and generalized software programs exist for statistical analysis. A data set analyzed by several software programs may have different results. It is beyond the scope of an AEC document to list the software programs and to display the variations in graphical and numerical output.

A5.2 Weibull Distribution Fit: Slope and Characteristic Life

Regression analysis can be performed with the failures recorded during testing. This process will estimate the relationship between, e.g., the failure cycles (counter) and the Weibull probability distribution. When plotting the failure counts on a Weibull plot, the scale of the axes on this plot will show the data points to be linear (or near linear) if they follow the Weibull distribution. Shape (slope) and the scale parameter (characteristic life, moment at which 63.2% of the fails have accumulated), are the relevant characteristics of a Weibull distribution. They can be estimated using various fit protocols, e.g., maximum likelihood.

Weibull fits are defined by the slope and characteristic life for the typical 2-parameter fits with the addition of the threshold value for 3-parameter fits. Differing sources in literature and software utilize varying symbols for each parameter.

Slope provides important information about the distribution's width. As slope increases, becomes steeper, the distribution becomes narrower. In effect with increased slope the failures are more tightly distributed. In the two graphs below, the relationship between the probability density function, Figure A5.1A, and the corresponding Weibull plot, Figure A5.1B are displayed.

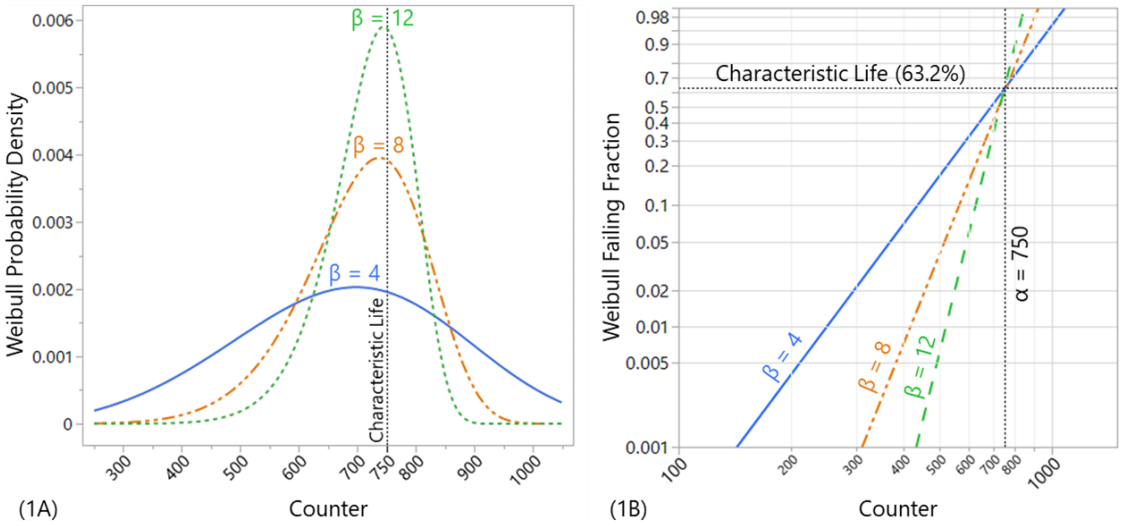


FIGURE A5.1: Weibull distributions with slopes (β) of 4, 8 and 12. The graph on the left (A5.1A) is the probability density function with the accompanied Weibull plots to the right (A5.1B). Data was generated using varied slope and a fixed characteristic value (α) of 750 (a.u.). Counter could be cycles, drops, etc.

It is clear to see in Figures A5.1A and A5.1B how the distribution is wider for shallower slopes. The characteristic life, 63.2% value, does not change with the slope. Visually (and mathematically), the mean value, 50%, does change in Figure A5.1A (each distributions peak value). As the slope increases, the mean visually approaches the characteristic life value.

A5.3 Example Weibull Distribution Plots

Figure A5.2 provides an example with 50 data points including 8 DUTs with no failures by experiments end. The surviving DUTs should be used in statistical analysis as censored data. Statistical analysis software should include the ability to work with censored data.

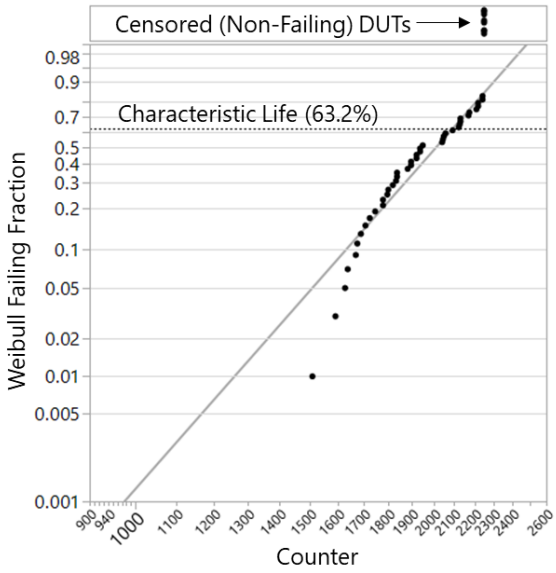


Figure A5.2: Provided is an example Weibull plot with 50 data points including 8 DUTs not yet failed at experiments end.

The axes are important with the X-axis being a counter: cycles, drops, etc. The Y-axis is the percentage of failed DUTs (aka cumulative distribution function).

Real data as shown in Figure A5.2 will have irregularly distributed failures. The resulting plot will have disconnects (large intervals in counts between failures), clustering (small intervals in counts between failures) and the like.

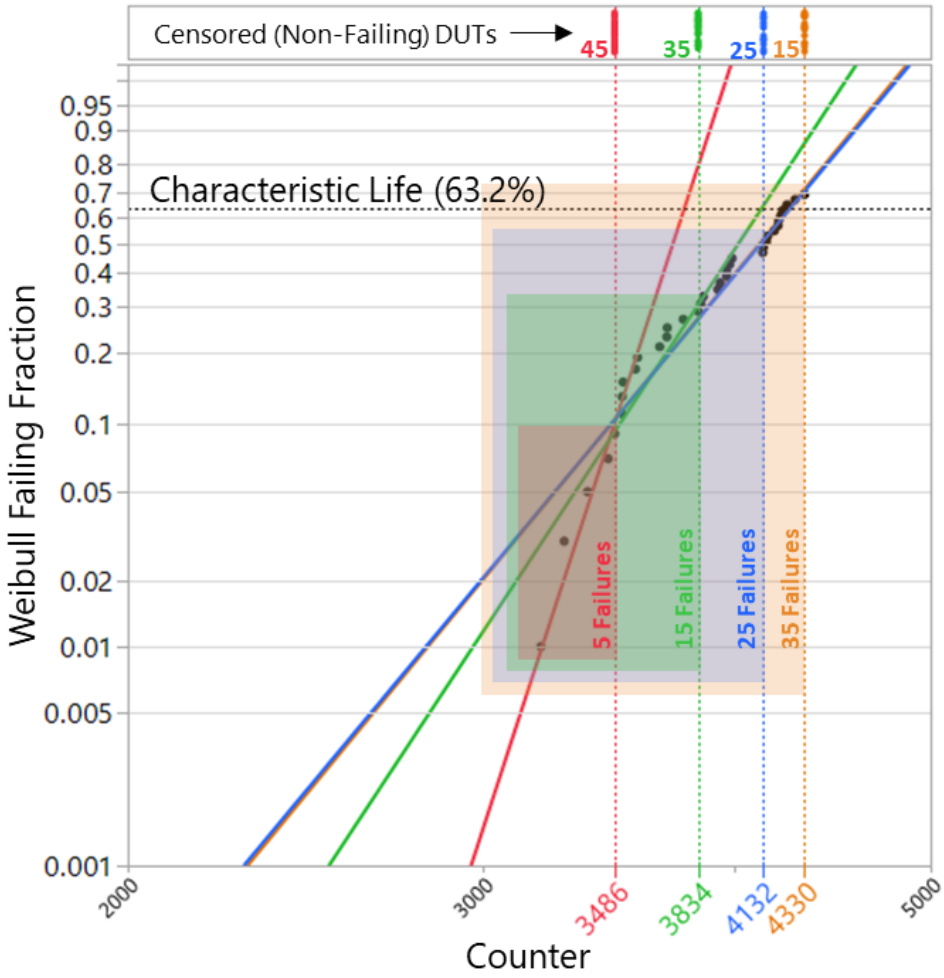


Figure A5.3: This example Weibull plot illustrates how the distribution fit (slope and characteristic life parameters) can change depending on the number of failures recorded. Each line represents the fit if testing was stopped after 5 (red), 15 (green), 25 (blue) and 35 (orange) failures of 50 DUTs.

The quality of the fit is dependent on the number of failures recorded during the stressing of the DUTs. The experiment represented in Figure A5.3 had 50 DUTs. Four subsets of the data were developed, with the assumption that the test was ended after 5, 15, 25, and 35 failures were recorded and the remaining DUTs were censored as passing at the counter of the last failure. As the failures increase, the fit parameters change; after 15 failures there is not a significant change in this test case. A general rule-of-thumb is below 10 failures the slope may be difficult to estimate and below 5 failures estimates are often inaccurate.

Engineering Statistics Handbook: 8.3.1.2. Lognormal or Weibull tests:
https://www.itl.nist.gov/div898/handbook/apr/section3/apr312.htm

The example in Figure A5.3 illustrates the need to have an adequate number of failing DUTs to determine the life distribution fit parameters. If the failure count is low, the calculated slope and characteristic life will give an inaccurate estimation of the characteristics of the DUTs. If the termination cycle is reached without reaching a sufficient number of failures, the parameters should not be calculated, instead the cycle at which any DUTs did fail should be reported.

A5.4 Two Failure Modes and Weibull Plots

Two or more failure modes or failure mechanisms during a BLR experiment are possible. A simple example is in drop test where you can have both printed board pad cratering (rip-out) and solder-joint failures.

Each failure mode will typically have its own life distribution model. In Figure A5.4A, the two failure modes are combined which results in a change of the Weibull parameters describing the overall life distribution. Figure A5.4B separates the two distributions with differing slopes, each representing a unique failure mode. A low slope, approximately 4, for a failure mode group of 10 failures and a high slope, approximately 11, for a failure mode group of 40 failures.

When comparing multiple datasets, a fixed probability value (e.g., 0.1% or Characteristic Life (63.2%)) is recommended if the population life distribution is used. These statistical values are outputs of the life distribution regression. If using attributes such as first failure, there is an inherent risk as this uses a single sample within the population.

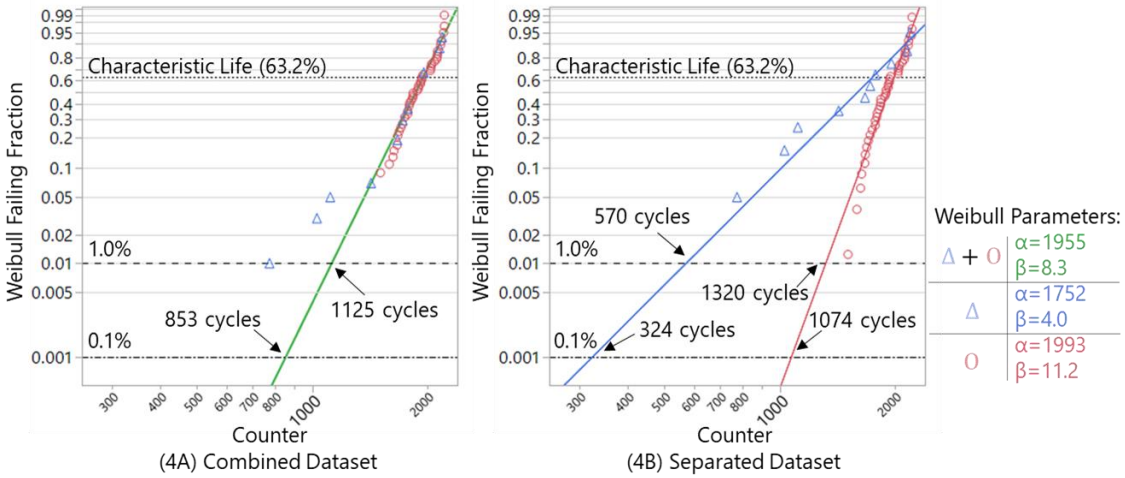


Figure A5.4: A dataset containing two failure modes are represented in the above Weibull plots. In A5.4A, the two modes are combined. While in A5.4B, the two modes are separated. With this dataset, the characteristic life does not drastically change between the two methods. However, the slope is significantly different as there is a large change between the two failure modes which are blended when the fit is calculated from the full dataset.

A5.5 3-Parameter Weibull Distributions

Two parameters, the characteristic life and slope, are typically used to describe the Weibull fit of the sample population. On occasions where the plotted distribution shows a curvature in the fit, the use of a 3-parameter, or threshold, fit may be considered. The third parameter defines a “failure free” zone of counts. In that zone, there would be no expectation of a failure. The dataset shown in Figure A5.2 has this described curvature. Figure A5.5 illustrates the fits for both the 2- and 3-parameter Weibull distribution. The 2-parameter plot shows the failures at low counts separating from the 2-parameter fit line. In contrast the data points follow the 3-parameter fit very well.

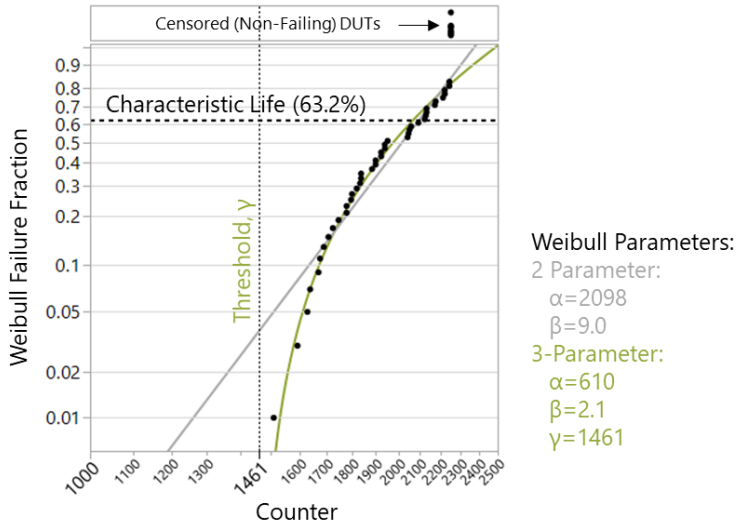


Figure A5.5: Plotted are both the 2- and 3-parameter Weibull fits of the data introduced in Figure A5.2. The data points follow the 2-parameter fit well above ~1700 cycles, but curve away below 1700 cycles. The 3-parameter, threshold, Weibull fit follows the data points well.

Note: For a 3-parameter plot, the calculated characteristic life is with respect to the threshold value. To compare a characteristic life between a 2-parameter and a 3-parameter fit, the 3-parameter values need to be added. In effect, the equivalent 3-parameter characteristic life is 1461 (failure free count, γ) + 610 (3-P characteristic life, α) = 2072. That 2072 counts can be compared to the 2-P value of 2098 counts. These two counts will generally be different.

A5.6 Weibull Plot Result Report

- A failure distribution plot (e.g., a Weibull plot), the fit values by the distribution type (e.g., Weibull: slope and characteristic life), the first failure value, number of failed DUTs, and total sample size.

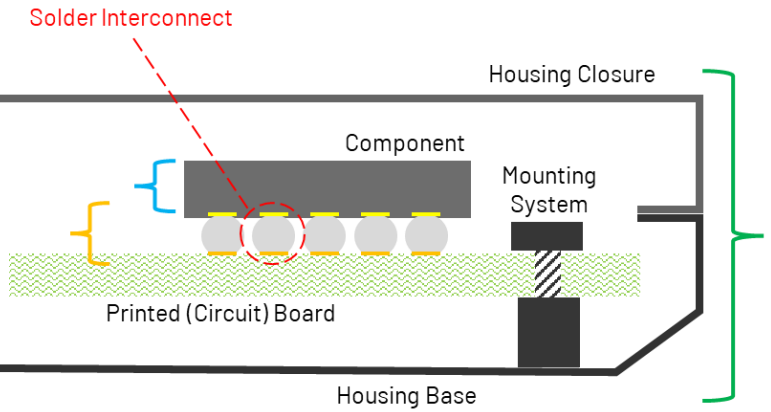
OR

- The actual failure data as a text file for the user to plot.

Appendix 6: Illustration of Reliability Testing Responsibility for Suppliers and Users

Component Level (1st Level Reliability)
Component Supplier (Tier 2)
Electrical function stability
PackageiIntegrity stability
Industry standards available for tests

Final Assembly Reliability
User (Tier 1)
Module electrical function stability
Module board-level reliability
Module housing reliability
User internal rules
End customer rules (OEM)



Board-Level Reliability (2nd Level Reliability)
Isolated Mounted DUT –
Component Supplier (Tier 2)
Solder interconnect lifetime and reliability
Cycling, drop/shock, bend, vibration, ...
Industry standards available for some tests
Module - User (Tier 1)
Cycling, drop/shock, bend, vibration, ...
User internal rules

Isolated Mounted DUT: Example, a daisy chain on a standardized PB
Module: Example, a final assembly intended for sale to an automotive OEM

Figure A6.1: A visual interpretation of who assesses the different reliability levels.

REVISION HISTORY

Rev #	Date of change	Brief summary listing affected sections
-	Mar. 12, 2024	Initial Release.