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Automotive Electronics Council
Component Technical Committee

BOARD-LEVEL RELIABILITY TEMPERATURE CYCLING TEST METHOD

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Component Technical Committee

BOARD-LEVEL RELIABILITY TEMPERATURE CYCLING TEST METHOD

Unless otherwise stated herein, the date of implementation of this standard for new qualifications and re-qualifications is as of the publish date above.

1. SCOPE

This document is an attachment to AEC-Q007 and contains a test method for experimental stress testing of solder joints and other interconnects. Solder joints are the package exterior soldered connections between an electronic component and a printed board. Other interconnects include wirebonds, substrate vias, flip-chip bumps, etc. The test method objective is to stimulate and precipitate failures in an accelerated manner compared to use conditions. This test method should not be used indiscriminately. Each experimental program should be examined for:

a. Any potential new and unique failure mechanisms.
b. Any situation where these test/conditions may induce failures that would not be seen in the application.
c. Any test condition that could result in an acceleration outside the boundaries of the acceleration model (e.g., exceeding material glass transition temperatures).

Passive electronic elements are not discussed in detail. The test method may be used for passive components.

Multi-chip modules (MCMs) may use the described test method as an alternative to IPC-9701.

The test method is for board-level reliability characterization and is not a pass/fail indicator for any application nor any industry nor user mission profile.

Use of this attachment does not relieve the IC supplier of their responsibility to meet their own company's board-level reliability program. In this attachment, "user" is defined as all customers using a device tested per this test methodology. The user is responsible to confirm and validate all test data that substantiates conformance to this test method.

1.1. Purpose

The purpose of this test method is to experimentally gather surface mounted component board-level reliability thermal fatigue life distribution data.

Ideally, each experiment would run to failure. Only with known failures can extrapolations to other conditions be made. Only with known failures can failure distribution analysis be conducted. (Failure distribution analysis guidelines can be found in AEC-Q007 Appendix 5.)

1.2. Reference Documents

Current revision of the referenced documents will be in effect at the date of agreement to the test plan. Subsequent qualification plans will follow updated revisions of these referenced documents.

1.2.1. Automotive

AEC-Q007	Failure Mechanism Based Testing Guidelines for Components Mounted to a Printed Board

1.2.2. Industrial

IEC 60068-3-5	Supporting documentation and guidance - Confirmation of the performance of temperature chambers
IPC-9701	Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments
IPC-9702	Monotonic Bend Characterization of Board-Level Interconnects
JESD22-A104	Temperature Cycling
JEP153	Characterization and Monitoring of Thermal Stress Test Oven Temperatures

1.3. Definitions

1.3.1. General Definitions

Definitions used within this attachment are in Section 1.3.4. In addition, other definitions may be found within the referenced board-level reliability (BLR) base document, AEC-Q007.

1.3.2. AEC-Q007 BLR Test Conformance

Performance of the testing in accordance with the test methodology as outlined in the base BLR document and in this BLR attachment allows the supplier to claim that the part has successfully completed the specified testing per AEC-Q007 and AEC-Q007-001.

1.3.3. Operating Temperature Grade and BLR Temperature Cycling Condition

The different Q10x and Q200 documents have stress temperature ranges applicable to different application conditions. These can provide a basis for choosing the temperature cycling conditions (see Table 1).

1.3.4. Definitions of Common Terms

Note 1: Use of Shall, Should, Must and May
Shall: A keyword indicating a mandatory requirement
Should: A keyword indicating flexibility of choice with a strongly preferred alternative
Must: The same as shall
May: A keyword that indicates flexibility of choice with no implied preference
Note 2: A reference to a definition (e.g., IPC-9701) may indicate the complete usage from the source or a modified usage from the source.
Note 3: Additional definitions of common terms can be found in the AEC BLR Base document, AEC-Q007.

% Change Failure Threshold: A change in electrical resistance that is a percent change above the baseline and DUT values. Other electrical measurements can be used in place of resistance.

Absolute Failure Threshold: A change in electrical resistance that does not consider the baseline nor DUT values. Other electrical measurements can be used in place of resistance.

Baseline Resistance: The resistance for the DUT measurement loop except the DUT. This would include the printed board, cabling, instrumentation, etc.

Board-Level Reliability (BLR): The reliability of solder joints and other interconnects of electronic components attached to printed (circuit) boards.

Catastrophic Failure: A worst-case event where a change in state from good to bad (failed) is permanent.

Chamber Temperature: The measured temperature for the chamber air environment away from samples and other hardware.

Cold and Hot Dwell Temperature: The temperature that is above Nominal Tmax for the hot dwell and is below Nominal Tmin for the cold dwell. The dwell temperature may be the average during a dwell. Sometimes called the soak temperature. (Based on IPC-9701)

Cold and Hot Dwell Time: The total time the sample temperature (not the chamber temperature) is within the specified range of (Tmax + tolerances) and (Tmin + tolerances). (Based on IPC-9701)

Cyclic Temperature Range/Swing: The difference between maximum and minimum dwell temperatures incurred during operational use or temperature cycling tests. (IPC-9701)

Daisy-Chain: An electrically conductive link that can be connected in series with other conductive links (like a chain of daisies) to form a continuous electrical circuit or "net". A single link is a conductive path inside the DUT from one solder joint to another solder joint. A loop is multiple single links where each single link is typically connected by a link on a PB.

Data Logging: Repetitive readpoint data collection.

Device Under Test (DUT): The production worthy part or a specialized test vehicle (i.e., daisy-chain component, etc.) used within the testing as specified herein.

Event: The time at or cycle when a failure criteria measurement occurs.

Glitch: A short in time reading or set of readings different from the normal (expected) readings.

In-Situ Measurement: Measurement conducted during a test (i.e., in place) rather than during an interruption of a test condition. (IPC-JEDEC-9702)

Instrument measurement time width: The nominal time an instrument uses to take a measurement.

Interconnect: Conductive element used for electrical interconnection (e.g., solder ball, lead, wirebond, PB, etc.). (IPC-JEDEC-9702)

Load: The sample(s) and associated fixtures (e.g., trays, racks, etc.) in the chamber during test. (JESD22-A104)

Load Transfer Time: The time it takes to physically transfer the load from one temperature chamber and introduce it into the other. Load transfer applies to dual and triple chamber cycling. (JESD22-A104)

Maximum Load: The largest load that can be placed in the chamber and still meet the specified temperature cycling requirements as verified by thermocouples. (JESD22-A104)

Maximum Nominal Temperature: The maximum nominal temperature for a specific test condition is the required temperature of the sample. (IPC-9701)

Maximum Sample Temperature: The maximum measured temperature experienced by the sample(s). (JESD22-A104)

Minimum Nominal Temperature: The minimum nominal measured temperature for a specific test condition is the required temperature of the sample. (IPC-9701)

Minimum Sample Temperature: The minimum measured temperature experienced by the sample(s). (JESD22-A104)

Nominal delta Temperature (range): The difference between nominal Tmax and nominal Tmin for a specific test condition. (IPC-9701)

Poll: Reading a value (e.g., resistance) or state (e.g., high) from a machine including recording devices. Also, the actual occurrence for an electrical reading.

Polling Rate: Usually, the frequency at which individual polls are made (e.g., 1 Hz). The time gap between individual polls.

Printed Board (PB): Printed Board is the planar structure to which electronic components are attached to complete a functional electrical circuit. Also known as a printed circuit board (PCB) and printed wiring board (PWB). (IPC-JEDEC-9701)

Relative Failure Threshold: A change in electrical resistance that is in addition to the baseline and DUT values. Other electrical measurements can be used in place of resistance.

Reliability: The ability of a product (surface mount solder attachments) to function under given conditions and for a specified period of time without exceeding acceptable failure levels. (IPC-9701)

Sample Temperature: The measured temperature during temperature cycling for test vehicles mounted on PCBs during BLRT. The measurements are on or very near the test vehicle. (Based on JESD22-A104)

Soak: See the Dwell definitions.

Temperature Ramp Rate: The rate of temperature increase or decrease per unit of time for the sample(s). The temperature ramp rate should be measured for the linear portion of the profile curve, which is generally the range between 10% and 90% of a specific test condition temperature range. Note: Ramp rate can be load dependent and should be verified for the load being tested. (JESD22-A104)

Test Conditions: The various temperature cycle range options. (JESD22-A104)

Test Vehicle: Test vehicles for BLRT may be specially designed electrical connections (daisy chains) in standard packaging, live product, or failed live product. (See DUT.)

Thermal Cycling: Exposure of assemblies to cyclic temperature changes where the rate of temperature change is slow enough to avoid thermal shock (typically less than 20C/min). (IPC-9701)

Thermal Mass: The ability of a material to absorb and retain thermal energy (heat). For BLR, thermal mass plays a role in electronic components lagging behind the chamber temperature state.

Thermal Shock: Thermal shock occurs when an assembly is exposed to rapid changes in temperature causing transient temperature gradients, warpages, and stresses within the part and/or assembly. The rate of temperature change for thermal shock is usually greater than 20C/min. (IPC-9701)

Total Cycle Time: Time for one complete temperature cycle. (IPC-9701)

Transient: An intermittent electrical event of elevated resistance.

Working Area: The portion of a chamber, used for stress testing, which meets the calibration requirements. (JEP153)

Working Zone: The volume in the chamber(s) in which the temperature of the load is controlled within the specified conditions. (JESD22-A104 and IPC-9701)

2. GENERAL DEFINITIONS

2.1. Precedence of Documents

The precedence of documents can be found in AEC-Q007 and includes the reference documents in both AEC-Q007 and this guideline (see Section 1.2).

2.2. Definition of a Test Failure

Electrical resistance measurements are typical for BLR temperature cycling monitoring. Resistance will be used for simplicity in the descriptions below. The basic concepts would work for other measurement types.

For board-level reliability temperature cycling, the temperature swings also induce a resistance swing. That resistance swing is NOT the failure definition.

Instead, the failure definition needs to properly reference the baseline condition. And the failure definition needs to have sufficient margin to not have false failures.

Figure 1 graphically represents three possibilities for choosing a reference resistance. From the reference resistance, a resistance failure value is chosen. If a resistance reading is above the resistance failure value, then a failure is recorded.

The plotted resistance is high while at hot temperatures, drops to a lower resistance at cold temperatures and then rises again to a higher resistance during one temperature cycle. Starting at hot temperature, high resistance, is used here for demonstration purposes only.

Though not shown in Figure 1, the middle representation can also use a % change for a resistance failure threshold. That change added to the reference resistance should be higher than the expected hot temperature resistance value.

The experimenter should provide a clear description of the failure definition in a final BLR report. The AEC-Q007 base document has a description of failure definitions in Section 2.5, Table 2, and Appendix 3.

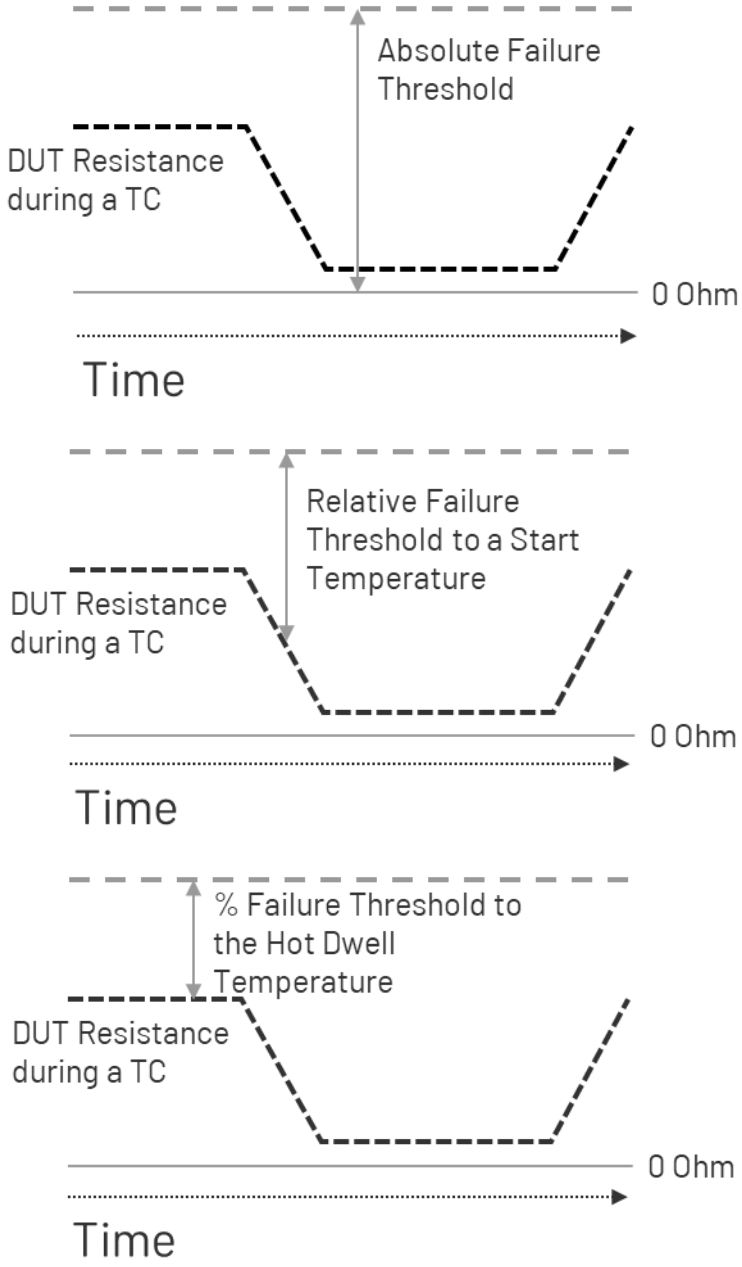

Figure 1: The top image shows an absolute resistance value for a failure definition. The middle image has the baseline reference resistance, for example, at room temperature while the entire resistance swing from Hot to Cold will be higher and lower than the baseline. The bottom image shows a reference resistance set at the Hot temperature.

2.3. Definition of In-Situ Measurement Terms

For the preferred in-situ monitoring there are some basic concepts that must be understood.

In Figure 2, the polling rate is how often a monitoring tool takes a data point. Caution is needed since there are two polling rates: the actual rate for the monitoring tool and the actual rate for a single device under test. For a monitoring tool recording data from multiple DUTs and even multiple subnets, the rate per DUT is slower than the tool rate. Both the tool and DUT-net rates should be documented.

Instrument measurement time is the actual interval of time needed by the tooling to gather a data point.

With a need to record (data logging), for example, resistance values during temperature changes, data collection rates should not be less than once a minute (IPC-9701). Data collection only at the dwell temperatures is missing the materials expansion / contraction differences during a temperature change and possible related electrical resistance failures. Intermittent resistance changes are often best detected during temperature changes.

2.4. Definition of Temperature Cycle Terms

Temperature cycling is the deliberate change in temperature for the device(s) under test (DUT) in a controlled and repeatable manner. The actual temperature cycle during a test should be the same throughout the complete BLRT.

Figure 3 provides a representation of a typical temperature cycle and terms.

An important fact is the actual temperature difference between the theoretical ideal profile, chamber air profile and DUT profile temperatures (Fig. 3). The theoretical ideal profile can, for example, be the idealized perfect profile or the temperature controller programmed profile. The chamber air profile would be that of the air surrounding the PBs with DUTs. The chamber air temperature will vary by location in the chamber.

Finally, the DUT temperature profile is the one of importance. The temperature profile at the DUT should meet the planned temperature profile. Temperature calibration of the DUT temperature and the chamber air temperature is necessary to understand variation. With that calibration data, the temperature profile at a DUT can be shown to meet the planned temperature range.

Generally, the DUT temperature will lag in time versus the chamber air temperature. Temperature calibration between the DUT temperature to the controlled planned temperature is necessary. The temperature profile at the DUT should meet the guidelines in Section 3.1 and Table 1.

Note that for many small DUTs, the dominant thermal mass will be the PB. Thus, temperature measurements on the PB instead of in/under the DUT are an alternative.

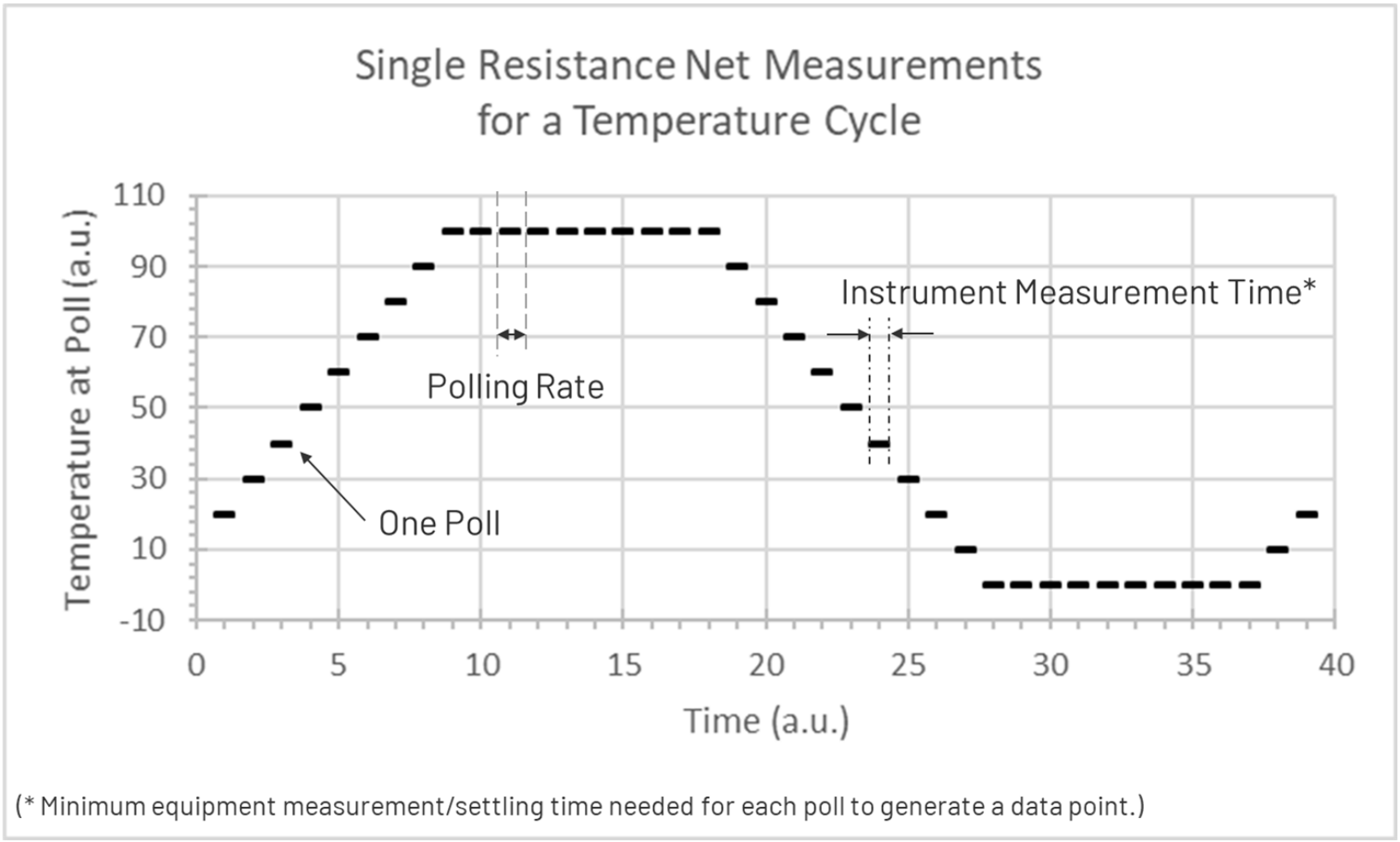

Figure 2: An example of polls, resistance measurements, during a temperature cycle for a single device or a single subnet.

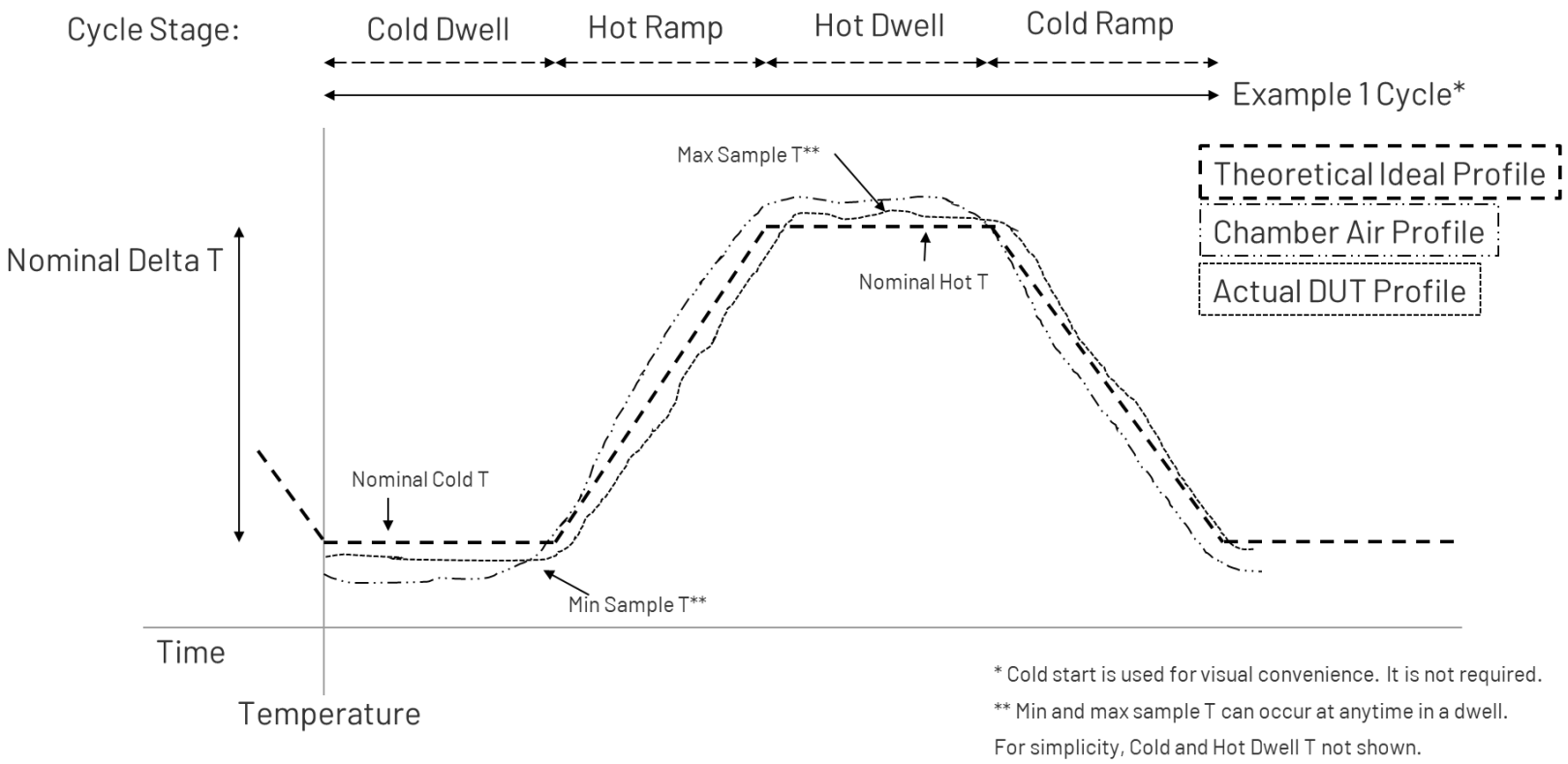

Figure 3: A temperature cycle and its terms are shown for reference.

3. BOARD-LEVEL RELIABILITY TEMPERATURE CYCLING

3.1. Board-Level Reliability Temperature Cycling Background

3.1.1. Temperature Range

The selected temperature cycling condition should meet or exceed the expected application ambient operating range. (An example set of possible operating ranges come from AEC-Q100.) BLR tests the lifetime of interconnects, not the semiconductor device reliability.

3.1.2. Dwell Time

The temperature dwell time is the method used for creating an experiment that is accelerated compared to a field application. The dwell times are short in duration compared to most applications. An experiment with short dwell times compared to application dwell times can have many more cycles of damage in a given time. The dwell time range of 10 to 15 minutes provides approximately equal damage and crack propagation [Coyle]. It is preferred that the dwell times at hot and cold extremes are equal.

3.1.3. Ramp Rate

The ramp rate uses existing industry practice documented in IPC-9701, IPC-SM-785 and JESD22-A104. From those documents, the upper limit of temperature change is the industry boundary between temperature cycling and thermal shock. Thermal shock is not the desired cycling method. Multi- (e.g., dual) chamber systems can be used if the ramp rate can be shown to meet the herein defined guidelines.

Ramp rate is measured under or near the DUT, not in the chamber air. Chamber temperature control however may use chamber air measurements. Then it is necessary to determine the difference between the DUT and chamber air temperatures.

3.1.4. Cycle Frequency

From experimental pragmatism, less than one cycle per hour (cph) is not recommended. BLR-TCC-03 (-40/85°C) at 1 cph with 10-minute dwells and 20 minute ramps provides a calculated lower boundary at a 6.25°C/min ramp rate.

3.1.5. Setting the Event Free Cycle Count for Experiment Termination

There will be situations where a supplier – user agreement needs to establish unique cycle count goals. Recommendations to establish this specific cycle count include numerical simulation both for the application and for the BLR test, reviewing existing BLR data if available, agreeing upon using the Coffin-Manson equation or something similar and also agreeing upon the constants used in the modeling and acceleration factor equations. See also Section 3.3.

3.1.6. Temperature Profile Monitoring

The temperature cycle should be confirmed by chamber temperature calibration and by in-situ chamber temperature monitoring. JEP153 documents a procedure for confirming a chambers temperature profile. Additional sources for calibration and monitoring procedures include IEC 60068-3-5, IPC-9701 and JESD22-A104. It is the chamber working zone, the chamber volume bounding the under-stress assemblies, which is critical for monitoring. In a final report both the air temperature and the temperature in an instrumented DUT are required.

Note: Putting a thermocouple (thermal sensor) in/under a small DUT can be difficult. For small DUTs the PB may be the main thermal mass and a thermocouple near the DUT can be sufficient.

Note: The temperature measurements for an instrumented DUT are not necessary during the entire experiment. Rather a measurement of at least 1 full cycle at the experiments start would be a minimum guideline.

3.1.7. User Specific Test Conditions

Any test conditions requested by the user and not specified in this document shall be negotiated between the supplier and user requesting the test condition. Unique test conditions should be documented in the final report.

3.2. Experimental Temperature Cycling Conditions

The temperature cycling condition parameters and notes listed in Table 1 and Table 2 impact test results. Careful documentation is fundamental for reporting the BLR results and that includes temperature cycling details.

Table 1: Interconnect Temperature Cycling Conditions

AEC BLR Temperature Cycling Conditions			
Test Condition	**Temperature Range *(Notes: 1, 2, 3)***	**Dwell Time *(Notes: 4, 5)***	**Ramp Rate *(Notes: 5, 6)***
BLR-TCC-0	-40/150°C	10-15 min	<20°C/min
BLR-TCC-1	-40/125°C	10-15 min	<20°C/min
BLR-TCC-2	-40/105°C	10-15 min	<20°C/min
BLR-TCC-3	-40/85°C	10-15 min	<20°C/min

Table 2: Notes for Temperature Cycling Conditions

1.	Tolerance for the DUT dwell temperatures is hot (-0/+10°C) and cold (-10/+0°C). (Preferred would be hot -0/+5°C, cold -5/+0°C) (IPC-9701)
2.	It is the responsibility of the data collector to choose the Test Condition. (See Section 3.1.1)
3.	Caution: When making extrapolations to different cycling conditions, it is recommended to confirm that material properties at different temperatures and possible failure modes are understood. An example is the mold compound glass transition temperature (Tg) being above or below the maximum cycling temperature.
4.	Range of dwell times is based on existing industry practices (Coyle). Dwell time choice may change the failure mode and event cycle count. Actual user (field) profiles typically have longer dwell times which may lead to a reduced characteristic life.
5.	The ramp rate and other factors are based on single chamber temperature cycling and not on dual chamber thermal shock (examples liquid-to-liquid and air-to-air).
6.	The ramp rate listed in the table is not a target ramp rate. It is an upper limit. A common ramp rate will be around 10°C/min. (The purpose is to not be in a thermal shock environment.) Ramp rates less than 5°C/min may prove to be impractical experimentally.

Reference: Richard Coyle, et al, “iNEMI Pb-Free Alloy Characterization Project Report: Part V – The Effect of Dwell Time on Thermal Fatigue Reliability,” Proceedings of SMTAI 2013, 470-489, Ft. Worth, TX, October 2013.

3.3. Terminating an Experiment

Since the temperature cycling test has the purpose to determine the reliability of solder joints and other interconnects for a DUT it would be desirable to run a test until the characteristic cycles-to-fail distribution is available. This is considered fulfilled as soon as 63.2% of the DUTs have failed.

There are practical limits to how long an experiment can run in chambers. A termination cycle count of 3000 cycles would be suggested as a pragmatic choice. The cycle count at termination and rationale for termination should be documented in the BLR report.

3.4. Temperature Cycling Chambers

Board-level reliability temperature cycling chambers are in general single chambers. The air temperature inside the chamber is changed to create the temperature dwells and ramps. Ramp rates are below 20 ^{o}C / minute.

Automotive electronic component suppliers use dual-temperature chamber systems for component qualifications (e.g., AEC-Q100). The dual-chamber system has unique chambers in which cold and hot temperatures are maintained. Some form of an elevator or shuttle moves the in-stress components between the chambers. The ramp rate for temperature change is quite rapid and generally exceeds the shock criteria of >= 20 ^{o}C / minute.

What matters for the experimenter is to achieve a ramp rate as specified in Table 1.

3.5. Temperature Cycling Sample Size

The sample size for an AEC board-level reliability test should be 1 lot of 50 samples. The “data points” (both failures and survivors) at the planned tests end should be 50.

Fifty samples are preferred but the supplier can achieve similar results with multiples of DUTs/PB that are near 50 in count. For example, a PB that has 8 DUTs can reach 48 total samples with 6 PBs and meet the statistical purpose.

If there are planned removals (e.g., for physical analysis) at different read points, extra samples will need to be added to the starting sample size. For example, if there are planned removals of 1 sample at 1000, 1500, 2000, 2500 and 3000 cycles, then 55 samples need to start the test (50 + 5 pulls). (These extra samples can also be used as substitutes for mishandling damage of other DUTs.)

A sample may be removed from test if failed and intended for electrical and physical analysis. That removed sample should have its count of cycles recorded for future statistical analysis.

Suppliers have extensive existing data sets using other sample sizes, e.g., the IPC-9701 sample size of 32. These data sets remain valid for generic data after the formal release of AEC Q007-001.

Availability of DUTs to users are unique supplier-user agreements.

4. ELECTRICAL AND PHYSICAL ANALYSIS

Table 3 below provides suggestions which electrical or physical analysis (EPA) methods can be of value. Before, during and after, refer to when in an experiment various EPA items are suggested. Note that dye-and-pry and mechanical cross-section are an “either or” method choice. See the AEC-Q007 BLR base document for a comprehensive list with method references.

Table 3: Suggested Electrical and Physical Analysis Methods

EPA #	Electrical and/or Physical Analysis Method	Before	During	After
EPA-1	Exterior Surface Microscopy and Imaging	•		•
EPA-2	Flatness-Tilt-Warpage Measurement	•		
EPA-3	Assessment of PB Assembly Quality	•		
EPA-4	Solder-Joint Visual Inspection after Reflow Process	•		
EPA-5	X-Ray Inspection of Solder Joints	•		•
EPA-6	Advanced X-ray Analysis	•		•
EPA-7	Acoustic Inspection for Delamination	•		•
EPA-8	Electrical Measurement of Component Daisy Chain after Reflow Process	•	•	•
EPA-9	Dye and Pry Penetrant Testing (also known as Dye-and-Pry)		•	•
EPA-10	Mechanical Cross-Sectional Analysis		•	•
EPA-11	Advanced Cross-Section and Metallographic Analysis		•	•

5. RECOMMENDED CONTENT IN A TEMPERATURE CYCLING BLR REPORT

Typically, the following content should be found in a final report.

- Experimental results
- Sample sizes (see Section 3.5)
- Experimental temperature cycling conditions (see Sections 3.1 and 3.2)
- Experiment termination details (see Sections 3.3 and 3.1.5)
- Test failure definition (see Section 2.2)
- Electrical and physical analysis (see Section 4.0)

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REVISION HISTORY

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-	Mar. 12, 2024	Initial Release.