Automotive Electronics Council

Component Technical Committee

Technical Session Abstracts

(Agenda subject to change)

2019 – Twenty-First Annual Automotive Electronics Reliability Workshop

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Novi, MI
Sheraton Detroit Novi Hotel

1.1 Snap-In High Vibration Products: AEC-Q200 Automotive for High Voltage Performance Requirements
R. Caeiro, KEMET Electronics S.A.

The Electric Vehicle (EV) Industry has emerged in recent years as a feasible alternative to internal combustion engine (ICE) vehicles aiming to reduce emissions that are linked to a major environmental concern about global warming. The on-board charger application has a new and important role in the industry with many electric vehicles with battery voltages ranging from 100V to 400V using Snap-In electrolytic capacitors as the DC-link in the charging circuit. Due to this exponential increase in the market and the advantages of aluminum electrolytic capacitors, such as high energy storage and low device impedance, the development of a new series capable of withstanding high vibration performance becomes increasingly more important. KEMET is releasing a new Snap-In product specifically designed for automotive applications with special features for vibration and high voltage reliability combining high ripple current, excellent surge voltage capability and long life, considering rated conditions applied. The new Snap-In series can withstand high vibration in accordance with the demanding requirements of the Automotive Electronics Council's AEC-Q200 qualification.

1.2 Performance Update of Multilayer Varistors Relative to TVS Diodes
D. West, AVX Corporation

TVS diodes have been used for circuit protection and Load Dump protection, in the automotive industry for decades. With the growing number of electronics in automobiles, it is worthwhile to consider alternative solutions for traditional overvoltage protection solutions that are smaller, lighter, and functional over a wider range of temperatures. Multilayer varistors (MLV) offer size reductions, temperature stability, higher energy density, and higher reliability circuit protection in standard EIA case sizes that are AEC-Q200 qualified. Size and weight reductions are intuitive by comparing a typical TVS diode SMAJ package and EIA 0805 case size, what is not always clear are the electrical and thermal characteristics inherent in the material and monolithic construction of MLVs that, gram for gram, are far superior to TVS diode technology. This paper provides an update on MLV performance as a viable TVS technology in the Automotive industry for 3 parameters: Temperature, Load Dump, and Clamping.

1.3 Use of New Magnetic Materials in High Power Applications
L. Weakley, KEMET

Wide band gap (WBG) semiconductors are being designed into power applications because of their improved efficiency over silicon. At higher power levels > 10kW silicon carbide (SiC) is currently dominating the application space but some manufacturers have recently demonstrated gallium nitride (GaN) field effect transistors (FETs) with 900V rating so suitable for higher power. In both cases these WBG semiconductors operate at higher switching frequencies, higher junction temperatures and higher voltages changes the types of passive components required. Automotive power requirements, moving from internal combustion engines (ICE) through mild hybrid electric vehicles (HEV), to full HEV then battery operated electric vehicles (BEV) and chargers are increasing WBG adoption. To keep current levels manageable at higher power levels the operating voltages are increasing from 450 to 900V. This presentation reviews the impact of these requirements on the capacitors and magnetics required. The capabilities of film, electrolytic and multi-layer ceramic capacitors are reviewed and contrasted. Recent KEMET developments with respect to accelerated testing of high voltage MLCC to demonstrated long term reliability are presented along with a technology for more energy efficient packaging of these capacitors. The application trends for the different capacitor types in SiC inverters are described and a Roadmap for the high density packaging is shown. New magnetic materials developed for high saturation power inductors and high impedance EMI filters are reviewed. Application of these in water cooled boost power inductors (50-150kW), composite power inductors, dual mode EMI choke coils and bus bar EMI cores are shown.

W.1 AEC-Q200 Document Revision Status & Discussion
Moderator: AEC Q200 Technical Committee

2.1 Aluminum Gate Wire Fatigue Generated Using Power Cycles

M. Santopa, STMicroelectronics

Automotive applications are showing challenging trends toward higher ambient temperatures and longer lifetime requirements (more heat losses, higher integrations, mounting near engines); therefore more reliable and higher temperature resistant ECU's are required in Automotive IRD. For this reason, the reliability of the interconnections (wire bondings) between die and package's external leads is fundamental for the automotive devices' lifetime and the proper function in harsh environments. In this paper, a reliability characterization study was performed on an automotive package by applying "burst" power cycles stress (pulsed-modulated current) aimed to stress the Al gate wires (7 mils thick) much heavier than a standard Ton/Toff power cycle. Ids burst current waveform is formed by approximately 188 pulses for a Ton=2sec, f=94Hz, duty cycle=17.8%. Virgin and "pre-conditioned" devices were used for the study in order to check the floor life time and environment influence as well. During the characterization it was found that the so-called "pre-conditioned" units showed a worse behavior. In particular, the burst current was intermittently degraded in one or more parts of the its pulses, corresponding to a RdsON increase. On the contrary, virgin units resulted working properly even at end test. Failure analyses of the anomalous units revealed no degradation of the inner layers (e.g., Ag sintering creeping, die crack, etc.), but after definite laser etch on selective windows on wire bonding areas for epoxy removal, it was noticed the cracking of both 7 mils Al gate wire stitches (double stitch bondings on AMB's Cu pad). These cracks resulted the physical root cause of the intermittent Ids behavior on "pre-conditioned" units. For double check, failure analysis was also performed on virgin units. No cracks on Al gate wire stitches were detected at end of stress test. In conclusion, the use of pulsed current cycling is a valid reliability stress test for highlighting and amplifying Al wire bonding fatigue (evolving in wire cracks and consequent gate intermittences). In this paper, this kind of physical failure mode resulted to be the only one that was activated by burst current cycling and that led the "pre- conditioned" devices to a premature failing.

2.2 Reliability Qualification of a 35 mohm 650V, 175C, GaN FET for Automotive Applications

R. Barr, Transphorm Inc.

The performance of 650V GaN FETs are well matched to the needs of the automotive industry, and will be adopted as concerns about reliability and robustness are addressed through accelerated testing and field data. One of the challenges facing the design and development of high voltage GaN FETs is reliability qualification at the full VDS rating and at elevated temperatures, as devices tend to fail parametrically due to "current collapse" and catastrophically breakdown due to design limitations and defects introduced during the fabrication process. This paper will review the Q101 compliant qualification data for a 650V, 175C rated GaN FET. A key difference between GaN technology and Silicon technology is that GaN enables the use of voltage for accelerated testing for Early Life Failure Calculations(extrinsic reliability). Voltage accelerated testing must be carefully implemented to achieve relevant data. In addition field reliability data will be presented along with the overall methodology used to qualify products for automotive applications.

2.3 Safety Condition Verification during Short Circuit Test on Plastic Encapsulated PMOS in H-Bridge Configuration

G. Corrente, STMicroelectronics

The control systems development of electric motors based on inverters, involved an ever-widening diffusion of microcontrollers driving H-bridge circuit. In general, an H-bridge circuit allows to control the power flow on every electric load, so during the last years the technical applications of this circuit had a big diffusion both on automotive and on consumer field. During the normal working of an H-bridge circuit, the microcontroller has to avoid activating all devices at the same time. Considering the H-bridge circuit, if the PMOS are activated at the same time a short circuit will occur between power supply and ground. If the devices are not suitably dimensioned they could go up in flames during short circuit current flow. From a safety point of view, therefore, knowing the behavior of above devices in short circuit conditions takes a great importance. In this paper, it is showed a method that allows to study the behavior of H-bridge circuit devices in short circuit conditions and let to test quickly the possible corrective actions. For the H-bridge circuit have been used N PMOS with 3x15mils source wires and molding compound self-extinguishing (according to spec. UL 94-V0). For tests have been implemented where the power supply voltage of H-bridge has been chosen on the basis of a real application. The work shows that short circuit outcome depends on carrying out typology of the same short circuit. On the basis of the value of resistor on gate of switch device have been realized two short circuit typologies. It is showed that on the basis of typology, the short circuit can cause flames on devices of H-bridge circuit. In particular, if the current pulse rising edge is steep, H-bridge devices blow up. Instead if the edge is jagged, devices burn. Same tests have been performed, moreover, using devices with wire bonding section increased from 15 to 20 mils. The work shows that whatever it might be the short circuit typology, no device goes up in flames. In fact, if the current pulse rising edge is steep, H-bridge devices blow up after about 8s with instantaneous current drop to zero and if the edge is jagged devices blow up as well. The method showed in the paper, therefore, allows to know the behavior of H-bridge circuit devices in a real short circuit conditions and to test quickly the possible corrective actions (e.g., BOM changes).

2.4 Heterointegration of Silicon and GaN LED Technology for Automotive Headlamps

J. Jablonski, OSRAM

Advanced forward lighting systems especially adaptive driving beams in the ECE regulation area have progressed from mechanical systems to LED Pixel solutions. Current approaches face a limit in the number of individual LED pixels given by the discrete component integration. A substantial new concept is the stacking of an active driver silicon IC and a light emitting LED Array on Gallium Nitride basis. The presentation will cover the device architecture and applications. Such “hybrid” LED packages (including ICs, and with the main function of light emission) are currently not yet covered by AEC Q102. First ideas will be presented how Q102 could be extended to cover such innovative components, taking into account the concepts of Q104 for MCMs.

W.2 AEC-Q101 Document Revision Status & Discussion

Moderator: P. Turlo, ON Semiconductor, & AEC Q101 Technical Committee

W.3 AEC-Q102 LED Qualification Document Revision Status & Discussion

Moderator: S. Sibrel, Harman International, and AEC-Q102 Sub-Committee

W.4 AEC-Q103-002 MEMS Pressure Sensors Document Status & Discussion

Moderator: Dr. M. Blyznyuk, Melexis, & AEC-Q103-002 Sub-Committee

3.1 Wire Bond Integrity Investigations using Advanced Pull/Shear Data Analysis

U. Abelein, Infineon Technologies AG

Wire bond integrity assessment is the core element of AEC-Q006. The standard was initially created to demonstrate the automotive capability of a Cu wire bond system. Therefore, an analysis of wire pull and shear force data is mandatory in the AEC-Q006 qualification flow. Pull and shear force data are assessed with respect to given standardized specification values as pass or fail. The results provided by this method are necessary to ensure automotive grade reliability but not sufficient to support a zero defect approach. More sophisticated methods of data analysis allow to extract much more information from the same set of wire pull and shear force data. In this presentation the advantages of using CDF (cumulative distribution function) probability plots for wire integrity data assessment will be demonstrated by a case study. It will be shown that CDF probability plot based data assessment allows to ensure an intrinsic ppm level reliability of the interconnect, as well as a comparable interconnect strength for all wires within a package. Furthermore even irregularities during the pull or shear test can be detected. This supports a zero defect approach and at the same time does not cause additional test efforts.

3.2 Application of Inline Defect Part Average Testing (I-PAT) to Reduce Latent Reliability Defect Escapes: Feasibility Study Results at NXP

J. Witowski, NXP Semiconductors

The detection of latent reliability defect (LRD) escapes is one of the most critical requirements to meet semiconductor Zero Defect goals for automotive quality. Latent defects may be of a size, type or location that do not initially kill the die, or they may lie in an untested area of the die. In either case, the die passes electrical test and escapes into the automotive supply chain. The demanding automotive environment of high heat, humidity and vibration can subsequently activate a small portion of these defects, leading to a premature failure. At the 2017 and 2018 AEC Technical Workshops, KLA Corporation proposed a methodology for latent reliability defect reduction through the application of Part Average Testing principles to inline defect and metrology data (I-PAT). NXP Semiconductor's ATMC fab (Austin TX) is one of the first facilities worldwide to investigate production implementation of this methodology. Specifically, KLA, NXP, and Optimal+ Corporation have formed a three-way proof-of-concept project to investigate the feasibility and value of combining defect data from I-PAT with electrical test results to make better overall decisions on die disposition. This "look back" study examines inline inspection data collected over a period of one year on two automotive devices. The inline data will be correlated with electrical test performance at both Wafer Sort and Final Test, including normal burn-in failures (to demonstrate improved test coverage), intensive burn-in failures (to activate latent reliability defects), and failure analysis from previous field returns.

Results from this study will demonstrate:

- The combination of inline defect inspection data and test data to improve overall product quality and reliability performance through:
    - Screening of statistical outliers based on defect inspection data
    - Improvement of any Geographic Part Average Testing (G-PAT) algorithm (such as GDBN, Cluster or Z-Axis PAT)
    - Improvement of Parametric Part Average Testing (P-PAT)
- Any possible correlation between electrical test and inspection data
- The capability to implement Machine Learning model in production for adaptive testing at burn-in based on a quality index using both test and defect inspection data

3.3 Fractional Failures Sampling - Equivalent to Zero Failure Sampling Plans

H. Lewitschnig, Infineon Technologies AG

100% inspection and random sampling are basic quality tools that are typically used in any production process and in the automotive industry as well. The automotive quality standard IATF16969:2016 describes acceptance criteria for random samples. For attribute data sampling, an acceptance criteria of 0 failures is required (section 8.6.6). Sampling plans are characterized by their operating characteristics (OC) curve. This reflects the likelihood to accept a sample as a function of the portion of defects in the basic set. The 0 failures sampling plan outperforms any sampling plan that allows failures with respect to the OC curve. This is a justification to require 0 failures sampling plans. Once a failure occurs, a countermeasure is introduced with a certain efficiency ϑ. If we add this information to the random sample and increase the sample size, we can show that the OC-curve becomes at least as good as the original 0 failures sampling plan. This is never achieved by sampling plans that allow failures! With this model, we developed an alternative method to 0 failures sampling plans. This can have a huge impact to the industry. Sampling might not necessarily be repeated once failures occur, but the information of introduced countermeasures is added to the sample. The result is very easy to handle and very transparent in the alignment and communication to customers.

3.4 Industry ESD Qualification Harmonization

A. Righter, Analog Devices

Today's automobiles are requiring ever more complex ICs to process the increased data - I/O frequencies of the many automobile applications including sensing, monitoring, and passenger safety. As IC technology scales to finer transistor size / linewidths, transistor count increases, and package capacitances increase, with ESD robustness (particularly for CDM) decreasing for the same IO area. The cost and time to develop larger AEC ESD target-robust circuits for high performance / high volume applications affects time to market. The inconsistency between the AEC and commercial ESD requirements, which follow ESD standards of JS-001 and JS-002 with their different test procedures, leads to confusion and does not take into account the same manufacturing facilities / controls used for both automotive and commercial system manufacture. It is past time to address this. The electronics industry is standardizing on JS-002, with the IEC, ESDA, JEDEC, MIL-PRF-38535 all specifying JS-002 for ESD testing, and will also be incorporated into Q100-011/Q101-005 soon. We propose a harmonization methodology for automotive applications that takes into account the manufacturing process ESD controls and the known safe levels for commercial product handling (250V HBM / 250V CDM) for high speed / high performance I/O.

4.1 Navigating "Road to Zero Defects" for Virtual 0-PPB Reliability in Semiconductor Products

L. Sheng, ON Semiconductor

To meet the "Zero Tolerance for Defects" policy or "Zero-Defects Quality" target has been our ultimate goal of excelling in reliability. This is especially vital for our customers to deploy electronic products in potentially life-threatening environments (incl., automotive). However, defects in semiconductor products are unavoidable due to the dramatically increased complexity in both design and manufacture. Consequently, to implement the complementary mitigation methods becomes the only path towards achieving the virtual 0-PPB reliability. To illustrate the relentless efforts required, this presentation will provide several case studies throughout all the stages from product designs to final tests. Our safeguards include design-for-reliability awareness, inline optical and electronic means of detecting defects, process maturity, and test-for-reliability practices at both silicon disposition and product sorts. Through the extensive and insightful efforts, we've achieved the virtual 0-PPB goal by navigating on these aspects along our "Road to Zero Defects".

4.2 Statistical Method to Ensure 1PPM Product Lifetime for Automotive

J.W. Young, TSMC

AEC-Q100 has clearly defined automotive product qualification procedure (stress conditions, sample size, etc.), yet there is no industry standard for lifetime prediction at use condition for gate oxide TDDB degradation. Historically, TDDB degradation has been ascribed using weakest link model and follows Weibull distribution; however, the continuous scaling of oxides and introduction of HK/MG dual gate stacks has led to deviation of TDDB distribution from Unimodal to Multi-modal Weibull distributions. This non-linear distribution has added complexity and inconsistency in extrapolation of lifetime prediction at use condition (< 1ppm for automotive applications) across industry. A statistical learning based self-consistent clustering model is proposed which can accurately predict oxide lifetime at low failure rate (< 1ppm). Agglomerative hierarchical clustering is performed on raw data to achieve 90% confidence in Weibull fitting and each cluster's weight is calculated. Bayesian Information Criterion for each cluster is calculated and cluster with minimum BIC is chosen so as to avoid problem of over/under fitting of data. Data of cluster with minimum BIC is scaled to desired sample size based. Finally, all the data is cumulated together to achieve one single Weibull distribution. To validate the accuracy of the model, large sample sizes of NMOS TDDB from 16nm and 7nm technology nodes were used for this study. A 20X improvement was observed for lifetime at 1ppm as compared to current bi-modal method. Based on Si-data validation, the self-consistent clustering model can accurately predict lifetime for stringent automotive requirement of < 1ppm.

4.3 Toward Zero Defect: Automotive Fab Best Practices for Assessing "Best Performing Tools"

Dr. J. Robinson, KLA Corporation

Most fabs today produce a mix of automotive and consumer semiconductor devices. Under pressure to improve aggregate semiconductor reliability, automotive Tier 1s and OEMs commonly specify that their wafers receive an automotive service package that includes routing through only the "Best Performing Tools." The goal of this requirement is to both maximize the process window at that manufacturing step and to minimize the step yield loss from random particle contribution. All stakeholders in this effort would benefit from understanding the elements of a comprehensive and effective method for conducting this study, as well as the impact of common errors that diminish the integrity of the assessment. The information produced in a rigorous "Best Performing Tool" program has multiple benefits. It not only identifies the process tools least likely to produce reliability defects, it also identifies those tools in need of remediation while establishing a baseline for proactive fleet-wide improvement. This iterative process results in lower defect density and therefore higher yields and reliability for the entire fab, as well as improving cycle time by offering multiple acceptable paths for wafers through the fab. The method is equally applicable to larger design-rule legacy fabs as well as advanced 300mm designs.

The Best-Known Method outlined in this paper will address the following elements:

- Metrics for success
- Factors in establishing an actionable baseline. Mistakes that can invalidate the results
- Identifying the Best Performing tools and isolating at-risk tools
- Stressing/Partitioning techniques to isolate sources of defects and variation and prioritizing what matters
- Validating changes and improvements effectively
- Considerations for long-term continuous improvement employing this method

Users of the method detailed here will receive actionable information to assess, initiate or improve the "Best Performing Tool" approach to their Zero Defect requirements.

5.1 Applicability of Standard Test Conditions and Requirements in the AEC Standards

R. Rongen, NXP Semiconductors

In the last couple of years, AEC has been discussing how to use application mission profiles in relation to the qualification standards. This resulted into the addition of, meanwhile well known, Appendix 7 to AEC-Q100, -Q101 and -Q102. The application mission profile of the semiconductor component, which is derived from the one of the ECU, is the starting point in the flow chart in Appendix 7. Consequently, it triggered a couple of interesting contributions and discussions in subsequent AEC workshops on the need for standardizing these mission profiles; more recently also driven by new application areas like battery charging or ADAS systems [1,2,3]. The grades in AEC-Q100 according to the operating ambient temperature range, are not sufficiently detailed in an increasing number of cases. In this paper, another step in this flow chart will be in the focus: the selection of test conditions and determination of duration requirements. It is taken for granted that conditions and durations commonly used are still valid, in some cases even after more than 20 years. This is specifically the case for environmental tests like HTSL, TC and HAST/THB. Standardized test conditions and duration requirements only apply when the relevant failure modes are covered, the acceleration of the underlying physical, chemical or electrical mechanisms is "true" (meaning non-relevant failures due to overstress cannot occur), as well as related acceleration models are understood and underpinned with data. Over the past decades, advanced technologies, materials and constructions have been developed and released for which this is not per definition the case. Examples will be presented to initiate the discussion to what extent the pallet of reliability tests methods, conditions and test duration requirements as currently used in the AEC (and JEDEC) standards still apply.

References:

[1] Extended Lifetime Qualification based on Standard Mission Profiles, Ulrich Abelein, Infineon Technologies AG, AEC-RW Detroit 2018

[2] Continental AEC-Q100 Improvement Proposals, Qualification Gap Closure for Systems-On-Chip, Carsten Ohlhoff, Continental, AEC-RW Munich 2018

[3] Qualification Requirements for Components Using Copper (Cu) Wire Interconnections, AEC-Q006-rev (June 8, 2015) and rev A (July 1, 2016)

5.2 Process Reliability and Integrated Circuit Qualification for Mission Profile of Over Grade Ambient Operating Temperature

T. Cheng, MediaTek, Inc.

A comprehensive process reliability qualification method for the integrated circuit (IC) component is reported corresponding to the electronic control unit (ECU) test requirement and mission profile. Through an appropriate methodology shown in this paper, the wafer process reliability specification is determined logically for the zero failure during mission profile lifetime, ECU high temperature endurance test, and IC high temperature operating life (HTOL) test. The process reliability parameter of acceleration lifetime testing data is scattered in the cumulative failure chart which is derived from probability density function (PDF) to cumulative density function (CDF). The real use lifetime is extrapolated by the temperature and voltage acceleration factor converting. And the final zero failure guarantee for a mission profile, ECU test requirement and IC HTOL test has to be determined in it. There are some scenarios of over grade ambient operating temperature (Ta) in the ECU test condition and mission profile. In this paper, we demonstrate the effectiveness of IC AEC-Q100 HTOL coverage on the over grade Ta ECU test condition and mission profile by calculating their equivalent test condition of HTOL. The methodology and equation for the equivalent ECU test and mission profile is established in this paper.

5.3 Practical Application of the Measurement Systems Analysis (MSA) for Automotive Semiconductor Process Control

D. Sutherland, KLA Corporation

Process control tools are the "eyes and ears" of a semiconductor fab – providing the tools necessary to monitor processes, flag excursions, disposition wafers and drive corrective actions. Process control falls into two main categories: metrology is the act of measuring physical features of the die (critical dimensions, film thickness, etc.) while defect inspection is the act of searching for defects (pattern deformations, particles, etc.) that are not supposed to be present. Automotive semiconductor IC manufacturing requires process control after nearly every process step in order to meet the stringent IC reliability requirements. Every measurement/inspection generates two questions: (1) What do I do with this lot?, and (2) What do I do with this process? The ability to effectively answer these questions depends on the capability of the tools used to make the measurement. The AIAG Measurement Systems Analysis (MSA) document provides general guidelines for assessing the quality of any measurement system used in the production of automotive parts. However, KLA has found that there is frequent confusion in understanding how these standards apply to semiconductor fab inspection and metrology due to the complex nature of these operations. In this paper we will review the criteria that define adequate capability for metrology and inspection tools and provide practical guidelines to help fab process control engineers make appropriate implementation decisions.

6.1 Board Level Reliability of Packages for Automotive Electronics

J. Bae, Samsung Electronics

For the evaluation required in AEC-Q100, Q104 and requested by BLR (based on IPC-9701) in various Tier-1, Samsung is pursuing it in a standardized way, and is studying how to satisfy specifications and how to accelerate evaluation. For the evaluation board, it was selected as the most commonly used PCB thickness through bench marking, and the board size was 132x77mm according to the drop test guidance (JESD22-B111) of JEDEC, and the BLR TC / Drop evaluation of Samsung product was conducted. So, we would like to introduce the study of factors that affect Board level reliability (Solder ball composition, Size, Pad Design, etc.).

6.2 SAE J3168 Reliability Physics Analysis of Electronic Equipment, Modules and Components Update

K. Hodgson, Ford Motor Company, & James McLeish, DfR Solutions

The Reliability Physics Analysis Standard SAE J3168 is being jointly developed by the SAE Automotive and SAE Aerospace divisions for use on Electrical, Electronic, and Electromechanical (EEE) equipment in Automotive, Aerospace, Defense and other High-Performance (AADHP) industries. The core document for the RPA recommended practice standard is nearing completion. It defines a science based process for reliability optimization, failure risk assessments and risk elimination through the use of Computer Aided Engineering (CAE) durability simulations. The objective is to determine if the EEE component sets selected for an application and the custom designed Printed Circuit Board (PCB) that provides electrical connections and structural support, as a system are able to reliably endure a service life under the application's intended environmental and usage conditions. RPA provides the ability to identify failure risks during EEE product design creation, so that any risks can be designed out or mitigated in order to achieve both component and Board Level Reliability (BLR) and produce Ultra Reliable and Safe EEE equipment. This presentation will provide an overview of the J3168 RPA process and discuss the information required of EEE component in order to be used in the durability simulations.

6.3 EIPD: A New Acronym for An Ageless Problem
J.J. Hajjar, Analog Devices

Electrically Induced Physical Damage (EIPD) persistently occupies the top bar of Integrated Circuit (IC) failure Pareto charts. This damage may result from IC manufacturing process defects, poor ESD/EMI controls in the assembly process, and / or flawed outgoing electrical testing. The majority of such failures are reported as customer-induced in product analysis reports. General best practice mitigation guidelines are subsequently proposed to the customer. However, increasingly, customers have taken issue with the assignment of the failure to their end-application. To address this concern a new customer support model was created, consisting of providing additional insight into the nature of the observed damage (and its suspected electrical path/severity of event) to the customer. This involves a detailed review of the failure analysis report, cross-referencing the die damage site with the schematic and, also, the corresponding layout of the circuit, with additional support upon customer request. This presentation describes this customer support model including case studies where EIPD was identified and the corrective action implemented to address the damage. It will also be shown that contrary to conventional wisdom, such root causes do not always stem from IC customer misapplication.

W.5 AEC-Q004 Zero Defects Activity Update & Discussion
Moderator: R. Rongen, NXP Semiconductors, & Q004 Sub-Committee

W.6 AEC-Q105 Touch Screen & Display Modules Activity Update & Discussion
Moderator: R. Kinyanjui, John Deere, & AEC Q105 Sub-Committee

W.7 AEC-Q100 Document Revision Status & New AEC Initiatives
Moderator: U. Abelein, Infineon Technologies AG, & AEC Q100 Sub-Committee

W.8 AEC-Q104 Multi-Chip Module Activity Update & Discussion
Moderator: T. Lawler, Lattice Semiconductor, & AEC-Q104 Sub-Committee