Automotive Electronics Council

Component Technical Committee

Agenda

(subject to change)

2008 - Thirteenth Annual
Automotive Electronics
Reliability Workshop

May 6, 7, & 8

Novi, MI
Sheraton Detroit Novi Hotel

Tuesday, May 6, 2008				
		7:30 am - 8:00 am	**Continental Breakfast (provided)**	
		8:00 am - 8:20 am	**Workshop Introductions**	
Session 1: Passive/Electro-Mechanical Issues 8:20 am - 10:25 am	**1A.1**	8:20 am - 8:45 am	Ron Demcko *AVX*	FlexiSafe MLCC Termination Device Performance
	1A.2	8:45 am - 9:10 am	Kazuo Kasue *Murata*	Investigation of the Environmental Conditions of Electronic Components for TPSM
	1A.3	9:10 am - 9:35 am	Reiner Kuehl *Vishay BComponents*	Advance Properties of Thin Film Resistors: Pb-free As A Vehicle for High Reliability and Better Performance Demands
	1A.4	9:35 am - 10:00 am	Ron Demcko *AVX*	Multilayer Varistor Performance in Automotive Environments
	1A.5	10:00 am - 10:25 am	Michael Azarian *University of Maryland (CALCE)*	Reliability of Flexible Termination Ceramic Capacitors in Temperature-Humidity-Bias Conditions
		10:25 am - 10:45 am	**BREAK: Coffee, drinks, snacks (provided)**	
Breakout Session		10:45 am - 12:50 pm	**Q200 Document Review & Discussion**	
Session 2: Discrete Semiconductor Issues 10:45 pm - 12:50 pm	**2A.1**	10:45 am - 11:10 am	Arthur Chiang *Vishay SIliconix*	Backside Emission Microscopy for Discrete Power Devices
	2A.2	11:10 am - 11:35 am	Harold Anderson *ON Semiconductor*	Copper Wire Bond: A Comprehensive Approach to Process Characterization
	2A.3	11:35 am - 12:00 am	Romeo Letor *STMicroelectronics*	New Spiked Gate Stress for Robustness Validation of Power MOSFET in the Automotive Environment
	2A.4	12:00 am - 12:25 am	Nishad Patil *University of Maryland (CALCE)*	Failure Precursors for Insulated Gate Bipolar Transistors (IGBT)
	2A.5	12:25 pm - 12:50 pm	Arthur Chiang *Vishay SIliconix*	ESD Characterization of Trench Power MOSFETs under CDM Model
		12:50 am - 2:15 pm	**LUNCH (on own)**	

Tuesday, May 6, 2008 (continued)				
Session 3: **General Component Issues** **2:15 pm - 3:30 pm**	**3A.1**	2:15 pm - 2:40 pm	Michael Azarian *University of Maryland (CALCE)*	Organizational Reliability Capability Assessment of Electronics Manufacturers
	3A.2	2:40 pm - 3:05 pm	Sony Mathew University of Maryland (CALCE)	Prognostics and Health Monitoring of Electronic Products
	3A.3	3:05 pm - 3:30 pm	Gerold Will *Continental*	Automotive Component Quality Requirements
		3:30 pm - 3:50 pm	**BREAK: coffee, drinks, snacks (provided)**	
Session 4: **Zero Defects (Part 1)** **3:50 pm - 5:05 pm**	**4A.1**	3:50 pm - 4:15 pm	Yael Cohen *OptimalTest*	Outlier Management Solution
	4A.2	4:15 pm - 4:40 pm	Justin Judkins *Ridgetop*	Die-Level Process Monitors Provide Foundry-Independent Device-Level Parameters and Performance
	4A.3	4:40 pm - 5:05 pm	Stephen Pateras *LogicVision*	The Embedded Path to Zero Defect Integrated Circuits
		5:05 pm - 7:00 pm	**DINNER (on own)**	
AEC Panel Discussion		7:00 pm - 9:00 pm	**Q101 Document Review & Discussion**	

Wednesday, May 7, 2008				
		7:30 am - 8:00 am	**Continental Breakfast (provided)**	
Session 5: **Pb-Free Issues** **8:00 am - 9:15 am**	**5A.1**	8:00 am - 8:25 am	Sony Mathew *University of Maryland (CALCE)*	Lead-Free Electronics: Tin Whisker Growth, Risk and Mitigation
	5A.2	8:25am - 8:50am	Min Ding *Freescale*	Sn3.5Ag and Sn3.8Ag0.7Cu Pb-free Alloys for Automotive BGA Application on Ni-Au Finish
	5A.3	8:50 am - 9:15 am	Hiroshi Yamashita *NEC Electronics*	Tin Whisker Growth Evaluation on Solder Joint
Session 6: **Zero Defects (Part 2)** **9:15 am - 10:05 am**	**6A.1**	9:15 am - 9:40 am	Kuotung Cheng *TSMC*	In-Situ Process Variation and Outlier Reduction
	6A.2	9:40 am - 10:05 am	Ruby Clark *Freescale*	Zero Defects Implementation-Holistic Approach in a Manufacturing Environment
		10:05 am - 10:25 am	**BREAK: Coffee, drinks, snacks (provided)**	
Session 7: **Zero Defects (Part 3)** **10:25 am - 11:15 am**	**7A.1**	10:25 am - 10:50 am	Dileepan Narayanan *Cypress*	Analysis of Wafer Bin Map Patterns for Lonely Die for Reduction of Customer Returns
	7A.2	10:50 am - 11:15 am	James Williams *Texas Instruments*	Zero Defects Launch Approach
Session 8: **Packaging Issues** **11:15 am - 12:30 pm**	**8A.1**	11:15 am - 11:40 am	Mike Varnau *Delphi Corporation*	Characterization of BGA Warpage in Simulated Solder Reflow
	8A.2	11:40 am - 12:05 pm	Galen Lin *Integrated Silicon Solution Inc. (ISSI)*	A Study on the Relationship between Epoxy Fillet Height and Device Performance in Function and Reliability
	8A.3	12:05 pm - 12:30 pm	Daniel Vanderstraeten *ON Semiconductor*	Impact of Mold compound Filler Particles on Local Thermomechanical Stress Variations
		12:30 pm - 2:00 pm	**LUNCH (on own)**	

Wednesday, May 7, 2008 (continued)				
Session 9: **Failure Analysis** **2:15 pm - 3:30 pm**	**9A.1**	2:00 pm - 2:25 pm	Eric Bedes *NEC Electronics America*	Failure Analysis Techniques for Marginal Semiconductor Devices
	9A.2	2:25pm - 2:50pm	Mike Azarian *University of Maryland (CALCE)*	RF Impedance Analysis for Reliability Monitoring
	9A.3	2:50 pm - 3:15 pm	Yizi Xing *NXP Semiconductors*	Fast Fault Diagnosis for Analog IC's
	9A.4	3:15 pm - 3:40 pm	Michael Wieberneit *NEC Electronics Europe GmbH*	FIB Assisted EMI and OBIRCH Analysis
		3:40 pm - 4:00 pm	**BREAK: Coffee, drinks, snacks (provided)**	
Session 10: **Electrostatic Discharge** **4:00 pm - 5:50 pm**	**10A.1**	4:00 pm - 4:25 pm	Michal Polewski *NXP Semiconductors*	Comparison of JEDEC and Q100 Standards and New Q100 ESD-CDM Calibration Issues
	10A.2	4:25 pm - 4:50 pm	K.T. Kaschani *Atmel*	The Significance of the Machine Model to the ESD Qualification of Integrated Circuits
	10A.3	4:50 pm - 5:50 pm	Charvaka Duvurry (et al) *Texas Instruments*	Proposal for the Reduction of ESD Compliance Levels (Audience Participation)
		5:50 pm - 7:30 pm	**DINNER (on own)**	
AEC Panel Discussion		7:30 pm - 9:00 pm	**Q100 Document Review & Discussion**	

Thursday, May 8, 2008

COFFEE (provided)		7:30 am - 8:00 am	**Continental Breakfast provided**	
Session 11: Qualification Issues 8:00 am - 10:05 am	**11A.1**	8:00 am - 8:25 am	An-Chi Kang *TSMC*	Comprehensive Requirements and Qualifications of Die Fabrication Reliability - Technology Platforms of 0.8µm to 45nm and Beyond for Automotive Applications
	11A.2	8:25 am - 8:50 am	Mike Wang *NEC Electronics*	Reliability Integration and Assurance in Manufacturing Process Transfer
	11A.3	8:50 am - 9:15 am	Paul Ngan *NXP Semiconductors*	Knowledge Based Qualification at NXP: Know the Failures to Guarantee NO Failures
	11A.4	9:15 am - 9:40 am	Lieyi Sheng *ON Semiconductor*	Reliability Enhancement by Suppression of Nano-Dendritic Defects in MIM Capacitors in Integrated Circuits
	11A.5	9:40 am - 10:05 am	Kirsten Roedle *NXP Semiconductors*	Defect Detection With Cold Testing in Automotive Qualification
		10:05 am - 10:25 am	**BREAK: Coffee, drinks, snacks (provided)**	
Session 12: Test & Statistics 10:25 am - 11:40 am	**12A.1**	10:25 am - 10:50 am	Tim Haifley *Altera Corporation*	Why Statistical Bin Limits Fail
	12A.2	10:50 am - 11:15 am	Erik Marinissen *NXP Semiconductors*	Embedded Multi-Detect ATPG and Its Effect on the Detection of Unknown Defects
	12A.3	11:15 am - 11:40 am	Tim Haifley *Altera Corporation*	To Bayes or Not to Bayes: ELFR (or How to Sharpen Those Limits)
Session 13: NVM & Memory Issues 11:40 am - 12:55 pm ** Refreshments available during session	**13A.1**	11:40 am - 12:05 pm	Chin-Piao Chang *TSMC*	Non-volatile Embedded Memory Solutions for Automotive Products
	13A.2	12:05 pm - 12:30 pm	Terry Pence *Actel Corporation*	Designing Safety Critical Systems for Neutron and Alpha ParticleSingle Event Effects Failures
	13A.3	12:30 pm - 12:55 pm	M. Janai (et al) *Spansion*	Thermal Acceleration Factors for Qualification of Trapping-Based NVM Products with Cycling Bake Intervals
WRAP-UP		12:55 pm - 1:10 pm	AEC Technical Committee	Closing Statements & Workshop Adjourned