Session 1A: Passive/Electro-Mechanical Issues

Tuesday, May 6

8:20 am – 10:25 am

1A.1 FlexiSafe MLCC Termination Device Performance

Ron Demcko, AVX

Designers have taken painful and extreme measures to insure that MLCCs used in Vcc filtering of modules and circuits will not crack during process or encountered use environments. Designer concern over performance is paramount - a failed, cracked MLCC could potentially lead to catastrophic failure of the module, system and automobile. This paper will discuss the impact of conductive polymer sub-layer termination materials upon MLCC performance in high flexure and temperature cycle environments. The effects of a modified electrode structure resulting in two series capacitors within a single polymer sub-layer terminated MLCC package will be documented and discussed relative to board flexure, strain and high temperature cycle environments. Alternate layout rules will be given.

1A.2 Investigation of the Environmental Conditions of Electronic Components for TPSM

Kazuo Kasue, Murata

In the automotive market, high reliability under increasingly severe environmental conditions is required of electronic components. With increase of automotive electronics applications, mounting of electronic components in the automobile has spread over a wide range of locations. Electronic components used for TPMS (Tire Pressure Monitoring System) are mounted inside vehicle tire. This is one of the harshest environments in the automobile. Within the tire exists a complex combination of environmental stresses consisting of temperature, humidity, vibration, mechanical shock, centrifugal force, corrosive gas, and pressure. For a limited range of conditions, we have measured the inner-tire environmental conditions (temperature, humidity, vibration, and gas, etc.) The purpose of this paper is to present the research on the environmental stresses associated with the TPMS application and examine its influence on component reliability.

1A.3 Advance Properties of Thin Film Resistors: Pb-free As A Vehicle for High Reliability and Better Performance Demands

Reiner Kuehl, Vishay BComponents

Thin Film Resistors are well established mass products in passive component market. With the introduction of Pb-free not only some problems but also new opportunities have arisen. Maximum solder joint temperatures can be extended from 110°C today (SnPb or SAC) to 140 or 150°C by the use of special Pb-free solders. New demands in stability, reliability of components and solder joints, and application at elevated environmental temperatures up to 175°C under the hood are demands for the near future in automotive electronics. Mission profiles will define the conditions of use in an intended application in combination with high robustness of solder joints against thermo cycling. High temperatures strongly influence the fitness for use at today's commodity resistor designs, especially at critical temperature condition and humid environment.

Results of new developments & optimizations on thin film materials in combination with proper electro-isolation system will be discussed. Their influences to electrical stability, resistance to environmental stress (resistance against humidity) and reliability will be demonstrated, as well as the comparison of solder joint reliability in dependence of the contact design. A new level of electrical properties in combination with the superior MELF case design leads to stability, reliability, and load per case size that is unacquainted so far for mass product resistors in this class.

1A.4 Multilayer Varistor Performance in Automotive Environments

Ron Demcko, AVX

The EMC requirements of today's automotive electronics are a natural fit for the use of MultiLayer Varistors (MLV's). MLV's offer documented advantages of large in rush current capability, high-energy transient suppression and off state bulk EMC capacitance. These, coupled with an extremely low FIT rate and excellent process capability, make MLV's a common device in today's automotive circuit protection. A series of optimized MLV designs are emerging that will allow MLV's to be used in a wider range of existing and future automotive applications. Among the new abilities are:

- **Expanded EMC filter range** - off state EMC capacitance can now be varied from < 1pf to >16nf.
- **Common mode / differential mode suppression MLV's**
- **Low leakage current MLV's** – off state leakage can be in the nano-amp region.
- **Higher energy load dump capable SMT MLV's**
- **150C evolution** – 150C rated MLV's

The impacts of these devices will be discussed relative to existing and next generation circuit optimization. Performance and reliability trends will be discussed and illustrated. Predictions on further developments within the industry will be made.

1A.5 Reliability of Flexible Termination Ceramic Capacitors in Temperature-Humidity-Bias Conditions

Michael Azarian, University of Maryland (CALCE)

Multilayer ceramic capacitors (MLCC's) are a common component of electronic circuits. Flexible termination MLCC's were developed to mitigate "flex" cracking, and have generated great interest within the automotive industry. Although their reduced susceptibility to cracking has been well documented, few independent evaluations of their reliability under environmental stresses are available.

A combination of temperature-humidity-bias (THB) testing and storage testing was performed to compare the reliability of flexible vs. standard termination capacitors. In the THB tests, capacitance, dissipation factor and insulation resistance were monitored in-situ in an 85°C/85% RH environment. The effectiveness of a conformal coating in mitigating degradation in THB conditions was examined. The effect of the presence of a voltage bias, as well as the level of bias, was evaluated by comparing results from the THB test to those from a storage test. In the storage test, individual parts were placed into an 85°C/85% RH environment without being mounted on a board, and electrically characterized on a periodic basis. These results provide a direct comparison of the environmental reliability of the newer flexible termination capacitors to that of standard termination capacitors, which have been in use for many years.

Session 2A: Discrete Semiconductor Issues

Tuesday, May 6

10:45 pm - 12:50 pm

2A.1 Backside Emission Microscopy for Discrete Power Devices

Arthur Chiang, Vishay SIliconix

By relating near infrared (IR) emission as a result of current flow to the underlying device structure under various biasing scenarios, engineers in semiconductor industry have been able to employ emission microscopy as a key tool in yield enhancement, failure analysis, and circuit design debug for more than 20 years. As more layers of metals are added over the years and the critical dimensions keep shrinking, less and less IR emission is able to escape the device top side for conventional microscopic analysis. In addition, some leakage would mysteriously recover after de-capsulation. Turning the device upside down, while leaving the molding compound on die surface intact, provides an alternative analysis venue, but it presents some challenges at the same time. These challenges include overcoming the severely attenuated emission signal and providing biasing conditions to the device. But chief among them is the sample preparation.

In order for IR emission to escape silicon, the substrate would have to be thinned. The extent of thinning required depends on its doping level. For normal integrated circuits where low substrate doping is typically used, a few hundred microns is an appropriate thickness for ease of operation. However, for discrete power devices where substrate is part of the conduction path, very high level of doping is required to minimize the added on-resistance (Rds_{on}) of the device. High doping level substrate absorbs much more IR emission, thus thinning the silicon to below 100 microns is necessary. Thin remaining silicon is not only needed for capturing the escaping IR emission, it is also needed to image the underlying device structure with IR light source that travels through thin silicon and bounces back again. In other words, the external light source is attenuated twice.

Thinning the discrete power devices to below 100 microns itself presents some challenges, especially in packaged form: 1) power devices are usually packaged with thick metal leadframe which needs to be polished off first, 2) the silicon die inside the package is usually not leveled with package outline, thinning would be uneven without careful readjustment during polishing, 3) making electrical contact to the substrate can be a delicate task, and 4) electrical characteristics of the device may change after thinning; all prior efforts are in vain should that happen. Thus, adopting backside emission microscopy to packaged discrete power devices presents an acute challenge for FA professionals.

In this paper, we present a complete backside emission microscopy procedure specially tailored for packaged discrete power devices. The technique can be used for device and process debug during development, yield enhancement during manufacturing, and failure analysis when malfunction occurs during qualification or in field use. Examples will be given for each case. An example below shows a thinned DPAK power MOSFET, the backside contact method, the detected emission at low leakage and the clarity of backside image at high magnification.

2A.2 Copper Wire Bond: A Comprehensive Approach to Process Characterization

Harold Anderson, ON Semiconductor

The introduction of copper wire as an interconnect material in package assembly, as an alternative to gold wire, has recently begun to gain traction. Historically, copper wire bonding has suffered from concerns in two key areas: process efficiency or return on investment (ROI), and risk of die damage (cratering). This paper presents a comprehensive approach to characterizing conventional thermosonic ball bonding as applied to the large wire diameters used in the area of power device technology, devices which are considered to have sensitive structures similar to bond over active circuits (BOAC) typical of integrated circuits. Although the focus here is on the larger diameter, 50um, wire size, the general observations will largely apply to fine wire (<33um) applications as well. The project scope encompassed process capability studies (e.g. wire pull, bond size/weldment area), temperature dependent reliability tests (HTSL and temp-cycle), electrical characterization (RdsON), CuAl intermetallic compound (IMC) formation, and includes initial finite element modeling. Data will show that when properly characterized, copper wire bonding is as reliable as gold wire bonding.

2A.3 New Spiked Gate Stress for Robustness Validation of Power MOSFET in the Automotive Environment

Romeo Letor, STMicroelectronics

Since several years of observation, Power MOSFETS demonstrated a failure rate at PPM level with a failure mode clearly related to a gate stress despite the devices are correctly rated and homologated with the standard gate stress described in the AECQ100. Deeper analysis has demonstrated that the actual standard test for gate oxide is not satisfactory to guarantee 0 failures as it does not represent the real application working condition. This problem can also be observed from a different point of view: In fact most of the time the specification of real working conditions is ambiguous; consequently it is difficult to evaluate the margins between the device specification and the stress applied to the device in the harsh automotive environment. But this way of thinking by reversing the problems can lead to a never ending discussion without converging to a real solution. To make a step ahead and reach the goal of 0 ppM, there is the need to apply a new procedure for homologating devices designated to work in a given environment. By example, the robustness validation method permitted individuating a new test that we named “spiked gate stress”. The presentation demonstrates the validity of the method using a practical example and by discussing the several points that are defined in the robustness validation:

- **Definition of the Mission profile -** This is evaluated by simulating the interaction of the gate oxide with the environment. For example the electrical behavior needs to be evaluated by taking in account the very fast transient voltages that are very difficult to clamp by external and internal protections. It is also necessary to underline that the definitive definition of mission profile needs the full collaboration of third parts. The spectrum analysis of the voltage applied to the gate can be characterized on the productions line and on the field.

- **Indication of the failure mechanism -** There are 3 failure mechanisms for gate oxide (breakdown, trapping and induced leakage). The presentation will describe the physical phenomena that are triggered and how this allows identifying the testing parameter (Voltage, time, temperature...) to emulate the mission profile and then properly characterize the devices. This is demonstrated with practical example using the characterization of Power MOSFETS differentiated by the gate oxide thickness.

This presentation has not the goal to impose a definitive definition of the gate stress, but the intension is to trigger a discussion with the AEC community with the aim to work together and define an effective common way out.

2A.4 Failure Precursors for Insulated Gate Bipolar Transistors (IGBT)

Nishad Patil, University of Maryland (CALCE)

The automotive industry is moving toward hybrid technologies which are environmentally friendly. In hybrid vehicles, insulated gate bipolar transistors (IGBT's) are used as switches in inverters to efficiently convert power between the batteries and the motor. In conventional automotive applications, IGBT's are used in traction motor control and ignition control. The failure of these switches in application could lead to potential downtime or failure of the entire system. It is therefore necessary to be able to determine the precursors to failure for these IGBT devices in order to undertake required maintenance action.

In this study, the failure modes, mechanisms and effects analysis (FMMEA) is performed to identify the critical failure mechanisms at the device level for punch-through IGBT's. The FMMEA analysis results show that the time dependent dielectric breakdown (TDDB), hot electrons and electrical overstress are the critical failure mechanisms for PT-IGBT's. For the critical failure mechanisms identified, the electrical parameters that could be potential failure precursor candidates are listed. Accelerated tests have been performed and selected electrical parameters have been monitored. The results of these tests are discussed. The electrical parameters that are potentially the most suitable precursors to PT-IGBT failures will be presented.

2A.5 ESD Characterization of Trench Power MOSFET's under CDM Model

Arthur Chiang, Vishay SIliconix

Electrostatic discharge (ESD) tests used to mean Human Body Model (HBM) and Machine Model (MM); the former attempts to simulate human, while the latter for the robotic arm, handling of the semiconductor parts during manufacturing, shipping, and assembly processes. It all changed in 2005 when Charged Device Model (CDM) was specified in AEC-Q101-REV-C as one of the two required ESD tests for automotive grade discrete semiconductors. Better understanding of ESD characteristics of discrete power devices under CDM becomes imperative.

The devices may be charged in one of two ways: direct contact or field-induced through capacitive coupling. For direct CDM method, static charges are initially stored in the body of a floating device and then discharged through the external ground. For the field-induced CDM method, the device is initially charged by the filed-induced method without the socket, and then discharged through a grounded metal probe. The device and the package impedance have an important impact on the CDM waveform.

In this paper, CDM characterization was performed for trench power MOSFET's in various packages. The influence of test parameters such as the charging method (direct or field-induced) and discharge mode (contact or non-contact) are studied. For a given test parameter, the impact of the package type, die size and gate oxide thickness are evaluated. For example, the graph below shows the impact of package type to the resultant peak discharge current. The higher the peak discharge current, the more vulnerable the semiconductor device is to CDM induced damage.

Our study shows that power MOSFET's are insensitive to CDM induced damage except a rare combination of small die, large package, and thin gate oxide. This paper will also compare the physical and electrical failure signature of CDM induced damage with that of HBM or MM.

Session 3A: General Component Issues
Tuesday, May 6
2:15 pm - 3:30 pm

3A.1 Organizational Reliability Capability Assessment of Electronics Manufacturers

Michael Azarian, University of Maryland (CALCE)

Electronic systems in automotive applications must satisfy strict and sometimes conflicting demands for safety and reliability under harsh conditions while simultaneously offering high functionality at low cost. Meeting these demands is becoming more challenging as the supply chain for automotive electronics grows increasingly diffuse and international. Competitive pressures are driving automotive manufacturers to use electronic materials, parts, sub-assemblies, and services obtained from lower cost suppliers and facilities.

The extent and effectiveness of a supplier's dedication of resources and effort to reliability, throughout the design, manufacturing, and feedback phases of the product development cycle, can yield important information about the likelihood that the company will provide a reliable product on an ongoing basis. This information can be obtained through assessment of organizational reliability capability, which can be quantified through evaluation of the set of activities associated with each of eight key practices. The results of such an assessment can lay the foundation for partnerships with suppliers to ensure product reliability improvement, and provide a useful basis for supplier selection. This approach also be used for self-assessment, to identify internal reliability practices in greatest need of improvement.

3A.2 Prognostics and Health Monitoring of Electronic Products

Sachin Kumar, University of Maryland (CALCE)

Prognostics and health management (PHM) is a method that permits the reliability of a system to be evaluated in its actual application conditions. PHM facilitates the estimation of the extent of degradation or deviation from an expected normal condition. Assessing the extent of deviation or degradation from an expected normal operating condition for electronics helps meet several critical goals, including advance warning of failures; minimizing unscheduled maintenance, extending maintenance cycles, and maintaining effectiveness through timely repair actions; reducing the life-cycle cost of equipment by decreasing inspection costs, downtime, and inventory; and improving qualification and assisting in the design and logistical support of fielded and future systems.

This presentation will discuss a methodology for conducting prognostics and health monitoring for electronic products. A case study will be presented to demonstrate the implementation of the methodology. The development of a baseline to define the healthy behavior of a product and evaluation of fielded products with respect to the baseline characteristics will be presented.

3A.3 Automotive Component Quality Requirements

Gerold Will, Continental

Although industry standards and various groups have been very instrumental in developing concepts and methods for qualification and testing of parts, Tier-1 suppliers continue to face the challenge of closing the gap between OEM expectations and electronic component quality performance. To help close these gaps, Continental has identified customer specific requirements in addition to industry standards that govern our process of quality control for electronic parts. These quality requirements cover the entire life cycle of the product. A centralized component database is maintained by supplier quality based on measurement of PPM for parts running in production. Use of this database aids designers in reducing risks by reusing parts that are already qualified and have good PPM performance. Qualification and approval standards which are product family dependent allow implementation of lessons learned and govern not only stress testing requirements but also production control and production testing by the part supplier during production. PCN/PTN requirements are defined with consideration for the OEM requirements for validation. A strategic purchasing process utilizes a closed loop control system which continuously uses measurement of supplier performance and modifies our database which drives sourcing strategies. Using "best in class" suppliers for each component family and redefining continuously lower PPM targets for each product family helps implement continuous improvement in meeting our customers zero defect requirements.

Session 4: Zero Defects (Part 1)
Tuesday, May 6
3:50 pm - 5:05 pm

4A.1 Outlier Management Solution

Yael Cohen, OptimalTest

With the constant increase for higher reliability products in an "ever lower cost" industry, the semiconductor testing faces new challenges that are no longer can be satisfied using traditional methods. A paradigm shift is required to switch into much more comprehensive solution that can address the new emergent need – outlier management system.

Outlier Management System (OMS) consist of several application modules that support every aspect of quality and reliability in a very structured process cycle. Starting with detecting outlier events or potential cases using advanced analysis system, configuring the right outlier detection algorithms whether for real time or offline with static limit or moving limits leveraging best known practices and technologies of adaptive testing capabilities etc., through executing these algorithms in a controlled environment for simulation and evaluation purposes all the way to execute them in real production environment, gather the data and monitor for quality.

In pursuing "ZERO DEFECT" environment, semiconductor manufactures needs to address all outlier potential root causes, including process related issues, ATE and hardware related issues and even human related issues. The only way we can march toward "ZERO DEFECT" environment is by being paranoid and take proactive actions accordingly, including setting the right monitors in the right locations, relay more on automated processes and eliminate human errors, apply more and more stages in our overall process to make sure we detect reliability issues in a "near time" fashion and address them as soon as possible. All these and more are few of the aspects of "Outlier Management System" (OMS) concept and methodology.

4A.2 Die-Level Process Monitors Provide Foundry-Independent Device-Level Parameters and Performance

Justin Judkins, Ridgetop

The drive for lean manufacturing and zero defects in the sub-90 nm era call for more aggressive quality control. Shrinking margins require proactive tools supporting yield learning – to focus on finding yield loss signatures instead of defects, to identify the trend and lead toward zero defects implementation. Foundries traditionally use scribe line transistors to determine model parameters and process statistics needed to determine safe design margins. This allows the designer to get higher performance while maintaining good yield, in the presence of process variation. Device characterization by collecting and analyzing empirical data from on-silicon structures is fundamental to practical CMOS circuit design.

A new technique called Die-Level Process Monitoring (DLPM) uses in-situ test transistors with the product circuit to extract critical process parameters during test. DLPM provides direct and independent measurement of Vt, ION saturation current, and resistor or capacitor mismatch. By looking at a number of test devices in sequence, the DLPM gathers the mean values, but also important statistical variation and spread. The test procedure may be simplified by encasing the DLPM in a test structure and serially extracting data through a simple boundary scan interface, reducing test time and supporting bare-die qualification. Since the DLPM and host circuits are subject to the same stresses and processes, this on-chip technique can support failure analysis and other activities. Through a suitable interface, like JTAG, DLPM can be activated to provide parametric data at any time during manufacturing or while in the field. The DLPM solution is low power, compact, and provides direct feedback on performance and yield issues.

4A.3 The Embedded Path to Zero Defect Integrated Circuits

Stephen Pateras, LogicVision

The migration to deeper nanometer technology nodes continues to increase semiconductor manufacturing test challenges. At these smaller geometries there are un-modeled and thus un-anticipated failure mechanisms, many of which affect the performance of the device. Many devices are also experiencing larger and often unpredictable leakage currents which not only increase power but can lead to thermal runaway and thus burn-up in the field.

These quality and reliability issues require a test approach capable of applying test patterns at the rated speed of the device under test. It is also necessary to create stress conditions during test that are equal or higher to functional stress conditions. This will lead to the acceleration of the burn-up process for marginal devices and therefore detection during manufacturing test.

This presentation will describe an advanced logic Built-In Self-Test (BIST) solution incorporating a distributed at-speed timing infrastructure that provides the switching activity and related stress conditions that are seen during functional operation. These are achieved through high scan rates as well as the application of bursts of at-speed functional clock pulses in all clock domains simultaneously. This BurstPhase technology also results in both very accurate at-speed tests as well as very high transition fault coverage. The combination of these factors is key to achieving zero defect levels.

Session 5: Pb-Free Issues
Wednesday, May 7
8:00 am - 9:15 am

5A.1 Lead-Free Electronics: Tin Whisker Growth, Risk and Mitigation

Lyudmyla Panashchenko, University of Maryland (CALCE)

A large number of electronic part manufacturers have adopted pure tin or high tin lead-free alloy finishes, as a replacement to lead-alloyed finishes. A major drawback of using lead-free tin finishes is tin whisker formation. A tin whisker is a conductive tin crystal, which grows spontaneously from tin finished surfaces, often in a needle-like form. Many whisker related field failures have been previously reported by the electronics industry.

It is widely agreed that compressive stress, generated within the tin plating, is a factor influencing tin whisker growth. Compressive stress may result from formation of intermetallic compound formed due to the interaction between the tin and the substrate material. This presentation will detail the tin whisker growth and risk for different conditions and some mitigation studies. Tin whisker growth parameters for different finishes, substrates, and load conditions will be discussed. Some of the mitigation strategies will also be discussed.

5A.2 Sn3.5Ag and Sn3.8Ag0.7Cu Pb-free Alloys for Automotive BGA Application on Ni-Au Finish

Min Ding, Freescale

The eutectic SnAg (Sn3.5Ag) and near eutectic SnAgCu (Sn3.9Ag0.6Cu, Sn3.0Ag0.5Cu) alloys are two major Pb-free alloys that have been studied extensively. Due to the lower creep rate and higher modulus, these Pb-free alloys will induce higher stress level at the solder/intermetallic interface in high deformation rate events such as impact or shock. Therefore, intermetallic (IMC) brittle failures are more likely to occur. At the package level, the direct result of this is increased missing ball yield loss due to IMC fracture in ball grid array (BGA) assembly, test, shipping and general handling. With SnAgCu, the situation becomes aggravated when it is attached to Ni/Au finishes.

The purpose of this work is to compare the performance of these two Pb-free alloys while they are used in automotive applications. BGA packages with different configurations were assembled with both Sn3.5Ag and Sn3.8Ag0.7Cu spheres. Studies were performed at different levels. At the intrinsic material property level, the melting and wetting behavior of the solder alloys were examined by Differential Scanning Calorimetry (DSC) and wettability test. At the solder joint level, cold ball pull (CBP) were used to assess the mechanical strength of individual solder joint at different stress conditions (as-assemble, multiple reflow, high temperature storage, etc.). The brittle fracture failure rate from this comparative test is believed to have correlation to the missing ball rate in the field. At the same time, the geometry of the spheres such as ball height/diameter and positioning were also recorded and compared. At the package level, the tray drop and packing drop test were conducted to provide a close resemblance to real shipping and handling conditions to predict the missing ball rate. At the board level, board mounting reflow study was performed to check the manufacturability of both alloys. The PCB board Cu dissolution rate was evaluated under high temperature stressing. Air temperature cycling and mechanical bending test were carried out to evaluate the solder joint reliability. Microstructure analysis by SEM/EDX was performed to compare the morphology and composition of the intermetallic layers as well as the bulk solder.

The SnAgCu alloy was recommended by iNEMI and JEITA for BGA spheres. However, the frequent occurrence of brittle IMC fracture and resulting high missing ball failure rate of SnAgCu on Ni/Au pad has raised serious reliability concerns. The result of this study shows that SnAg can reduce the missing ball yield loss by at least an order of magnitude while maintaining the same level of manufacturability and solder joint reliability. Therefore, it is a viable candidate to replace the SnAgCu alloy.

5A.3 Tin Whisker Growth Evaluation on Solder Joint

Hiroshi Yamashita, NEC Electronics

Substitution of Sn-Pb on electronic assemblies with lead free has proven to be much more difficult than expected. And one of the main issues is whisker growth from Tin based alloys, because the alloys have the nature of the whisker growth. NEC Electronics therefore has adopted Ni/Pd/Au as one of our whisker-free terminal finishes. In this paper, we report the study of Tin whisker growth on assembled modules in combination with Ni/Pd/Au terminal finish and several SAC305 solders under the high temperature / high humidity condition. From our study results, whiskers appear to be dependent on the solder paste more than the monolithic terminal finishes, and these results indicate that we should consider all Tin based materials on the board for the solution of whisker growth.

Session 6: Zero Defects (Part 2)
Wednesday, May 7
9:15 am - 10:05 am

6A.1 In-Situ Process Variation and Outlier Reduction

Kuotung Cheng, TSMC

The automotive electronics industry is striving for zero defects in product reliability. Every step in the supply chain must consider ways to improve controllability, reduce variability, identify outliers, remove defects and ensure that the product meets the industry's zero-defect requirement. Traditional methods include test screening (test coverage, tri-temperature tests, burn-in, etc.) and statistical screening (PAT, SYL, SBL, etc.) All these measures are taken after the wafer process, and it has been proven that sub-one ppm level can be achieved. How to make further improvement? This presentation reviews an approach to reduce process variation and minimize outliers while wafers are still being manufactured. It presents a service package that is offered to customers who need to ensure a higher level of reliability for their products with the goal being zero defects.

6A.2 Zero Defects Implementation-Holistic Approach in a Manufacturing Environment

Ruby Clark, Freescale

"Zero Defects" has become an integral part of manufacturing organizations providing parts for the automotive industry. Defect reduction/prevention and preventing the reoccurrence of defects have been an integral part of a "Zero Defects" approach to manufacturing. Success is achieved only when the entire organization meets the requirements of a "Zero Defects" environment.

In this presentation I will describe and illustrate how the Manufacturing Organization of Freescale Semiconductor's Chandler Wafer Fab facility has integrated a "Zero Defects" mindset throughout the entire manufacturing facility. I will illustrate how "Zero Defects" is approached holistically with an emphasis on a systems approach, not a program approach. The presentation will cover how "Zero Defects" is integrated into every aspect of the organization, from planning to final testing. At the end of the presentation, attendees will have the basic understanding of how "Zero Defects" has been integrated into a manufacturing facility and has helped to improve quality.

Session 7: Zero Defects (Part 3)
Wednesday, May 7
10:25 am - 11:15 am

7A.1 Analysis of Wafer Bin Map Patterns for Lonely Die for Reduction of Customer Returns

Dileepan Narayanan, Cypress

The purpose of this study is to determine if application of 'Lonely Die' algorithms on wafer bin maps can screen latent defects and reduce customer returns. A 'Lonely Die' can be understood as a single 'good' (passing) die in a cluster of repaired / failing dice in a wafer. The idea is to determine if a cluster pattern of 'bad' (failing) dice in an area can predict dice with a high probability of ending up as customer returns. Identifying defect patterns in a wafer provide hints to process / tool problems and facilitate easier root cause identification. An algorithm was developed that compared X-Y coordinates of customer returns on a specific device with corresponding wafer bin maps to determine if the returns were 'Lonely Die'. The study showed that our algorithm could screen out up to 91% of the returns analyzed (a 10x improvement in PPM) for a yield impact of 5%. This work helps contain customer returns, while enabling analysis of future burn-in / reliability / EFR data for 'Lonely Die'. This study is expected to help progress towards zero defects for automotive products, drive down PPM levels for commercial products and improve quality across the board.

7A.2 Zero Defects Launch Approach

James Williams, Texas Instruments

In the Automotive industry, the Quality and Reliability requirements continue to be lowered. The entire module sold by our customers has a total Dppm of < 10, which translates to no fails from their suppliers. Zero Defect Launch (ZDL) is the name of the TI method to support this requirement. ZDL approach is to look at the overall flow that creates (design, fab, assembly & test) a device and how our customers use the product. Zero Defect Launch has a double impact of a mindset change and zero fails at the customer. The mindset change affects everyone that comes in contact with a device from conception through delivery of the final product. Requires each person to look at their job and ask would I want to spend my money for the final product? If the answer is no, then what can I do to improve the quality/reliability of my process. This may include taking ownership of a process tool, a tester, or even a test program that will insure the best product is created. If not, then do not continue to process.

Zero fails at a customer is a hard concept to put your arms around. It can be done, if you clearly understand how the product is designed into the applications and how it will be used by the customer. It will require implementation of best practices for reliability, design, manufacturing, test, and working with the customer. There must be an open data sharing as to how the system/device is tested at the supplier & the customer line (voltage, frequency, temperatures, unique algorithms, etc.). There will be times that a product needs to be released before it is ready, but once again ask yourself 'would I spend my money for this product?'. If you can not answer Yes, then do not release. Remember best practices can be planned without a delay in product release.

In summary, Zero Defects is required by our customers to engage in new business opportunities, which will require a mindset change of each individual and zero fails at our customers. It must be approached with a "can do attitude", which will eliminate our customers from removing our defects. This approach has been proven to work based upon Dppm reported by our customers.

Session 8: Packaging Issues
Wednesday, May 7
11:15 am - 12:30 pm

8A.1 Characterization of BGA Warpage in Simulated Solder Reflow

Mike Varnau, Delphi Corporation

BGA (Ball Grid Array) IC packages are being widely used as the IC package of choice for pin counts greater than 176 leads. However, this package is highly asymmetric and undergoes significant warpage during the solder reflow assembly process. In the worst case, some of the BGA solder balls lift out of the solder paste before solder liquidus, and then the BGA flattens out after solder solidus and presses the solder ball into the soft solder deposit from the reflowed paste creating an apparently good solder joint. This mechanical solder joint can easily pass electrical testing in the factory, but will fail very quickly in the field. This paper provides a statistical summarization of thermal warpage characterization of 3 different BGA constructions versus storage environment and reflow profiles. It also compares the BGA warpage against the competing circuit board warpage for an estimate of the probability of occurrence.

8A.2 A Study on the Relationship between Epoxy Fillet Height and Device Performance in Function and Reliability

Galen Lin, Integrated Silicon Solution Inc. (ISSI)

Silver epoxy is used mainly for die attachment in many types of SMT IC packages. It also serves as a medium which provides better thermal dissipation and stress buffer between IC and surrounding molding compound. In the IC assembly industry, an epoxy fillet height of less than 75% (as measured against the IC chip height) has been generally required as specified in manufacturing specification. It seems, however, no study on the relationship between the epoxy fillet height and device performance in function and reliability has been reported. In this investigation, three splits of ICs (for 4M SRAM, 100 pin LQFP) with different epoxy fillet heights at 60~75%, 100% and epoxy overflow (limited to die surface coverage within the scribe line) are used in an attempt to provide this missing information. Assembled units in the splits are undergone through IR reflow and TCT before comparing their performance in function and reliability. Splits with epoxy fillet height at 100% and epoxy overflow are found to induce shear stress easily on the die surface, resulting in a 25% failure rate with package de-lamination after IR reflow and TCT. The de-lamination can lead to die surface crack and device functional failure, as seen from the products field returns, which is actually the reason of initiating this investigation. For the split with 60~75% epoxy fillet height, the die side-wall can block the shear stress from extending into the die surface, and thus no de-lamination has been seen. The industrial specification of less than 75% epoxy fillet height is thus confirmed and justified.

8A.3 Impact of Mold compound Filler Particles on Local Thermomechanical Stress Variations

Daniel Vanderstraeten, ON Semiconductor

Thermo-mechanical package-induced stress is known to affect the electrical and mechanical performance of IC's and is well understood and documented by the industry. The study of the impact of different sized filler particles coming from the mold compound giving very local stress variations is new. This abstract wants to give a view of the work that has be done on the topic. Molding compounds are mainly consisting out inert fillers particles. These filler particles are in mold compounds silica (SiO2) spheres with a size ranging typically between 0.5 to 150 micrometers. The variation in filler size is influencing significantly the local stress on top of silicon as explained here after. When a large silica particle is present in the vicinity of the die surface, the local stress in the silicon can show a pronounced stress peak due to the mismatch in thermal expansion coefficient (CTE). This is due to the stiffness and size of the particle with respect to its surrounding particles.

A simulation model was build using the assumption that one large particle is surrounded by similar sized smaller ones. Simulations at different temperatures (-40, 25 and 260°C) and different particle sizes were done to see the impact of the local stress variations. They are revealing that the local thermo mechanical stress variation can be significant due to filler size variation. The stress variations can go in to the range from 4MPa to 90MPa in the vertical direction depending on the filler size and stress temperature, not location on the IC surface. The calculated mechanical stress values can be double of what is found in the older thermo-mechanical stress models using an even distribution of material of the IC surface. As these variations can influence the electrical analogue parameters counter measures are evaluated. Mold compound with a more even smaller filler size and polyimide coating are the ones checked. Both are giving an improvement but further evaluations need to be done to see the gain. The results of both will be discussed during the workshop.

Session 9: Failure Analysis
Wednesday, May 7
2:00 pm - 3:40 pm

9A.1 Failure Analysis Techniques for Marginal Semiconductor Devices

Eric Bedes, NEC Electronics America

When performing failure analysis on marginal semiconductor devices, the typical analysis techniques used for hard failures such as Photon Emission and IR-OBIRCH may become ineffective. Hard fail devices are typically analyzed by initializing the device into a static fail condition and then performing the failure analysis. With a marginal device, holding a static fail condition is often very difficult to achieve and different analysis techniques are required for successful fault localization. OBELISCH analysis, Dynamic Emission, and FIB Circuit Modification are several techniques that are very effective for analyzing marginal failures. High-speed failures and function failures due to long transient response times are problems that typically must be analyzed dynamically. Choosing the best analysis technique will often depend on the results of several candidacy checks such as IDDq, Shmoo, and Temperature analysis. These candidacy checks can provide subtle clues to help determine the nature of the fail mechanism and the best analysis technique to complete the fault localization.

9A.2 RF Impedance Analysis for Reliability Monitoring

Michael Azarian, University of Maryland (CALCE)

Accompanying the growing use of microprocessors and signal processors in vehicles has come the need to reliably transmit signals having frequencies of several hundred megahertz or more across interconnects and cables. At these frequencies, signal propagation is concentrated at the surface of the conduction path, a phenomenon known as the skin effect. Degradation of interconnects and conductors, such as cracking of solder joints due to fatigue or shock loading, also usually initiates at the surface and propagates inward, making the performance of high speed electronics increasingly sensitive to small cracks or corrosion, or damage to insulation in wiring harnesses.

This paper describes the use of RF impedance measurements as an early indicator of physical degradation of electronic systems. Simultaneous measurements were performed of RF impedance and DC resistance while an electronic component was stressed. The RF impedance was observed to increase in response to the physical degradation while DC resistance remained constant. Failure analysis revealed that the RF impedance increase resulted from a partial crack in a solder joint. This approach provides a means for monitoring degradation in electronic assemblies and wiring, as well as identifying potential failures prior to their occurrence.

9A.3 Fast Fault Diagnosis for Analog IC's

Yizi Xing, NXP Semiconductors

Automotive industry demands on fast failure analysis of field returns. However, failure analysis (FA) is everything except easy for a complex analog IC, especially when the failure mode is expected to be diffusion-process related. The throughput time is long and costs are high. For an FA engineer, most of all, it is a lot of manual work. It is well known that fault diagnosis (FD) using Automatic Test-Pattern Generation (ATPG) tools can help to speedup failure analysis to a great extent. But in the world of analog, nothing comparable exists. Only limited investigations have been done in the academic world. No application on real life silicon has been reported so far.

In this presentation, the method and results of fault diagnosis based on fault simulation for analog ICs will be explained. The methodology of analog fault simulation has been initially used for test development, test coverage estimation and defect screening. Now we will demonstrate, by using an IC in mass production, that analog fault simulation can also be used successfully for fault diagnosis. The method uses a database obtained for this IC by extensive simulation of extracted faults from its layout against the production test program. The FA results of the field returns of the IC over the past 3 years are used for validation. The outcome shows very good match. Analysis of the data and further improvements will be given.

9A.4 FIB Assisted EMI and OBIRCH Analysis

Michael Wieberneit, NEC Electronics Europe GmbH

The most common failure analysis (FA) techniques for fault location besides electrical testing are emission microscopy analysis (EMI) and OBIRCH analysis, which are well known standard methods in today's FA flows. Abnormal EMI or OBIRCH spots may be obtained by comparison between a known good device and the device under test (DUT) at same electrical stimulation. With increasing device integration density and complexity, the EMI and OBIRCH response become more complex and does not allow in any case to pinpoint directly to the defect site.

This paper address one worst case scenario of complex EMI and OBIRCH response, in which all spots are connected to only one failing net. For the defect location additional analysis is required considering both the layout and electrical conditions of the failing net. Examples will show strategies for FIB modification in order to drive the failing net in different electrical condition leading to a simple EMI and OBIRCH response which allows a clear estimation of the true defect site. FIB assisted defect location can be a powerful approach for a complex EMI and OBIRCH response. In many cases we could demonstrate that just one modification step is required to get a simple EMI and OBIRCH response pinpointing the defect site. This approach increases the failure analysis success rate based on EMI and OBIRCH techniques.

Session 10: Electrostatic Discharge
Wednesday, May 7
4:00 pm - 5:50 pm

10A.1 Comparison of JEDEC and Q100 Standards and New Q100 ESD-CDM Calibration Issues

Michal Polewski, NXP Semiconductors

In the past two years CDM-ESD testing took important place in the IC qualification program. As the number of products that require CDM verification increases significantly it is important to find the methods that reduce the qualification effort (number of tests). Building up this knowledge would allow to minimize the ESD-CDM measurements costs and to shorten the time-to-market as well. Comparing the JEDEC JESD22-C101C and AEC-Q100-011B standards and using the more severe one brings the substantial reduction in number of qualification tests. Furthermore, also calibration aspects play an important role.

Comparison of the JEDEC and Q100 standards for ESD-CDM testing will be presented, based on measurements results. New software has been developed to capture discharge current waveforms. It will be shown that the AEC-Q100-011B represents the worst-case CDM test condition, because the first discharge peak current is 10 to 30% higher than in JEDEC JESD22-C101C. Therefore, AEC-Q100-011B is recommended for cases when qualification of the device should fulfill both consumer and automotive market requirements.

For qualification tests it is also very important to minimize the calibration risk and to detect the changes in measurement setup at early stage. It was noticed that the standard ESD-CDM Q100 calibration procedure does not cover the cases that may come from CDM measurements practice. Differences in the ESD-CDM discharge current peaks due to e.g. change of dielectric foil parameters are observed during qualification stresses. The performed measurements showed 20% difference in first discharge current peak. It was also found that marking the chips with a pen could impact the discharge current waveform. Additional calibration steps are proposed to improve the ESD-CDM measurements in practice.

10A.2 The Significance of the Machine Model to the ESD Qualification of Integrated Circuits

K.T. Kaschani, Atmel

Abstract not available at time of publication

10A.3 Proposal for the Reduction of ESD Compliance Levels (Audience Participation)

Charvaka Duvurry (et al), Texas Instruments

The automotive industry continuously strives to achieve 'zero defects' from electronic products and in this pursuit the ESD specifications for IC components play an important role. While good ESD levels are critical and always important, there have not been any detailed studies that clearly establish what the true relevant automotive industry requirements should be. For example, do the automotive ICs face a different set of conditions in production lines? Are these conditions relatively harsher than for standard IC production lines? Do IC chips in automotive application systems see larger residual voltages than in other PCB systems? Does the ESD design window affect the automotive IC designs also? Are there any case studies that establish increased failure rates for automotive applications when the component level HBM is reduced to below 2kV? This panel invites open public discussions from the AEC members to examine the published data and recommendations from the Industry Council on ESD Target Levels in terms of the automotive environment. The final purpose of this workshop is to arrive at realistic and safe ESD levels that are commensurate with safe handling and are compatible with the practical ESD design limits. This strategy is critical for the IC customer/supplier interactions in the near future.

Session 11: Qualification Issues
Thursday, May 8
8:00 am – 10:05 am

11A.1 Comprehensive Requirements and Qualifications of Die Fabrication Reliability - Technology Platforms of 0.8mm to 45nm and Beyond for Automotive Applications

An-Chi Kang, TSMC

AEC-Q100 has clearly defined the automotive product qualification including stress items, stress conditions, sample size, acceptance criteria and so on. However, there is no industry standard for automotive process qualification (or intrinsic reliability, die fabrication reliability). Although intrinsic reliability stress items have been defined in AEC-Q100, detailed requirements such as stress conditions, test methodology, and acceptance criteria are not defined yet but just stated that test methods, calculations, and criteria should be available to the user upon request.

This presentation qualitatively and quantitatively explains specification requirements of intrinsic reliability including temperature definition from the viewpoints of mission profile and physico-mechanisms, failure rate requirements and relations to in-line process control, and DC life time requirements. The feature parameters of each stress item for all kinds of components such as MOSFET for advanced CMOS technologies, LDMOS for high voltage technologies, BJT, MIM capacitor for RF, mixed-mode technologies and so on across all generations are discussed and defined to determine the intrinsic life time. The calculation methodologies and acceptance criteria are included. The major technical issues for nanometer technologies and beyond of automotive grade are also discussed. Intrinsic reliability from micron to nano-meter generations of various technologies are finally consolidated to show automotive-grade availability as the technology platforms for automotive product manufacturing.

11A.2 Reliability Integration and Assurance in Manufacturing Process Transfer

Mike Wang, NEC Electronics

NEC Electronics has established a stable supply chain for automotive MCU products according to NEC's Multi-FabTM strategy. Following this strategy, NECEL had planned to transfer 0.15um embedded flash process from Japan fab to Roseville, California fab. Process transferring increases supply capability to satisfy US and EU customers' demands. On releasing our upcoming fab line, it is important to examine not only devices' functionality and electrical characteristics, but reliability properties as well. Ensuring Roseville device's reliability performance to match that from Japan is essential to fulfill both supply requirement and execution of Zero Defect program.

NEC has continuous activity to achieve built-in reliability in manufacturing stage by systematic assessment of device level reliability characteristics. Upon process qualification of Roseville fab, we tried to conduct efficient evaluation planning based on FMEA methodology specifically designed for reliability evaluation. Key process parameters affect reliability are extracted by in-depth parameter comparison between Roseville and Japan fabs. For most influential manufacturing parameters that impacts reliability, thorough experiment designed to determine device's physical degradation mechanism and valid process control range was performed. Our desire is to realize equivalent device reliability in fab process transfer. Our approach and actual experience of reliability improvement are explained in this presentation.

11A.3 Knowledge Based Qualification at NXP: Know the Failures to Guarantee NO Failures

Paul Ngan, NXP Semiconductors

A New Qualification Strategy is being implemented at NXP, to address the ever-increasing challenges in technological complexity as well as the pursuit of better and better quality and reliability (e.g. zero defects). It is called Knowledge Based Qualification Methodology (KBQ).

The Knowledge Based Qualification aims to understand the reliability capability (and hence the boundary) of each of the building blocks (process, IP/library and package/assembly and their interactions) with respect to a particular application area. The reliability knowledge generated from those building blocks will be used to update reliability design rules and models for future uses. For product qualification, the concept of mission profile is utilized to calculate the equivalent stress time in order to demonstrate the equivalent reliability. Structural Similarity data is used to construct the most optimal qualification plan.

The approach avoids many drawbacks of "cookie-cutter" qualification approach (one size fits all) (For example, running HTOL 1000h regardless) and allows application specific qualification. The strength and (potential) weakness of KBQ will be discussed and contrasted with standard Stress Driven Qualification.

11A.4 Reliability Enhancement by Suppression of Nano-Dendritic Defects in MIM Capacitors in Integrated Circuits

Lieyi Sheng, ON Semiconductor

Mixed-signal automotive integrated circuits require high voltage capability, high temperature operation, high reliability (0ppm) as well as low cost. One of the key components of a mixed-signal device is integrated linear capacitors. Metal-insulator-metal (MIM) capacitors with silicon nitride (Si_3N_4) as the dielectric are integrated into the AlCu backend of ON's 80V mixed-signal process. Although sufficient for many other applications, a single-digital ppm failure rate of MIM capacitors was not acceptable for automotive products.

A comprehensive failure analysis procedure nondestructively revealed for the first time the TiN nano-dendrite defect growing from a 10-nm-diameter aluminum whisker. From the unique features of the defect appearance as well as the interactions with its surrounding, we concluded that an Al whisker from the bottom Al surface was the defect origin.

This failure origin clearly suggested the importance of optimizing the bottom aluminum process module to prevent whisker occurrence. The enabled process has remarkably reduced reliability risks by suppressing the defectivity by a factor of 40. This reduced product wear-out returns from dozens-of-ppm to sub-ppm levels.

11A.5 Defect Detection With Cold Testing in Automotive Qualification

Kirsten Roedle, NXP Semiconductors

For automotive qualification of Integrated Circuits (ICs), AEC-Q100 requires electrical testing at cold, ambient and hot temperature after High Temperature Operating Life test (HTOL). After Early Life Failure Rate test (ELFR) and Burn-in in production, electrical testing is done at ambient and hot temperature. HTOL is a test simulating the IC life cycle while accelerating the IC degradation during application. This test is typically executed on a small amount of samples, but for an extended period of time to explore wear out mechanisms. In contrast, ELFR is performed on a large amount of samples for a short time to provoke early life time failures.

During the HTOL qualification of a Car Radio IC, all stressed samples did pass electrical testing at ambient and hot temperature, but one sample failed at an intermediate readpoint at cold temperature. No parameter shift was detected at hot and ambient. If a new failure mechanism has been detected, then cold testing after ELFR and burn-in might be necessary.

Failure analysis (resistive interconnect localization followed by cross sectioning) revealed that the root cause of this ROMBIST-failure (BIST = BUILT-In Self Test) was a particle, located between metal1 and metal2 in 0.16µm CMOS-Flash technology. This was not detected at inline QA (Quality Assurance) inspection or at 0hr cold testing, but only after operational life at cold testing. On another circuit location, this particle may have revealed completely different temperature related behavior.

To summarize, an Early Life Failure was observed by cold testing. Failure analysis showed that a particle caused the defect. Cold testing is too expensive to apply in production, e.g., after Burn-in. Instead, an improved particle screening in the diffusion was implemented in order to achieve zero defects.

Session 12: Test & Statistics
Thursday, May 7
10:25 am - 11:40 am

12A.1 Why Statistical Bin Limits Fail

Tim Haifley, Altera Corporation

This presentation introduces a modification of the AEC standard bin limit method, AEC-Q002, when applied to large complex semiconductors. The AEC test method depends heavily upon the normality assumption which usually fails due to known fundamental issues in semiconductor production. The AEC method says that we estimate a fixed but unknown bin failure rate and that we sample from a very large population distribution. This presentation introduces a method to rescale bin results so that the normality assumption can be applied. This presentation introduces the concept that the bin failure rate being estimated may, in fact, be a random variable rather than a fixed but unknown value.

12A.2 Embedded Multi-Detect ATPG and Its Effect on the Detection of Unknown Defects

Erik Marinissen, NXP Semiconductors

There is a constant drive to improve test quality and reduce test escape rates. A test approach that enhances test quality is the so-called *multi-detect test*. In such a test, faults from known fault models are targeted multiple times by different test patterns, in an attempt to achieve fortuitous detects of other, so far unknown and unmodeled, defects. Multi-detect stuck-at tests share some of their attractive benefits with regular single-detect stuck-at tests: test generation requires a gate-level netlist only, and a failing test proves a faulty IC. However, a conventional multi-detect test, i.e., the *n*-detect test, does not come for free; its size grows linear with the value of *n*.

In this paper we present an Automatic Test Pattern Generation (ATPG) method for embedded multi-detect which exploits the abundantly available don't care bits in test patterns. When combined with traditional single-detect ATPG, our EMD(*m*) approach tries to embed up to *m* detections of each fault in the regular patterns, without requiring additional patterns. Both simulation and high-volume silicon measurements show that this approach is indeed effective in catching other, so-far unknown and unmodeled defects. When combined with conventional *n*-detect ATPG, our EMD(*n,m*) approach (for $n<m$) reaches even better results.

12A.3 To Bayes or Not to Bayes: ELFR (or How to Sharpen Those Limits)

Tim Haifley, Altera Corporation

This presentation introduces Bayes methods to augment zero defect sample plans traditionally employed in reliability tests. The zero defect sampling requirements of AEC-Q100 are based upon sampling (frequency) theory. This says that we estimate a fixed but unknown failure rate (PPM failure for ELFR or FIT rate in LFR) and that we sample from a very large population distribution. If we observe zero defects, then we rely upon confidence limits to estimate that failure rate. This presentation introduces the concept that the failure rate being estimated may, in fact, be a random variable rather than a fixed but unknown value. Issues of traditional sampling theory estimation and the improvement of those estimates using Bayes probability limits are discussed.

Session 13: NVM & Memory Issues
Thursday, May 7
11:40 am - 12:55 pm

13A.1 Non-volatile Embedded Memory Solutions for Automotive Products

Chin-Piao Chang, TSMC

Among various designs of flash memory, the split-gate flash outperforms the stack-gate flash in parallel programming capability, lower power consumption, better array efficiency, higher speed flexibility, and highly compatible process with CMOS technology platform. Therefore, the split-gate flash is more suitable as the embedded solutions for system-on-chip design.

In this presentation, the product advantages like low power, high speed and reliability benefits like data retention of the split-gate embedded flash IP on mainstream technology platforms are shown. The reliability certification contents for automotive applications are introduced including flash IP design parameters with cycling evolution, endurance life time with dppm failure rate across temperatures, disturb immunity versus cycling, and data retention capability. Then the qualification flow of flash IP toward automotive quality are also shown including effective burn-in and screening. The manufacturing learning of commercial-grade embedded flash IP in advance of automotive product provides “technology burn-in” (IP design and process) in time and volume and leads to zero ppm requirement of automotive quality. The major technical issues with technology shrinkage up to 90nm are explained. In addition to the embedded flash IP, the OTP (One Time Programming) solutions for automotive product is also presented from IP characteristics to qualification flow

13A.2 Designing Safety Critical Systems for Neutron and Alpha Particle Single Event Effects Failures

Terry Pence, Actel Corporation

Line widths used for manufacturing semiconductors continue their relentless downward trends, while circuit complexities and clock speeds increase. The benefits of this trend for the system designer are increased functionality and capability at a lower unit cost. But what underlying issues may impact safety critical system designs? What are the new challenges in device reliability in regards to ground level radiation?

Today’s designer needs to understand the potential impact of radiation effects, what kind of test data to ask for and how to interrupt what they are given. Faced with an ever increasing choice of technology and products classes (FPGA's, ASSP's, ASICS's), which do you choose in order to optimize your design for safety, reliability and fault tolerance? This paper presents recent Neutron particle test results and analysis, the projected impact on automotive electronic systems and the various techniques, some adapted from the space community, which can be used to address increased reliability of safety critical systems. While it appears the low hanging fruit for improved automotive reliability has already been picked, new technology introduction requires careful analysis and part selection for applications where failure just is not an option.

13A.3 Thermal Acceleration Factors for Qualification of Trapping-Based NVM Products with Cycling Bake Intervals

M. Janai (et al), Spansion

A tutorial is provided on the physical aspects of localized trapping-based NVM's affecting qualification cycling and data retention methodology, and linking to applicable JEDEC standards/specifications. Experimental data are presented characterizing and comparing relaxation effects on electrons and holes under various cycling, cycling rate, and relaxation bake scenarios, and comparing “laboratory” to “user-mode” cycling. Discussion and analysis are provided, with conclusions/recommendations drawn from the experimental data. A listing of applicable references/citations is provided (“recommended reading” for further technical detail). And also, a supplement is provided outlining industry participation and leadership in the JEDEC Non-Volatile Reliability Task Group (JSC14.3TGNVMR, 2005-2008).