

Session 1A: Passive/Electro-Mechanical Issues (Part 1)

Tuesday, May 22

8:20 am – 10:00 am

Two Rivers Room

1A.1 Quartz Crystal – Reliability and Application

Arthur Lee, Hong Kong Automotive XTALS Ltd.

Quartz Crystal is a piezoelectric device, and is a key component of the oscillating circuit. Many people will think Quartz crystal is the first component production engineers will replace when they have a failure board; and it is a component that purchasing people will hardly find a reliable vendor; yet to many design engineers it is a mysterious little black box. This application note will discuss how to specify a quartz crystal from the application circuit characteristics and the reliability aspects. The application circuit characteristics aspect will cover negative resistance and Max ESR, Definition of Drive Level, Load Capacitance, various electrical parameters, error budget for frequency tolerance. The Reliability aspects will cover Sleeping Crystal and DLD, Shock, Vibration from TPMS application point of view, Spurious specification as well as Temperature Cycle characteristics.

1A.2 Ferrite Components: Reliability of Performance Under Load

Jeff Bruce, Steward

Ferrite cores, chip beads and components are widely used in automotive electronics to filter unwanted high frequency noise from both control and power circuits. For a wide range of automotive applications, ferrites have proven to be reliable and dependable and consistently up to the task in meeting harsh, demanding AEC test requirements and standards. One issue of reliability that is often overlooked by circuit designers is the drastic change in performance of ferrite chip beads in the presence of DC bias current. The impedance provided by a "600 ohm" chip bead can decrease by 70% or more in the presence of significant bias current. Accurate Spice models can be a valuable tool to predict the function of passive components in active circuits. However, if the performance of a passive device, like a ferrite chip bead, changes as current increases, then a Spice model based on "no load" performance is misleading, and therefore of little value. This presentation will illustrate the instability of ferrite chip beads under bias and demonstrate the value of dynamic Spice models that can accurately predict chip bead performance under changing load conditions. Alternative solutions will be discussed for those applications where chip bead performance is questionable.

1A.3 MLCC ESD Performance Findings

Ron Demcko, AVX

Electronic systems are increasingly portable and miniature as a result of integrated circuits scaling downward, power sources become more efficient/miniature and system I/O methods shrinking. As a result systems that have never been exposed to harsh environments and harsh transient voltage requirements are now seeing a variety of difficult applications. Additionally, cost pressures on circuitry in need of very low levels of electromagnetic event protection dictate the use of low cost solutions to voltage swings in consumer circuitry. This paper will concentrate on characterizing the transient performance of a variety of multilayer ceramic capacitors in different case size, dielectric and manufacturer. Tests were performed in a non-industry manner to induct failures into good devices and determine a worst-case performance scenario. These tests were aimed to parallel worst case brute testing seen at several customer sites. That is, an increasing number of end users do pass/fail system testing on end systems with 10 positive ESD pulses followed by 10 negative ESD pulses. These customers would like to get a rough idea of capacitor capability prior to completing a design. Optimized design capacitors will be presented and capacitor effect on ESD voltages will be discussed.

1A.4 Electrostatic Discharge Damages in Multilayer Ceramic Capacitors (MLCC's) and their Relation to MLCC Design-Rules

Engel Guenter, EPCOS

We present the results of investigations about the damage thresholds and the typical failure modes in low capacitance (1nF – 10nF) MLCC with various rated voltage levels (50V – 200V) and with different technologies (NME: noble metal inner electrode and BME: base metal inner electrode). The ESD strikes applied are according to IEC1000-4-2 but with voltage levels between 2KV – 25KV adapted such that electrical value deterioration and damages inside the MLCC is kept to the possible minimum. The results show that the capacitance value is critical to the damage threshold, as well as the voltage rating. The cross sections typically show discharge channels, but also further cracking which easily could be (and most probably was often in the past) misinterpreted as thermal shock crack. It is also shown, that MLCC's designed with NME (noble metal inner electrode-) technology show much more robust ESD behaviour compared to BME (base metal inner electrode) – technology with the same capacitance value. The results are also discussed in relation to bias dependence of MLCCs. We conclude that besides the recommendation design rule to use Varistors, either Cap-values $\geq 22\text{nF}$ are necessary to avoid ESD troubles, or, in applications where 10nF is the maximum capacitance value, NME-based MLCCs with specified ESD rating are to be used.

Session 1B: Discrete Semiconductor Issues (Part 1)

Tuesday, May 22

8:20 am – 10:00 am

Tulip Grove Ballroom

1B.1 A “Good” Automotive Power MOSFET Switch

Krishna Shenai, PhD, Utah State University

To cope with rapid advances in semiconductor technology and customers' expectations toward performance and reliability, it is necessary to identify defect lots earlier in the production lines. One of the major causes for field-failure of DC-DC power converters is the failure of power MOSFET's. Choosing power devices for converter applications has been largely based on selecting the optimum voltage and current ratings and the lowest on-state resistance devices to reduce heating. Blocking state leakage current limit of power MOSFET's has never been a criterion with designers. In this paper we show that careful screening of power MOSFET's for leakage current can have a significant impact on the reliability of devices and hence, on the field-reliability of the DC-DC power converter itself. For technologically advanced applications such as power supplies for high-end servers and automotive electronics, it is essential that only the best power MOSFET's are used to prevent failures, improve field-reliability, and reduce manufacturing and operating costs.

The time between failures is a very useful measurement to analyze reliability models for time-dependent operation of systems in the field. In many cases, the failure-generation process is assumed to be stationary, even though the process changes its statistics as time elapses. This paper analyses the reasons for failure of power MOSFET's in the useful life period of the device and based on a Weibull analysis estimates the reliability of the devices and the probability of failures. The analytical model results are validated using field-failure data collected from a range of computer power supplies operating under typical field conditions.

It is found that careful screening of power MOSFET devices for low levels of leakage current enhances the reliability of single switch active clamp DC-DC converters. This may be true for other topologies as well. A statistical model based on the Process Capability Index (Cpk) is proposed which offers designers a convenient way to include the best devices in their converters. Also proposed is a method of estimating the reliable life for a power MOSFET device based on failure rates estimated by the Weibull probability distribution functions. The results have been partly verified with field-failure figures dropping dramatically for DC-DC converters consisting of “good” power MOSFET's.

1B.2 Q101-Inspired Validation of Custom Power Modules

Jack Marcinkowski, International Rectifier

AEC Q101 has provided an aggressive set of standardized tests for discrete power semiconductors for use in demanding automotive applications. Some applications require performance (e.g. current level or Rth) or form-factors which cannot be achieved by standard discrete packages. These applications are usually satisfied using custom designed power modules. Many of these custom module designs do not use the same encapsulation methods (e.g. transfer molding of thermoset plastic) and assembly processes commonly used in standard packages. These custom modules still need to meet aggressive automotive type reliability and validation requirements. However, they may not easily fall into the standard battery of Q101 tests, and as they are application specific, generally must meet a specific customer specification including reliability requirements.

This presentation discusses our experience with validation testing of such modules as we attempted to design a reliability/qualification program utilizing Q101 as a guideline in addition to the customer specified testing. We provide a comparison of a typical module validation plan versus Q101. We highlight some specific incompatibilities between AEC-Q101 and module testing, and discuss our approach to these issues. We discuss our use of Q101-style tests as a HALT test where the application conditions are known to be less stringent than the Q101 requirements

1B.3 Field-Reliability of an Automotive Switch – a New Paradigm

Krishna Shenai, PhD, Utah State University

Traditional approaches to evaluating power semiconductor field-reliability do not account for system-level dynamic electro-thermal stresses. Paradigm shifts in accelerated stress-testing methodologies and field-reliability modeling are needed to develop next-generation of power semiconductors for value-driven consumer and mission critical military/space applications including automotive and aerospace systems.

We report on the results obtained from an extensive study of the field-reliability of compact power supplies based on a novel system-driven “top-down” approach in which electrical and thermal stresses are evaluated under dynamic long-term switching conditions. It is explicitly shown (experimental and theoretical) that dynamic charge exchange between reactive components (inductors and capacitors) and power semiconductor switch critically determines the long-term field-reliability of a power system. A number of accelerated stress-testing techniques are proposed and evaluated to optimize this phenomenon that include new specifications for avalanche rating, leakage current, single-electron burnout, and package layout.

We report, for the first time, an integrated system-driven approach that combines advanced computer simulation

and accelerated stress-testing to develop component and system specifications for improved and predictable design of an automotive power switch with “built-in” field-reliability. The overall expected impact is an increase by an order of magnitude in the mean-time-between-failures (MTBF’s).

1B.4 Life Time Prediction of Smart Power Devices for Automotive Exterior Lighting Subjected to Nominal and Overload Conditions

Romeo Letor & Sebastiano Russo, STMicroelectronics

System design for zero failure requires defining a risk assessment to take into account all potential parametric variations. In our specific case, the choice of a lamp driver will be performed on the basis of its resulting reliability in terms of number of activations versus all parameters variations (battery voltage, ambient temperature, etc.....). This criterion is valid both for nominal operating condition and for overload conditions. A minimum life time will be required in nominal operating conditions while a software strategy defining a maximum number of activation in overload to handle the fault will be required to prevent catastrophic failures in overload conditions.

For this purpose the concept of mission profile is a powerful method to predict the life time of a smart Power operating in a given system. In general the mission profile is not available but in this specific case the mission profile can be extracted by means of a detailed simulation of the device interaction with the system. On top the application of this method requires a full comprehension and characterization of the stresses applied to the device during operation in the system.

This presentation analyses in details the relation between the operating conditions and the stresses applied to the smart Power driving automotive bulbs: The inrush current of the lamp creates a fast thermal transient on the driver. During this transient the heat cannot propagate deeply, so the thermal stress is confined to a very small layer of the silicon. Accordingly a specific characterization defines the correlation between the thermal transient and the resulting cumulated stress.

Beside this, the mission profile is influenced by the interaction of the smart power device protection with the electro thermal behavior of the lamp. Hence a detailed simulator was properly designed in order to take all parameters in account. (Example: Low current limitation, High battery voltage, lamp parameter variation, Low ambient temperature).

Two practical examples are illustrated comparing the simulation result with experimental results:

1. Reliability with nominal load
2. Reliability evaluation with overload.

Session 2A: Passive/Electro-Mechanical Issues (Part 2)

Tuesday, May 22
10:20 am – 12:00 noon
Two Rivers Room

2A.1 Flexure Robust Capacitors

Bill Sloka, KEMET

Board-flexure-related cracking has long been an issue with multilayer ceramic capacitors (MLCC), especially when larger case sizes (ca. 0603 and larger) are used. Careful circuit board design is needed in order to keep MLCC from areas of high flexure stress such as edges, large connectors, etc. Additionally, careful handling of boards during chip population and subsequent SMT processes is necessary in order to avoid board-flexure-related cracking. This paper discusses various aspects of board flexure as well as guidelines useful in avoiding board flexure related cracking. Several MLCC products that either reduce the incidence of flexure cracking, or fail open when cracked in the classic board flexure crack mode, or eliminate flexure cracking altogether are discussed in detail with respect to design philosophy, board flexure test performance, and other device performance parameters, as well as suggested application. Use of various design philosophies has resulted in a broad flexure robust product line that offers an optimal solution for most applications.

2A.2 Reliability of Passive/Active Components with “Safe Constructions” - Experience on Whisker Testing and Solderability

Reiner W. Kuehl, Vishay

Since our first discussion on “*Reliability of Lead-free Passive Components in View of Solder Processes and Quality*” at the 8th annual AEC Reliability Workshop in Kokomo/IN in autumn 2002 meanwhile the electronic component industry has switched more or less to Pb-free contact terminations. Experiences of more than four years of practice from field and testing are available today for evaluation.

Today there is a common sense in industry on the definition of: what Pb-free design(s) are reliable; what tests can be used in order to qualify a proper whisker mitigation of tin surface finishes; and what demands are important on solderability at the low and high peak temp limits. These basic points will be wrapped up. Typical reasons and influencing parameter on “failed” samples with “safe designs” of tin surface finish (mainly on passive components) will be shown, discussed, and evaluated in its relevance. Results of several thousands of whisker tests will be concluded. Correlations on whisker mitigation and solderability requirements and their influencing parameter will be shown.

2A.3 Flexisafe Ceramic Capacitors

Ron Demcko, AVX

Abstract not available at time of publication

2A.4 Conductive Polymer Technology

Jayson Young, KEMET

Conductive polymer capacitors continue to gain popularity throughout many industry segments as designers search for leading edge capacitor technologies to keep up with changing demands. This presentation will focus on the many advantages this technology has brought to the industry since its initial inception. Advantages such as high volumetric efficiency, capacitance retention at elevated temperature, improved frequency response and benign failure mode will be among some of the topics discussed. In addition, we will explore new developments in polymer technology and component design that will continue to expand this technology into applications previously associated with alternative component technologies.

Session 2B: Discrete Semiconductor Issues (Part 2)

Tuesday, May 22

10:20 am – 12:00 noon

Tulip Grove Ballroom

2B.1 Effect of Extremely Long Time of Hot Repetitive Short Circuit on Smart Power of Last Generation

Sebastiano Russo & Lucia Torrisi, STMicroelectronics

The technologies scaling in power devices and consequently the increasing of specific power level, together with the more aggressive reliability requirements – which must reproduce the worst condition at which the device may be submitted during the real life, like short-circuit – impose to examine the whole system “silicon die / package”; particularly what can be critical is the interface die / bonding wire. The packages shrinkage leads to consider - up to now - Au wires as the best choice, due to Au low resistivity and its ability to be reduced in dimension in order to bond on small areas. As well known, the main issue concerning Al / Au interface is the inter-metallic compounds growth. The present work shows the results of an extremely long period of “hot repetitive short-circuit” stress, applied to VI-Power devices of last technology generation using double level metal and passive pads on

2nd metal layer, and the physical evidence of a very big IMC formation without sensible electrical degradation.

2B.2 Effect of Post Mold Cure (PMC) on Semiconductor Device Reliability with Focus on Discrete Diodes and Transistors

Michael J. Varnau, Delphi

Post Mold Curing (PMC) of transfer molded plastic IC packages has been standard practice since the 1960s when plastic body IC packages became reliable enough for general industry acceptance. Recent advances in molding compound technology have led several manufacturers of discrete devices such as diodes and transistors to eliminate the PMC process as a means of cost reduction. This paper is a tutorial on the technology, and an assessment of potential reliability ramifications of eliminating PMC. Generally PMC is the preferred and default process. However, data indicates that in some cases performing PMC actually degrades the reliability of a device in a temperature cycling environment. The final conclusion is: There are multiple failure modes, and there are offsetting effects associated with eliminating PMC, that are design and application specific, which precludes making a broad based assertion on the suitability of eliminating PMC for discrete diodes and transistors.

2B.3 Reliability study of Die-on-Leadframe Technology for Automotive Applications

Michael Ohm, International Rectifier

In order to handle higher electrical power, e.g. for starter generator application, in automotive environments with cost and space restrictions Die-on-Leadframe technology was developed by International Rectifier to meet these requirements. Here, the power semiconductors, in this case MOSFETs, are bonded directly to the current rails of the module. This makes the use of expensive power substrate technology like DBC or IMS unnecessary. Die-on-Leadframe solves two of the most important design imperatives of power modules: current carrying capability and heat conduction/spreading. The automotive application which the study is based on is a water-cooled three-phase inverter having 3 MOSFETs per switch to meet the high current requirements. In order to assemble the module and avoid the Multi-Chip-Module (MCM) yield issue, all MOSFETs went through Known-Good-Die (KGD) testing. The presentation will particularly concentrate on the reliability of the die on leadframe solder joint during thermo-cycling. Failure curves will be presented for direct solder attach and attachment using an AlSiC interposer underneath the die, which greatly improved thermo-cycle capability. Results of the full validation matrix will also be presented, which include all typical reliability tests needed to qualify automotive modules for the harsh environment.

2B.4 Using Linear Superposition to Understand the True Meaning of Theta-JA

Roger Stout, ON Semiconductor

Abstract not available at time of publication

Session 3A: Passive/Electro-Mechanical Issues (Part 3)
Tuesday, May 22
1:15 pm – 2:55 pm
Two Rivers Room

3A.1 Automotive Multilayer Varistors

Ron Demcko, AVX

Abstract not available at time of publication

3A.2 Automatic Optical Inspection

Zoltán Németh, EPCOS

The purpose of the presentation is to give an overview on the potentialities and difficulties in implementing AOI systems. It highlights the points have to be considered during the planning and implementing phase by using examples from a realized project for passive components. The scope of the presentation is:

- Differences between eyesight and digital image processing
- Advantages and disadvantages of AOI
- Requirements of a proper failure definition
- How to reduce type II failures?
- Technical pitfalls
 - Monochromatic aberration
 - Shape recognition
 - Reflections and shadows
 - Recognition of hide objects
- Effects on product quality
 - compare before and after situation
- Effects on productivity

3A.3 Decoupling Capacitors

Michael Randall, KEMET

Integrated circuit (IC) technology has advanced over time, requiring innovative decoupling capacitor solutions. This paper discusses several new and advanced decoupling capacitor solutions, targeted to meet the power management needs of advanced microprocessors. These solutions offer very high capacitance density (as high as $>1,000\mu\text{F}/\text{in}^2$) combined with very low inductance (as low as $<1\text{ pH}$). These products have novel designs, targeted to the specific needs of the decoupling community such as board and package “real estate” management, microprocessor thermal management, power noise filtering, board flexure robustness, and simplicity of design and use. Additionally, these products were developed with the intent of reduction in “total cost of ownership,” having the potential to enable decoupling component reduction and to reduce pick and place steps.

3A.4 A High CV Capacitor with Low ESR Flexible Fuse Built in for Reliability Demanding Applications

Slavomir Pala, AVX

The automotive industry's current trend is to use ever greater number of electronic components in its new models. The performance of these electronic components in such harsh environments and electrical operational conditions is the most demanding outside of that required for Military and Space applications. This demands that the supply chain provide very high reliability products with proven performance in these most demanding of applications in ever shorter design cycles in a cost benefit manner.

Increasingly all aspects of safety as well as reliability has to be taken into consideration and the consequences of component failure be thoroughly considered. As electronic applications plays an increasing role in cars functionality, performance and safety this presentation will focus on two electronic components with a higher generic safety characteristic in failure as well as offering higher reliability levels.

The presentation will focus on new generation of capacitors with higher nature safety behaviour and thus offering higher reliability role compare to general ones. The discussion will be around capacitor technologies of Niobium Oxide Capacitors (OxiCap™) and Tantalum Capacitors with an integrated flexible fail-safe fusing system. These offer the circuit designer the opportunity to engineer his circuits in the anticipation of a component level failure but still maintain a reliability management control of the system.

Session 3B: Semiconductor Components - General Issues

Tuesday, May 22

1:15 pm – 2:55 pm

Tulip Grove Ballroom

3B.1 New Quality Requirements for Specific Electronic Component Commodities

Jean Clarac, Siemens VDO

The aim of this presentation is to give an overview of some new electronic component requirements based on real failures observed in the field at different car manufacturers. The definition of these requirements has been established for several different families of components (active, passive and electromechanical) used in a lot of electronic control units. The different root causes of the failed components have been checked in a deep way using the failure analysis reports provided by the electronic component suppliers. These analyses allow us to formulate requirements which have been classified for each electronic component commodity in three main categories:

Qualification requirements
Production requirements
Test requirements

This paper will give an idea on these new requirements. This could be the base of a new study for AEC council in order to make a new step in the quality of electronic components and should be used as an improvement to reduce the gap toward the zero defect approach.

3B.2 Stress Interaction Tests

H. Lewitschnig & W. Kanert, Infineon

Stress testing according to Q100/Q101 uses various stressors to cover the product's lifecycle. This set of tests is an accepted standard. Nevertheless, on product level there might be specific failure modes that cannot be elicited by Q100/101 standard stress testing. This can lead to "blind spots" in the product qualification. These are failure modes that could occur in the automotive application in the field, resulting in an increased failure rate. Stress interaction tests can be used to reveal such failure modes by regarding two or more stressors.

Stress interaction tests are derived from the environmental stress to which the devices are exposed in the automotive application, thus they are generally valid and apply to all kind of devices. Orthogonal designs can favourably be used for setting up stress interaction tests, where 2 stressors are applied, representing the combined field stress in the automotive application. To locate the position of each design point, end of life tests are used. The design points are approached by various ways to evaluate for path-dependency of the applied stressors.

The results give an insight into the occurrence or non-occurrence of conceived failure modes. Field stress conditions are estimated to determine the relevance of them. Specific fields of applications are given for stress interaction tests as well as further outlooks to refine the test setups.

3B.3 Quality Spill Analysis for Avoidance of PPM Peaks on Purchased Semiconductor Components

Hans Cervá, Siemens VDO

Accidents are defined as sudden but random, economically severe quality problems during product development or delivery with failure rates higher than about 100 PPM. Several recent cases were studied to derive common characteristics which allow a classification of the events. Representative examples will be given. Focusing on semiconductor front end technology the interface between design and process technology and the currently process-focused quality approach were found to be sources for accidents. As an alternative a product function oriented view is proposed, which entails e.g. establishing quality milestones in the process flow, or new statistical process control methods. Moreover, the risk of the applied technologies for the product related design was often not evaluated with the right conclusions and caused accidents. This study calls to make use of established quality control methods more intensively but always being aware of the final application. The measures will have to be identified and set up together with the semiconductor industry.

3B.4 EOS Rootcause Evaluation by Means of Failure Signature Investigation

Gerold Schrittmesser, Infineon

Chapter 1

- How does EOS-ESD damage appear at customer
- EOS-ESD related customer rejects - standard flow
- EOS-ESD related customer rejects - improved flow

Chapter 2

- EOS-ESD introduction (indications, sources)

Chapter 3

- Simulation of EOS events and failure signature evaluation
- Comparison with FAR - failure signatures
- MATRIX: EOS failure signature(s) vs. possible root cause

Session 4: Semiconductor Testing (Part 1)

Tuesday, May 22

3:15 pm – 4:55 pm

Tulip Grove Ballroom

4A.1 Part Average Testing (PAT) in the Electrical Wafer Sort

Peter Binkhoff, ELMOS

This paper describes the implementation of the PAT as a part of a continuous improvement process at ELMOS in 2004. It will help with examples from the real live to understand the aim of PAT and the advantages when implemented. An overview of our "home grown" software shows what is mandatory to have for setting up and maintaining PAT in production. Furthermore, will a collection of "Lessons Learned" help to avoid that PAT become something of an issue?

4A.2 Development and Use of a Parametric Failure Mode Effects Analysis in a Semiconductor Manufacturing Environment

Daniel J. Le Saux, Skyworks Solutions

The effectiveness of a wafer fab is often measured in its ability to react to problems in a timely manner as they arise during the manufacturing cycles. Sophisticated process controls are developed and deployed with the hope that process variation will be minimal and that the manufacturing processes will be predictable. When one of those process controls fails and scrap is created, a series of actions take place to contain the problem, uncover root cause and develop a corrective action plan. The effectiveness of the corrective action is verified and when successful, everyone is satisfied that a process improvement has been achieved.

The use of parametric process control plans coupled with a dynamic parametric failure mode effects analysis can spot potential high-risk process failures before they occur allowing the process engineer to take action proactively at a much lower cost. Once the process control plan is generated, every possible parameter failure mode is evaluated to assess the effects of the failure, the potential causes of failure and existing prevention and detection controls. Ranking scores are then attributed for severity, probability of occurrence and detectability based on a set of documented guidelines. A resulting Risk Priority Number is calculated for each process failure mode based on these scores. Finally, action items are generated for RPN values above a predetermined threshold. This approach allows risks to be ranked and forces actions to be taken on the highest threats.

The traditional sequence when using these tools is to generate the FMEA and subsequently develop the control plan. Skyworks has taken a novel approach whereas the

control plan is generated first to ensure that all process parameters are documented, and then use this list to develop the FMEA. Data from the FMEA drives changes back into the control plan creating a closed-loop, continuous improvement mechanism. This paper will show the advantages to using this approach and what cost savings can be achieved.

4A.3 Improving Automotive IC Quality. A Case Study on the Implementation of Advanced Iddq Strategies Targeting Product Quality Improvement, Burn-in Elimination and Test Cost Reduction

Markus Schmid, Q-Star Test

To be able to keep up with the increasingly stringent quality requirements imposed on semiconductors for automotive applications by the automotive business a very effective reliability screening is needed. This paper presents the progress on the implementation of an advanced IDDQ test strategy, with the objective to combine overall test time and test cost reduction with product quality improvement and burn-in elimination.

4A.4 SPC, PAT What's Next? - Advanced Data Mining

Philippe Briot, Briot & Associates

Abstract not available at time of publication

Session 5: Zero Defects

Wednesday, May 23

8:00 am – 9:40 am

Tulip Grove Ballroom

5A.1 OEM SCR Expectations In A Zero Defects Environment - Perspectives From Your Supply Base

Mary Carter-Berrios, KEMET

Achieving zero defects, by definition, dictates that change must occur. Typically all changes must be communicated to OEM customers, many of those passing these changes on to their customer. Over time, the responsibility for approving these changes has either been passed down to or expanded to include Program Managers at the individual location level. For commodity components, such as capacitors, this means that the responsibility has been expanded over all programs, as these basic components are used on all programs. What has resulted

is an increase in approval time, precluding implementation of those improvements that help us all achieve zero defects.

This paper is intended to illustrate industry performance relative to the SCR approval process. The identity of individual OEM customers will not be provided. In contrast, the paper is intended to educate the audience on supply base perspectives relative to overall industry performance. It is also intended to spark enthusiasm for how this area relates to realizing quality improvements in a timely manner.

5A.2 Zero Defect as Key for our Future

Klaus Behrendt, Infineon

Presentation of a strategy and a collection of corresponding projects which serve to meet the customers' requirements for Zero Defect (ZD). The represented scope contains several Front End volume production lines for power and automotive semiconductor products:

- Motivation and definition of a common goal
- List of specific projects to support the strategy
- Definition of appropriate indicators with targets to measure the achievements
- Details of selected examples:
 - o Zero Defect Mindset to convince every employee of the value of ZD
 - o Harmonization and optimization of SPC to use for line control
 - o From rigid to "Intelligent Scrap Limits" for wafer testing
 - o Fast inline feedback with Advanced Process Control (APC)
 - o Defect Density reduction to identify and to eliminate the most reliability relevant defect types

This Zero Defect program is embedded in an Automotive Excellence Program from the entire business division.

5A.3 Advanced Zero Defects Activities for Automotive Products

Tony Walsh, NEC Electronics

Automotive semiconductor products require Zero Defect Quality. This paper discusses the activities used by NEC Electronics to achieve that goal. The activities involved in a Zero Defects Program require a wide variety of tools and processes across the total supply chain and support functions. This paper will explain some of the activities applied in the area of Design, Manufacture, Test, Improvement, Capability and Problem Resolution.

For the supply chain the use of Built-in Self and Scan at Design to improve test coverage and improve failure rates. To prevent defect escape and maintain process capability the application of an innovative "Human Sensor" activity based on the employee's high level of consciousness and NEC's original, SPC based QWACS are used at Manufacturing and at Test the use of novel temperature

screens are applied. In the area of support Monitor Burn-in Tests are employed for feedback to Improvement activity coupled with reliability tests to improve Capability. Finally, the globalization of Failure Analysis to improve customer support.

5A.4 Towards Zero Defects by Cost Effective Screening Methods

Y. Xing & M. Lemnawar, NXP Semiconductors

Automotive applications have driven IC quality levels towards Zero Defects. Statistical screening methods like the Part Average Testing (PAT) have been recognized as an effective method to enable the semiconductor industry to meet such high quality demand. Different implementation techniques in the production process are available, either commercially or developed by the semiconductor companies themselves. These techniques vary from post to on-line and/or real time test-data processing by hardware and/or software tooling. In most cases, adaptation of the existing test production process is necessary and capital investments are needed. In practice, these concerns may slow down the pace of the implementation roll-out plan, especially at places where equipments are shared in production lines with non-automotive products.

NXP has had many years of experience of practical implementation of PAT in the production lines for the automotive products. A technique called Moving-Limits Testing has been developed, which can be used to deal with parameter nearest-neighbor residuals within a wafer, or screen out assembly failures during packaged product testing. This particular way of dynamic PAT implementation requires only slight modifications of production test programs at very limited increase of costs. Another way of screening out defects is to make use of parameter correlations, like the ones between Iddq and the operating frequency in a digital SOC. Such correlations, however, can be found between many parameters of an analog IC, which can be easily explored for defect screening. This presentation will demonstrate the effectiveness of these methods obtained from automotive products in volume production over the years, substantiated by the failure analysis results.

Session 6: Novel Methods - Test & Analysis

Wednesday, May 23

10:05 am – 11:45 am

Tulip Grove Ballroom

6A.1 ESD Protection Structure Qualification - A New Approach for Release for Automotive Applications

Werner Kanert & Michael Goroll, Infineon

To protect semiconductor products from damages due to electrostatic discharges separate protection structures are necessary. These structures are part of the device pad circuitry and designed for a dedicated wafer technology and ESD (electrostatic discharge) withstanding voltage. None of the present automotive qualification standards covers a qualification and release of ESD protection structures related to their designed ESD strength. The paper will introduce a new qualification strategy for ESD protection structures depending on the designed ESD target. On dedicated ESD diodes drifts of several parameters vs. time were analyzed. The results will be presented and discussed. Release targets for automotive applications will be defined and shown.

An ESD protection device is able to transfer positive and negative electrostatic discharge pulses to ground faster than the device which has to be protected. Bi-directional Z-Diode structures and their breakdown behaviour can be used as such devices. They are part of a wafer technology dependent device pad circuitry which will be used in several products. The wafer technology itself will be qualified and released according to standard procedures covering devices, metallization and dielectrics reliability. A qualification and release procedure for ESD protection devices is missing and must be defined inside these standards. The target ESD withstanding voltage must be assured. Based on the drift analysis of dedicated ESD diode parameter release targets for automotive applications must be defined and discussed.

6A.2 A Novel Technique for Failure Analysis on Multiple Chip Packaged IC Devices

Smile Peng (et al), Integrated Silicon Solution, Inc.

The Multiple Chip Package (MCP) technique gradually becomes a new IC industrial trend in miniaturization. Technique development for easy and expeditious failure analysis on any single chip inside the MCP is indispensable as this trend continues. In the past, using probe-card to probe the chip directly or employing side-braze tool with re-bonding art to convert a chip into a package suitable for electrical characterization have been used in the MCP industry. However, the abovementioned methods need preparation of additional hardware before possible execution of any electrical measurement.

In this study, for the first time, a novel technique for failure analysis on a failed die in MCP has been developed. We first remove the chip to be analyzed from the MCP and place it on the center of a "host" package (used for single chip production), which has been ground up to the point that its lead frame is exposed. Aluminum wires are then bonded to connect the pads on the chip and the exposed lead frame on the package. A unique feature in this technique by using the single chip package (presumably already in production) as the host package is that existing electrical tester system and test program is immediately available for the purpose of analysis. No additional effort in any custom built testing hardware and software is necessary. Performing electrical failure analysis on the device in this technique is exactly identical to the way usually done on one in a single chip package. This novel technique provides a simple and expeditious way for failure analysis on a failed MCP chip.

6A.3 Sample Preparation Techniques For a Solid Immersion Lens

Tetsuya Sakai & Tsuyoshi Shirahama, NEC Electronics

Automotive semiconductor devices require 0 ppm quality level. Thus the precise analysis of failed samples and root cause determination has become crucial. With the increase in complexity of semiconductor devices exact fault localization has become more difficult. Emission Microscopy (EMS) and OBIRCH are key analytical tools for fault localisation. Both tools are optics based so their spatial resolution depends on the wavelength of light. Failure point localization for recent devices has not always been possible due to inadequate spatial resolution.

To improve the spatial resolution, a Solid Immersion Lens (SIL) is used for EMS and OBIRCH. SIL is only used in backside analysis. This can become a problem when, as in the case of small packages, the lead frame structure interferes with the operational window of the lens. A solution to this is to prepare the sample, ground to hundreds of micrometers using a mechanical polisher and remounted onto another device. The remounted sample is rewired and the package de-capsulated from the backside. EMS using SIL can now be successfully preformed. This technique can overcome the physical restrictions of using SIL and can be applied to many kinds of failed samples.

6A.4 Diagnosis of Structural Scan Failures to the Net/Node Level Using the Inovys Ocelot Tester and the Tetramax or FastScan ATPG Tools

Thomas Van Vossel & Kelly Burnside, AMI Semiconductors

As ASIC designs increase in complexity, speed and density, increasing test time and cost become a challenge to maintain high profit margins. One solution is the leveraging of Design for Test methodologies, such as structural scan testing, which verifies the internal semiconductor components rather than the functional behaviour of the entire device, resulting in a simpler and

lower cost test strategy. However, this technique can result in difficulties for design debug and failure analysis, necessitating a fast, reliable method for diagnosis of these structural scan issues.

The Inovys Ocelot testers allow testing of scan chain failures in an FA lab setting, creating datalogs in Tetramax or FastScan format and then diagnosing the failure to the net/node level. This represents a significant technical advantage over the traditional methods of structural scan diagnosis, reducing the time and effort required to accomplish design debug or failure analysis on structural scan issues.

Session 7: Pb-Free Issues
Wednesday, May 23
1:15 pm – 2:30 pm
Tulip Grove Ballroom

7A.1 Accelerated Ageing and Solderability Test of Tin Plated Components

Marc Dittes, Infineon

The introduction of new lead(Pb)-free surface finishes on semiconductor components requires a critical review of the current solderability test conditions. In order to identify a reasonable test for the solderability of the components it is necessary to correlate both the accelerated ageing to natural ageing in typical storage conditions and to correlate a solderability test such as "Dip & Look" to real board assembly conditions. Such data are not available today.

In this presentation we will introduce such a correlation for natural ageing with accelerated ageing in various conditions (dry heat 150 °C and 170 °C, damp heat 85 °C / 85 % RH and steam ageing) for matt tin plated components. We provide a mathematical model of the oxide growth with the respective parameters for all above conditions based on oxide thickness measurements by TEM analysis and show that standardised accelerated ageing exceeds the natural ageing by orders of magnitude. Moreover we show the correlation of a critical reflow assembly process to Dip & Look solderability test for both SnPb soldering and lead-free soldering for various component types. Finally we will propose alternative parameters for both the ageing and testing of the solderability of tin plated components.

7A.2 Solderability Issues Resulting from Lead Free Processing

Jack McCain, Siemens VDO

Abstract not available at time of publication

7A.3 Matte Tin (Sn) Plating of Semiconductor Devices – Update of Whisker Growth Study

Bruce Townsend (et al), Spansion

Now that the semiconductor industry has essentially completed transition to lead free ("Pb-free") processing, and having met the July 1, 2006 deadline (with the exception of a few market segments; namely Automotive, Medical, Mil-Aero, and a few others), many new Pb-free processes are undergoing continuous improvement and optimization through on-going individual and collaborative initiatives (iNEMI, IPC/JEDEC, AEC, etc.). At this time, we feel that it is beneficial to the automotive reliability community to share knowledge, in an effort to improve the reliability of Pb-free components in automotive applications, and the purpose of this presentation is to do just that in a specific area of current interest - development and optimization of Pb-free plating processes, including mitigation of tin whisker growth in the post-plating and application environments.

Our earlier work on plating process development and optimization has been previously published, and presented at the IPC/JEDEC 6th International Conference on Lead Free Electronic Components and Assemblies (Aug. 19-20, 2004 in Singapore). Based on previously published data, and on-going results presented here, we continue to demonstrate that 100% matte tin plating on copper substrate lead frames (with post-plating anneal bake, and no nickel underlay barrier), can be resistant to whisker growth under a variety of environmental stress conditions.

Session 8: Semiconductor Qualification/Validation

Wednesday, May 23

2:50 pm – 4:30 pm

Tulip Grove Ballroom

8A.1 DoD Trusted Integrated Circuit Policy

Sydney Pope, Department of Defense (Acquisition, Logistics & Technology)

Microcircuits and related electronic devices are increasingly dominated by global commercial interests, making issues of trust (anti-tampering), product reliability, and assured sources of supply increasingly more difficult to manage. The purpose of this paper is to present possible policies and strategies to help address both defense and aerospace risks in this area. The product development strategies and supply-chain management practices of today do not adequately prevent electronic device tampering, counterfeiting, and reverse engineering. They do not assure that components, which are heavily dependant upon commercially derived technologies and designs, will conform to the performance demands inherent in aerospace and defense environments. Neither do they depend on them being maintainable throughout their service-life. This paper suggests ways the defense and aerospace sectors might better assure that their electronic devices and systems the Department has become dependant upon can be trusted to perform securely and reliably.

8A.2 Failure-Driven Qualification for Reliability and Analysis of Electronic Components

Pascal Lecuyer, Atmel

Electronic devices are playing an ever-growing role in highly demanding automotive or avionic applications – particularly in terms of improved safety and comfort. However, as semiconductor technology for use in vehicles becomes more and more complex, the need to identify and understand failure mechanisms has become vitally important. The MEDEA+ FdQ project involves the whole automotive industry value chain in addressing this issue by developing a failure-mechanism driven qualification methodology for an enhanced reliability of electronic components.

A consortium including, SIEMENS VDO, EADS, NXP, AMIS, STM, IMEC and coordinated by ATMEL has been working since 2004 towards the implementation of the failure-driven qualification concept into the Automotive and Avionic industries. This resulted in potential failure mechanisms knowledge, reliability assessment methods and an initiative towards Zero Defect in the field. As AEC-Qxx Stress Test Qualification is supposed to remain a basic stone in the qualification approach, a preliminary document was issued to describe the practical

implementation of the failure-driven concept consistently with the AEC-Qxxx documents.

8A.3 Failure-Mechanism-Driven Reliability Monitoring

Matt Kas, ON Semiconductors

At ON Semiconductor, we are currently redefining our RAP (Reliability Audit Program) (“Pass the Specification”/Go-No Go Environment) into a SRM (Statistical Reliability Monitor) Process (Dynamic Environment conducive to failure rate improvement) from Device Selection through execution. The current RAP program is stress driven and does not predict the Field Failure Rates and Mechanisms. In other words, On Semi’s current RAP is currently “go” “no go” type testing. Our Automotive customers frequently ask for comprehensive RAP data. At this Lean Six Sigma Black Belt Improvement project, we start with selecting right devices for failure mechanisms, implementing shift analysis with narrower spec limits for early out of control warnings, and selecting Failure Mechanism correlated RAP tests. We would like to minimize # of tests required. We target to end the project with implementing statistical monitors which flag the sensitive parts for RAP program.

ON Semiconductor is in the process of transforming/improving the RAP process from a Stress Driven Monitoring Process into a Failure Mechanism Driven Monitoring Process. The suite of metrics are being tailored to monitor the failure mechanisms which limit the Reliability. This is distinguished from a stress-driven monitor approach in which a fixed suite of acceptance stresses or other testing are prescribed and applied without customization according the failure mechanisms for the component. Both intrinsic (wearout and systematic) and extrinsic (defect-based) sources of failure are addressed. Recently, there are also efforts at JEDEC JC14 Committee to release new standard for Failure Mechanism Driven Reliability Monitoring JESD659B. ON Semiconductor is also closely following this standard to improve its RAP process.

8A.4 Robustness Validation – Why Are We Here and What Do We Get Out of It

Roger Rickey, R.F. Rickey & Associates, Inc.

This paper focuses on the history of the Automotive Component Qualification process, the change in customer requirements, a revised method for component qualification using Robustness Validation qualification methodologies, and the benefits thereof. To determine the robustness of our designs we must determine the mission profile – what conditions under which the component must function, develop the specifications for the components operating parameters, and test to FAILURE to determine the margin between the specification and the component’s performance.

In order to be considered robust, the component’s performance must exceed the specification boundary limits. By testing to failure, or End of Life (EOL) we

determined the robustness of the component and know its reliability value. In order to be considered robust, the component's performance must exceed the specification boundary limits. By testing to failure, or End of Life we determined the robustness of the component and know its reliability value.

Session 9: Semiconductor Testing (Part 2)

Thursday, May 24

8:00 am – 9:40 am

Tulip Grove Ballroom

9A.1 Iddx Monitoring In Failure Analysis and Continuous Quality Improvement

Michael Wieberneit, NEC Electronics Europe GmbH

It is well known that for digital CMOS integrated circuits (ICs) the characteristic of the quiescent power supply current (Iddx) is able to detect potential defects of the device. Iddx monitoring based on the Iddq pattern implemented in the mass production test is a novel approach in the failure analysis of NTF devices. Because the Iddx current is measured in the power supply lines the detectability of a potential defect on digital CMOS IC is very high, however a localisation of the potential defect by means of the current response is almost impossible.

In this paper we demonstrate a failure analysis process based on Iddx monitoring together with fault location techniques as emission microscopy (EMMI) or OBIRCH. Examples show the correlation between abnormal Iddx signature and the possible defect spots measured by EMMI or OBIRCH. As a result, to understand the true position of the defect conclusive results of Iddx, EMMI, OBIRCH and layout analysis is required. Being successful in the failure analysis triggered by the Iddx monitoring, the vectors leading to the abnormal Iddx signature are used to improve the Iddq coverage within the mass production test. It is shown by an example that by this approach the quality of digital CMOS ICs has been improved towards a single digit ppm level.

9A.2 Multivariate Methods of Quality Assurance in Automotive Electronics Production

Beyreuther, Siemens VDO

The relevance and complexity of automotive electronics is enormously increasing since years. Especially on component level it is more and more crucial to avoid and further decrease any field returns and warranty issues. That is the reason why quality improvement programs for a zero defect approach are installed within this sector. One aspect of reaching this target is to improve the process control of electronics production as a preventive measurement.

This presentation will introduce a new statistical method of multivariate process control with the help of a first case study done in cooperation with a semiconductor supplier. The disadvantages of the current univariate state of the art process control are presented and show clearly the necessity of a multivariate approach. This, according to the name of the new method, especially lies in the simultaneous control of all relevant variables and their mutual relationship within the process. A short overview of the mathematical background of this method will be given and illustrated by the case study. Especially, a new way of signal interpretation will be presented, which solved the last main obstacle of this method on the way to industrial practice.

9A.3 Maverick Lot Handling Implementation at NXP Semiconductors

Jaap Bisschop, NXP Semiconductors

Driven by automotive customer requirements for Zero Defects a program for improvement has been set up in NXP Semiconductors. As a part of this program Maverick Lot Handling was introduced throughout the production flow. Maverick triggers have been defined for all stages in production, i.e. in-line, PCM, Wafer test and Final product test. The triggers are based on a possible quality and reliability risk for the product. In addition, rules for maverick lot dispositioning have been defined and implemented. Decisions are made by the Material Review Board, and are based on a solid risk assessment. Special attention will be given to maverick limit setting at wafer test and final test. Examples of detected maverick and the physical defects captured by the handling are shown.

KPI's are monitored and the results are reviewed in regular PDCA meetings in operations, with special attention for interactions between waferfab and assembly operations. Based on this feedback improvements are implemented in wafer fabrication, and in assembly and test operations, which lead to prevention of re-occurrence and ppm reduction. A summary of experience with maverick handling is given.

9A.4 Strengthening Logic BIST with Iddq - Taking the Best of Both Worlds

Hans Manhaeve (et al), Q-Star Test

A Logic BIST approach typically combines stuck-at and speed testing. This paper discusses extending Logic BIST testability by including graded IDDQ testing during the BIST execution. The application and implementation of such a strategy on a recent Freescale Semiconductor SoC device illustrates its feasibility. In addition, the paper proposes and discusses the use of a new combined stuck-at - IDDQ fault coverage metric to determine the quality of a given test set when running both logic and Iddq tests. The results obtained show that a very high fault coverage IDDQ test is achievable by reusing the pseudo-random patterns provided by the Logic BIST controller. The end result is a test time saving BIST approach combining both stuck-at and IDDQ test in a single BIST execution, combined with a new test quality metric.

Session 10: Memory & SER

Thursday, May 24

10:05 am – 11:45 am

Tulip Grove Ballroom

10A.1 Read Disturb in Flash Memories: Reliability Case

Marcello Monchiso, STMicroelectronics

It is known that program/erase cycling of Flash memories induces a degradation of the tunnel oxide insulating property usually referred to as Stress-Induced Leakage Current (SILC). An issue related to SILC is the read disturb, affecting cells in an addressed word-line, which can cause electron injection through tunnel oxide in the floating gate of erased cells during read operation. Read disturb can also be present in Flash memory with a poor tunnel oxide quality. Aim of this paper is discuss the effect of read disturb phenomena occurring in Flash memories embedded in microcontroller commonly used in automotive application. Cell Failure Density extrapolation from experimental data using statistical method is able to estimate defect probability and application's failure rate.

10A.2 Stress Methods Screen High-Voltage Oxides in Serial EEPROM Device Arrays

Miko Buzinski, Microchip

Low failure rate infant mortality failures are occasionally observed after standard automotive-production electrical tests. In some cases, these failures are related to failure of the high-voltage (20V) oxide (Vpp) within an automotive electronic system's serial EEPROM device array. With the oxide voltage clamped internally to prevent breakdown, and the voltage being internally pumped, normal high-voltage stress methods that place voltage at 80% of breakdown are not possible. This presentation will put forth a solution to this problem by showing how high voltage can be reached during automotive production test, and how the end-user application can be evaluated. The presentation will show how the stress on the oxide during production tests does not need to be as stringent as during end-application use. Additionally, methods of optimizing the voltage stress can be evaluated, resulting in higher stress on the oxide to screen latent defects, without sacrificing test coverage or affecting test time. The presentation will also show how improved stress tests can be run on automotive production units that have been tested and passed without stress. During this testing, small quantities of parts consistent with the field failure rate are rejected, resulting in reduced customer field failures.

10A.3 SER Overview

Tom Lawler, Lattice Semiconductor

High energy particles can induce radiation charge that induce soft error events in any integrated circuit particularly memory and logic circuits. The newly release Failure Mechanism Based Stress Test Qualification For Integrated Circuits AEC-Q100 revision G includes a new requirement for Soft Error Rate (SER) assessment using the JEDEC Soft Error Rate test methods. The radiation affects on device mechanisms responsible for soft error events will be reviewed. The AEC-Q100-Rev G uses the JESD89, "Measurement and Reporting of Alpha Particles and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices," test methods to quantify the soft error rates of integrated circuits used in automotive applications. A number of silicon device, product design and system mitigation options will be discussed.

10A.4 Radiation-Induced Soft Errors in 90nm and Below

Paul Ngan, NXP Semiconductors

Radiation-induced soft errors are an increasingly important reliability issue, primarily because of growing bit counts. Typically, the failure rate due to soft errors exceeds that of all transistor degradation issues combined. Soft errors are caused by cosmic neutrons or by alpha particles emitted by radioactive impurities. Static and dynamic RAMs are generally the most sensitive components. However, the contribution from logic to the SER at the chip level is increasing with technology scaling. In 90- and 65-nm technologies the soft-error sensitivities of a flip-flop and an SRAM bit-cell are comparable.

This presentation will discuss the impact of soft errors on chips processed in 90-nm and below. We will treat the experimental and theoretical methods that are used to assess the soft-error sensitivity of design elements. We will show experimental soft-error rate (SER) data for 90- and 65-nm processes. The influence of different factors will be discussed, including supply voltage, temperature, data pattern, bit-cell type, process variations, and the use of different process options. We will discuss methods to mitigate soft errors and how these are affected by technology scaling. Finally, we will discuss our view on the SER assessment of safety-critical product designs.

Session 11: Packaging Issues

Thursday, May 24

1:15 pm – 3:20 pm

Tulip Grove Ballroom

11A.1 Kirkendall Void and High Temperature Storage Life Testing

XinMiao Zhao & Frank LeGeros, Cirrus Logic

Kirkendall voids are a well-known failure mechanism affecting gold-aluminum ball bonds. In this work, ball bond failures post 1000 hour high temperature storage life (HTSL) tests are studied. The results show that there are limitations to HTSL testing. We found that ball bond failures due to Kirkendall voiding could be reduced by using a new high tensile strength type of bonding wire containing palladium. The data shows that ball bonds made with Pd alloy wire have a longer lifetime at elevated temperature than bonds made with standard "four nines" gold wire. An activation energy value for this new bond wire was derived.

11A.2 Warpage of Large BGA Packages - An Investigation on the Mismatch between Simulation Data and Actual Measurements

Daniel Vanderstraeten, AMI Semiconductor

Large Ball Grid Array (BGA) packages have the bad behavior to warp heavily during the solder reflow process. For BGA packages with a body size of 35x35 mm and bigger we receive on a regular base custom returns due to excessive warpage. Simulations using material properties provided by our subcontractors are showing the opposite. This paper shows the investigations done to reveal the gap in the materials properties and provides also a possible solution for the problem. Finite element simulations techniques, optical measurements and basic material analysis analysis techniques have been used to identify the gap.

11A.3 Innovation in High Performance Semiconductor Packaging Within NXP Semiconductors

P. Orberndorff (et al), NXP Semiconductors

The obvious trend in semiconductor packaging of decreasing package size is still continuing driven by integration and price erosion. Within semiconductor packaging several new concepts are now being used and developed which offer the opportunity to occupy a smaller space on the PCB or higher i/o per sq inch. The trend shows a development towards leadless packaging. Although these leadless packages will first penetrate in normal consumer products, it is expected that in the near future also high-end electronics, such as automotive electronics will be impacted.

In this presentation we would like to shed some more lights on these leadless packages and point out some of the advantages and possible disadvantages. We will show the recent improvements regarding the reliability of the well known BGA in relation to board level reliability and from there move to QFN and then will explain our newest concept: the Ultra Thin Leadless Package (UTLP) which can be seen as a successor of the QFN. This new concept has clear production advantages while at the same time allowing a further reduction in size.

11A.4 Novel Technique for Detection of Intermittents in Ball Grid Array (BGA) Packages

Douglas Goodman & James Hofmeister, Ridgetop Group, Inc.

Ball Grid Array (BGA) packages are commonly used for Field Programmable Gate Arrays (FPGA's). These packages contain a dense array of solder balls that are used to affix the device to a printed circuit board, but are subject to aging and eventual failure due to degradation of the solder joints from vibration and other environmental conditions. According to EETimes, 81% of new digital electronic designs utilize FPGA's. In this paper we introduce a solder joint built-in-self-test (SJ BIST) for detecting high-resistance and intermittent faults in operational, fully programmed FPGAs. The approach is simple to implement, offers a method to detect high-resistance faults that result from damaged solder joints, and uses a maximum of one small capacitor externally connected to each selected test pin or each group of two test pins.