Automotive Electronics Council

Component Technical Committee

Agenda

(subject to change)

2006 - Eleventh Annual
Automotive Electronics
Reliability Workshop

May 9, 10, & 11

Indianapolis, Indiana

Sheraton Indianapolis Hotel & Suites

Tuesday, May 9, 2006

COFFEE (provided)		8:00 am - 8:30 am	**Continental Breakfast provided**	
Session 1: Passive/Electro-Mechanical Issues 8:00 am - 12:00 noon		8:30 am - 10:00 am	**Breakout Session #1: ZVEI/SAE Zero Defect Review**	
	1A.1	8:30 am - 9:00 am	Thomas Zahner *OSRAM Opto Semiconductors GmbH*	Thermal Characterisation of High Optical Power LEDs
	1A.2	9:00 am - 9:30 am	Hisamitsu Kawasaki *SANYO Electronic Device USA*	Reliability Testing of Organic Semiconductive Capacitors
		9:30 am - 10:00 am	**Q200 Document Review & Discussion**	
		10:00 am - 10:30 am	**BREAK: Coffee provided**	
		10:30 am - 12:00 noon	**Breakout Session #2: AEC Zero Defect Review**	
		10:30 am - 12:00 noon	**Q200 Document Review & Discussion**	
LUNCH (on own)		12:00 noon - 1:15 pm		

Tuesday, May 9, 2006 (continued)

Session 2: Discrete Semiconductor Issues 1:15 pm - 3:00 pm	**2A.1**	1:15 pm - 1:40 pm	Gerold Schrittesser *Infineon Technologies AG*	EOS-ESD Root Cause Evaluation by Means of Failure Signature Investigation
	2A.2	1:40 pm - 2:05 pm	Don Marzewski *Visteon*	Root Causes of Electrical Over Stress on Power Drivers
	2A.3	2:05 pm - 2:30 pm	Philippe Lejeune *Galaxy Semiconductor Solutions*	Integrating Parts Average Testing (PAT) into the Production Test Process
	2A.4	2:30 pm - 2:55 pm	Russell Graves *Ridgetop Group, Inc.*	An Electronic Prognostic Monitor for MOSFET TDDB
		3:00 pm - 3:30 pm	**BREAK (provided)**	
Session 3: Semiconductor Testing (Part 1) 3:30 pm - 5:10 pm	**3A.1**	3:30 pm - 3:55 pm	Gary Bolla *Visteon*	Capitalizing on Hidden Reliability Information After Customer Required Design Qualification Testing of Electronic Modules
	3A.2	3:55 pm - 4:20 pm	David Parker *Pintail Technologies*	New Standards for Quality: Real-time Dynamic Parts Average Testing at Final Test
	3A.3	4:20 pm - 4:45 pm	Emilio Salvioni *Salland Engineering (Europe) BV*	PAT and SBL Implementation
	3A.4	4:45 pm - 5:10 pm	Rajit Chandra *Gradient Design Automation*	Using a Temperature-aware Design Approach to Increase Reliability of Mixed-signal Integrated Circuits
DINNER (on own)		5:10 pm - 6:45 pm		
AEC Panel Discussion		6:45 pm - 8:00 pm	**Q101 Document Review & Discussion**	

Wednesday, May 10, 2006

Session	Paper	Time	Speaker	Title
COFFEE (provided)		7:30 am - 8:00 am	**Continental Breakfast provided**	
Session 4: **Memory - NVM, EEPROM, SRAM** **8:00 am - 10:55 am**	**4A.1**	8:00 am - 8:25 am	Marcello Menchise *STMicroelectronics*	Failure Rate Prediction for Data Retention
	4A.2	8:25 am - 8:50 am	François Giroux *STMicroelectronics*	Zero Failure Approach: Oxide Breakdown Reduction in EEPROM Products
	4A.3	8:50 am - 9:15 am	Martin Mason *Actel Corporation*	Neutron and Alpha Particle Single Event Upset (SEU) Failures in SRAM Technologies
	4A.4	9:15 am - 9:40 am	Mark Lowden & Paul Hay *Delphi Electronics & Safety*	Error Correction Coding (ECC) for Embedded Memories
		9:40 am - 10:05 am	**BREAK: Coffee provided**	
	4A.5	10:05 am - 10:30 am	Earl Caustin *MOSAID Systems, Inc.*	Testing Considerations for Accurate Measurement of Radiation Sensitivity of Modern High Speed Semiconductor Memory Devices
	4A.6	10:30 am - 10:55 am	Venkatesh Vasudevan *Intel*	Changes in Non-Volatile Memory Qualification Methods
Session 5: **Semiconductor Testing (Part 2)** **10:55 am - 11:45 am**	**5A.1**	10:55 am - 11:20 am	Michael G. Pecht *CALCE Electronic Products & Systems Center*	Prognostics for Automotive Electronics
	5A.2	11:20 am - 11:45 am	Greg LaBonte & Frederic Artuphel *Test Advantage, Inc & STMicroelectronics*	An Industrialization Program for DPPM Improvement
LUNCH (on own)		11:45 am - 1:15 pm		

Wednesday, May 10, 2006 (continued)

Session	Paper	Time	Speaker	Title
Session 6: **Zero Defects** **1:15 pm - 5:10 pm**	**6A.1**	1:15 pm - 1:40 pm	Tom Siegel *Delphi Electronics & Safety*	Delphi's Zero Defect Approach for Semiconductors
	6A.2	1:40 pm - 2:05 pm	Zhichun Wang *Philips Semiconductors*	Importance of Multi-Temp Testing in Automotive Qualification and Zero Defects Program
	6A.3	2:05 pm - 2:30 pm	Werner Kanert *Infineon Technologies AG*	Qualification Strategies in the Age of Zero Defect
	6A.4	2:30 pm - 2:55 pm	Masamichi Murase *NEC Electronics - Japan*	Zero Defects Quality for Automotive Bare Die Products
		3:00 pm - 3:30 pm	**BREAK (provided)**	
	6B.1	3:30 pm - 3:55 pm	Ralf Schlörke *Infineon Technologies AG*	Zero Defects Plans for Power Semiconductor Modules
	6B.2	3:55 pm - 4:20 pm	Tim Haifley *Altera Corporation*	To Bayes or Not To Bayes: ELFR (or how to sharpen those limits)
	6B.3	4:20 pm - 4:45 pm	Joeri Klutsch *AMI Semiconductor*	ASIC Quality Improvement through Dynamic Part Average Testing
	6B.4	4:45 pm - 5:10 pm	Ruby Clark *Freescale Semiconductor*	Product/Process Change Control in a “Zero Defects” Environment
DINNER (on own)		5:10 pm - 6:45 pm		
AEC Panel Discussion		6:45 pm - 8:00 pm	**Q100 Document Review & Discussion (Nick Lycoudes, Freescale - Industry Update on Reliability Test Methods)**	

Thursday, May 11, 2006				
COFFEE (provided)		7:30 am - 8:00 am	**Continental Breakfast provided**	
Session 7: **Packaging Issues** **8:00 am - 10:05 am**	**7A.1**	8:00 am - 8:25 am	Masakazu Yamana & Michael Wieberneit *NEC Electronics*	Reliability of COC Technology for Automotive Application
	7A.2	8:25 am - 8:50 am	Mike Varnau *Delphi Electronics & Safety*	Impact of Warpage on BGA Quality
	7A.3	8:50 am - 9:15 am	Russell Graves *Ridgetop Group, Inc.*	An Advanced Electronic Prognostic for FPGA Solder Joint Networks
	7A.4	9:15 am - 9:40 am	Min Ding *Freescale Semiconductor*	The Brittle Fracture of BGA Solder Joint during High Temperature Storage A Comparative Study of High Speed Shear/Pull and – A Comparison between SnPb and Pb-free Alloys
	7A.5	9:40 am - 10:05 am	Pascal Oberndorff *Philips Semiconductors*	Surface Mount Technology in the Pb-free Era
		10:05 am - 10:30 am	**BREAK: Coffee provided**	
Session 8: **New Technologies** **10:30 am - 11:45 am**	**8A.1**	10:30 am - 10:55 am	Glenn Tessmer *Texas Instruments*	Wire Bonding Divergence at the 65nm Node
	8A.2	10:55 am - 11:20 am	Bertrand Leigh *Lattice Semiconductor*	Managing Power and Noise on 90nm FPGA and Beyond
	8A.3	11:20 am - 11:45 am	Tomoya Omata *NEC Electronics - Japan*	Transistor Reliability and Its Effect on Circuit Characteristics in 90nm Node LSI's
LUNCH (on own)		11:45 am - 1:15 pm		

Thursday, May 11, 2006 (continued)				
Session 9: **Failure Analysis Issues** **1:15 pm - 2:55 pm** **** Refreshments available during session**	**9A.1**	1:15 pm - 1:40 pm	Diganta Das *CALCE Electronic Products & Systems Center*	Failure Modes, Mechanisms, and Effects Analysis for Automotive Electronics
	9A.2	1:40 pm - 2:05 pm	Eric Bedes & Will Frizzell *NEC Electronics America, Inc.*	Fault Localization and Verification Techniques for Semiconductor Devices
	9A.3	2:05 pm - 2:30 pm	Cleston Messick *Northrop Grumman*	Intermittent Failures in High Pin Count Packaging
	9A.4	2:30 pm - 2:55 pm	Zhongning Liang *Philips Semiconductors*	Surface ESD
WRAP-UP		3:00 pm - 3:30 pm	AEC Technical Committee	Closing Statements & Workshop Adjourned