

## Session 1: Passive/Electro-Mechanical Issues

Tuesday, May 9  
8:30 am – 12:00 noon

### 1A.1 Thermal Characterisation of High Optical Power LED's

*Thomas Zahner, OSRAM Opto Semiconductors GmbH*

The junction temperature of Light Emitting Diodes (LED's) is a primary reliability factor, which is affected by thermal resistance of the device. Exceeding the maximum rated junction temperature could lead to accelerated light output degradation and sometimes even to catastrophic failures. Therefore thermal characterisation of high optical power LED's is very important. It has to take into account that the power applied to the device is converted into heat and light (~20-30% efficiency). This means the thermal characterisation of LED's can not be completed without knowing the energy flux emitted as light. Beside that the interpretation of the thermal resistance is not obvious and the common definition is not sufficient. Therefore establishing a standard on how to do thermal characterisation of light emitting devices is necessary.

### 1A.2 Reliability Testing of Organic Semiconductive Capacitors

*Hisamitsu Kawasaki, SANYO Electronic Device USA*

SANYO developed OS-CON Capacitors almost 20 years ago and has been providing the Aluminum Solid Capacitors with Organic Semiconductive Electrolytes to many customers. These capacitors are very reliable at low and high temperatures and have unique characteristics that set them apart from regular aluminum capacitors. Over the last two decades, there has been a significant increase in onboard automotive electronics. Vehicles today have devices that control everything from ABS modules to Telematics. These electronic devices require high reliability standards because they control a majority of a vehicle's functions. SANYO currently follows the AEC standard requirements to maintain the quality and reliability of our components. The current AEC Standard does not require the measurement of variable temperatures after the reliability test for passive components.

SANYO recommends additional low and high temperature measurements to project conditions for long life performance of the capacitors. The additional test specifications should define the exact temperature. Sanyo performed the same reliability tests on an OS-CON and an aluminum capacitor. After the first test, additional measurements at a low and high temperature showed the differences in capacitance and ESR between the two capacitors.

## Session 2: Discrete Semiconductor Issues

Tuesday, May 9  
1:15 pm – 3:00 pm

### 2A.1 EOS-ESD Root Cause Evaluation by Means of Failure Signature Investigation

*Gerold Schrittmesser, Infineon Technologies AG*

#### Chapter 1

- How does EOS-ESD damage appear at customer
- EOS-ESD related customer rejects - standard flow
- EOS-ESD related customer rejects - improved flow

#### Chapter 2

- EOS-ESD introduction (indications, sources)

#### Chapter 3

- Simulation of EOS events and failure signature evaluation
- Comparison with FAR - failure signatures
- MATRIX: EOS failure signature(s) vs. possible root cause

### 2A.2 Root Causes of Electrical Over Stress on Power Drivers

*Don Marzewski, Visteon*

This seminar will review the basic construction of MOS and then talk about EOS mechanisms. We will also discuss how Smart MOS devices with self protection can EOS. This presentation may also dispel popular myths about EOS root causes.

Silicon MOS devices that are EOS typically do not have a clear failure mechanism since any evidence of potential root causes may be destroyed through device meltdown. Root Cause and corrective actions of EOS in power MOS devices are basically disregarded by component suppliers and Failure Analysis (FA) labs. FA labs cannot analyze a device if it has been vaporized away. Component suppliers cannot point to a specific Root Cause, so there is always a question of culpability. Even Smart MOS devices with protection circuitry fail with the same EOS signature. FA labs, component suppliers and module suppliers are then forced into creating a list of possible root causes of why devices can EOS. Traditional fish bone diagrams for EOS identify causes such as Electro Static Discharge (ESD) handling damage, wafer particulate contamination, and poor heat sinking. We will investigate these causes of EOS and help to eliminate what it is not.

## 2A.3 Integrating Parts Average Testing (PAT) into the Production Test Process

*Philippe Lejeune, Galaxy Semiconductor Solutions*

Parts Average Testing (PAT) is experiencing a wave of adoption among semiconductor companies that serve the automotive industry. The goal of PAT is to remove "outliers", that is, parts which exhibit atypical characteristics when compared to parts from the same wafer or lot. The current PAT requirements imposed by automotive suppliers are somewhat vague, and it is incumbent upon the semiconductor supplier to determine the right balance between increased reliability and decreased yield. In order to make this tradeoff intelligently, engineers need to perform a combination of yield simulation, historical data analysis and empirical studies, and closely monitor the process over time.

This paper, citing customer case studies, will describe a closed-loop approach to PAT and other DPM-reduction techniques, which improve device quality while minimizing unnecessary yield loss. Techniques for simulating PAT binning and correlating outliers with burn-in failures will be discussed. In addition, we will examine the requirements for integrating a complete PAT solution into the wafer manufacturing process.

## 2A.4 An Electronic Prognostic Monitor for MOSFET TDDB

*Russell Graves, Ridgetop Group, Inc.*

The ability to identify performance degradation and failure modes in integrated circuit (IC) components significantly enhances the safety and reliability of a component, system, or sub-system. Specifically, the ability to monitor electronic aging at the board level, and to detect an impending IC failure, facilitates the advent of corrective actions necessary to avert a catastrophic event. Based on the application of a board-level prognostic monitor chip, accurate predictions of electronic aging and end-of-life failure modes can be extracted.

A prognostic chip has been designed to monitor the Time Dependent Dielectric Breakdown (TDDB) of MOS transistors. The self-stressing integrated MOSFETs that are monitored by the prognostic chip act as the TDDB aging sensors for the host application. The monitored MOS transistors are identical to those used in the host IC, to insure that the extracted data maps to the condition of the key components of the host IC. The prognostic circuitry biases the MOS transistors to accelerate aging under certain environmental conditions. For this reason the monitor, or sensor devices in the prognostic chip are designed to be sacrificial, and are not used in the host application, but instead are packaged separately, mounted, and biased at the board level.

TDDB of silicon dioxide has been found to be exponentially dependent on the electric field across the gate oxide. Although the exact mechanism for every failure mode is not known, it is generally accepted that breakdown is caused by oxide charge trapping, and an effective oxide thinning, or reduction in the barrier height

seen by free carriers at defect sites. Acceleration of the breakdown of an oxide can therefore be achieved by applying a voltage higher than the supply voltage, to increase the electric field across the oxide. When the test monitor device fails, a certain fraction of the circuit lifetime has been used up. The fraction of useful circuit life that has been used up is dependent on the amount of overvoltage applied and can be estimated from the known distribution of failure times.

## Session 3: Semiconductor Testing (Part 1)

**Tuesday, May 98**  
**3:30 pm – 5:10 pm**

## 3A.1 Capitalizing on Hidden Reliability Information After Customer Required Design Qualification Testing of Electronic Modules

*Gary Bolla, Visteon*

This paper presents a strategy for Tier 1 suppliers to the automotive industry to use for acquiring and feeding back the "hidden information" from OEM Design Qualification (DQ) testing into the product development process, especially into product development testing, design models, and design guidelines. Although the approach may be applied to all products subjected to DQ testing, electronic modules consisting of printed circuit assemblies (PCA's) for automotive OEM customers will be the primary focus.

Customer DQ testing typically involves functional and environmental testing of pre-production product to an all-must-pass battery of customer specified tests. Its purpose is to demonstrate to the customer that the product they have contracted will survive their battery of tests, and hopefully *their* customers' (i.e. the consumers') usage environment. If the product (design) performs perfectly little value will be added, only assurance that the product is ready for production.

By performing "physics-of-failure" (PoF) based accelerated design margin testing on products that have survived customer qualification testing, important information of the products' failure mechanisms will be learned and knowledge may be captured through improved development testing, design models, and design guidelines. Key findings with this approach include an understanding of what internal development testing is most appropriate for design change verification.

### 3A.2 New Standards for Quality: Real-time Dynamic Parts Average Testing at Final Test

David Parker, Pintail Technologies

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The quest for extreme reliability in today's automotive industry has put pressure on semiconductor suppliers to implement zero defect initiatives. Any field returns or warranty issues related to electronic components are costly in terms of time, effort, money, and potential loss (as in 'life'). One method for improving the reliability of semiconductors going into cars is called 'parts average testing' (or PAT). The Automotive Electronics Council AEC-Q001 Rev. C guideline recommends a general method for using PAT. PAT is a methodology that prescribes detecting devices with test results that fall outside the six sigma limits for a given wafer, lot, or group of parts being tested and removing them from the population. Today, PAT is applied at the wafer sort step by most IC suppliers and it is generally performed using off-line, post processing analysis. However, solutions exist in the market today where real-time, on-line analysis is performed at both wafer sort and final test. In order to meet the true spirit of applying PAT to detect and remove outliers in semiconductor test, it should also be applied at final test. This paper will examine the advantages of real-time on-line PAT for improving IC reliability in the automotive industry.

### 3A.3 PAT and SBL Implementation

Emilio Salvioni, Salland Engineering (Europe) BV

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Semiconductor manufacturers serving the automotive world are facing the challenge to provide components whose reliability is beyond the capability or economic reach of standard processes. Implementing key methodologies like PAT and SBL is now mandatory and must be implemented without disruptions to the test floor operations. Product/Quality managers demand effective, flexible, accessible and future proof tools. The floor manager demands tools that actively help maximize efficiency.

The Dynamic Test-Cell Controller (DTC) here proposed is a low cost, scalable and open tool. The user determines the extent to which the tool is deployed within a single platform or to multiple/all platforms. The DTC provides best-in-class functionality to optimize the wafer-sort process. It has control of both wafer map and tester data STDF files are created by DTC, producing 100% data integrity, regardless of the mix of platforms. Trends can be monitored and actions triggered in real time (i.e., probe card cleaning, SBL flags, etc.). Test data in STDF format are processed locally with wafer maps data, good dice from bad clusters and outliers are immediately identified and binned-out. All settings and algorithms in the DTC are fully accessible to the expert user, who determines the best methodology to identify and screen cluster defects, outliers for each product and each single item in the test program.

### 3A.4 Using a Temperature-aware Design Approach to Increase Reliability of Mixed-signal Integrated Circuits

Rajit Chandra, Gradient Design Automation

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The constant temperature assumption used in mixed-signal design does not provide enough detail to predict the potential functional failures in final silicon that may be caused by parametric failures in circuits sensitive to temperature and temperature gradients. For more highly integrated designs with high power devices—such as digital blocks, bandgap reference circuits, PTATs, audio amplifiers, DACs, As, LDOs, and switching regulators—even a few degrees of variation in temperature over the temperature sensitive circuits can cause incorrect chip functionality. In addition, the use of constant temperature in reliability analysis may miss potential problems such as electro-migration or material breakdown due to inaccurate assumptions about the temperature variation and maximum temperatures.

Because of these problematic thermal-related design issues, a new temperature-aware design approach to estimating and predicting thermal behavior early in the design process is proposed. This approach integrates the IC design; chip, package and ambient temperature conditions; and the process technology impact to predict the performance of an integrated circuit in its final environment. Understanding the detailed temperature on individual devices and wires enables designers to understand the true performance and reliability of a design throughout the design process. Using this approach during the design stage allows designers to discover and make the changes necessary to correct temperature gradients, thus preventing devastating impact on chip performance, reliability, cost, and project schedule.

**Session 4: Memory - NVM, EEPROM, SRAM**

**Wednesday, May 10**

**8:00 am – 10:05 am**

### 4A.1 Failure Rate Prediction for Data Retention

Marcello Menchise, STMicroelectronics

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Microcontrollers with embedded non-volatile memories are widely used in the automotive market. Ability to retain the stored information for long time is the main characteristic of such memories. Automotive market is demanding very long data retention time and 0 rejects on field. In this job we are presenting a methodology to measure data retention performance and failure rate prediction. Data showed refers to advanced technology developed in STMicroelectronics.

## 4A.2 Zero Failure Approach: Oxide Breakdown Reduction in EEPROM Products

*François Giroux, STMicroelectronics*

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Driven by the high level of quality required by the Automotive industry, the development of new approaches is a necessity to reach the zero failure target at customer level. To meet this specific demand, ST introduced an Automotive Grade Program. As a part of this program, this contribution presents a zero failure approach where each stage of the product quality supply chain is addressed. The starting point of this approach is the data acquisition. Failure analysis, on qualification and production ramp up rejects, allows the identification of the main failure modes to be addressed. Based on this "failure mode" knowledge, a continuous research for quality solutions and innovative methods enables an increase of product robustness. The work directions are:

- Design: Design for Reliability, Design for Manufacturing, Design for Test...
- Technology: optimized recipes dedicated to critical elements
- Detection: screening, Statistical Bin Limit (SBL), and Part Average Testing (PAT)
- Application review in partnership with key customers

At each step, a risk assessment is performed with adequate validation. A feedback loop allows to check the efficiency of the implemented solutions and implement a continuous improvement for the following developments. The example of high voltage oxide breakdown reduction in the EEPROM products illustrates the presentation. Concrete ways to increase the robustness of these products are described based on the expounded zero defect approach.

## 4A.3 Neutron and Alpha Particle Single Event Upset (SEU) Failures in SRAM Technologies

*Martin Mason, Actel Corporation*

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The issue of single event upsets (SEU) in SRAMs devices has been well documented for many years. An issue that was primarily an aerospace and military based concern is increasing affecting ground based electronic systems especially those using cost saving deep sub-micron technologies. Failure In Time (FIT) rates for applications such as power-train and engine control modules can be several orders of magnitude higher for SRAM based technologies than nonvolatile alternatives such as Flash. This paper presents details on the problem and presents a case study of programmable logic devices based on SRAM, Flash and anti-fuse technologies. In particular the issues or configuration versus data SRAM upsets is explored as well as mitigation techniques and alternative technologies that can be used to strive for 'zero defects' in deployed automotive electronic systems and avoid the impact of potential SEU upsets in SRAM based FPGA solutions.

## 4A.4 Error Correction Coding (ECC) for Embedded Memories

*Mark Lowden & Paul Hay, Delphi Electronics & Safety*

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Error Correction Coding (ECC) for Embedded Memories - Data retention failures are a significant failure mode of microprocessors containing flash memory arrays. Shrinking cell sizes are also threatening to reduce the reliability of SRAM arrays due to single event upsets (SEU). The addition of error correction coding (ECC) circuitry to such arrays significantly reduces these failure rates by correcting single bit errors during operation. ECC allows automotive electronics manufacturers to use leading edge flash memory technologies in production with the excellent reliability demanded by the automotive industry.

## 4A.5 Testing Considerations for Accurate Measurement of Radiation Sensitivity of Modern High Speed Semiconductor Memory Devices

*Earl Caustin, MOSAID Systems, Inc.*

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For obvious reasons automotive drive-by-wire technology mandates the need for ever-increasing reliability levels in automotive electronics. Simultaneously, the ever-increasing requirement to reduce costs mandates the use of commercial off the shelf (COTS) semiconductor components in automotive electronic subsystems. Semiconductor memory is and will continue to be an essential part of automotive electronics subsystems. The amount of semiconductor memory will inevitably grow in quantity, density, speed and complexity as the requirements and intelligence of automotive electronics increases in future years.

One aspect of semiconductor memory reliability that has been studied intensively is its sensitivity to radiation. Alpha particle radiation from radioactive contamination of the packaging materials used in early semiconductor memories was eventually identified as the root cause of serious system failures in early computers. Luckily that issue was resolved well before the intense use of electronics in automobiles. Space electronics packages are routinely exposed to cosmic ray radiation and are carefully designed to withstand and/or recover from data loss inevitably caused by such radiation. Because the earth's magnetic field and atmosphere significantly reduce the ground level penetration of cosmic charged particles the effects of the residual charged particle radiation on ground level electronics has been far less of a problem until recently. Neutron radiation which penetrates the atmosphere to the ground level much more readily has historically not been a major contributor to memory failures in ground based electronics.

Now, however, COTS semiconductor memory device line widths are at 45nm and decreasing, data rates are measured in GBytes/sec and increasing, voltage levels are at 1.2V and decreasing, densities are at multi-Gigabits and increasing and complexities now standardly include synchronous operation, bank interleaving and data

bursting. In recent years commercial aircraft have experienced flight control systems failures which were traced to the unannounced replacement of COTS memory devices with devices produced with a new manufacturing process utilizing smaller line widths. While these newer devices were identical in form, fit and function, their reduced line widths made them more susceptible to radiation induced data loss. It is apparent that modern COTS semiconductor memory devices will increasingly become more sensitive to ground level radiation. Automotive systems manufacturers will be required to understand and to take into account the growing sensitivity to ground level radiation of the semiconductor memory components they design into future automotive electronics especially as drive-by-wire becomes standard. It is imperative to fully characterize these radiation sensitivities.

It is shown in this presentation that many studies of radiation sensitivity of modern semiconductor memory devices may have significantly underestimated the radiation because they did not test the devices in their normal mode of operation. It is shown that radiation sensitivity will be underestimated unless the test conditions include high speed operation, bank interleaving, complex timing control, burst operation and data scrambling.

#### **4A.6 Changes in Non-Volatile Memory Qualification Methods**

*Venkatesh Vasudevan, Intel*

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Non-volatile memory technology has changed dramatically over the years. New failure mechanisms have arisen while some familiar ones have diminished in importance along with the emergence of improved characterization methods. In response, JEDEC qualification methods for Non-volatile memory are undergoing major revision. This presentation describes the changes and JEDEC's response. Key changes include: 1) conversion to channel erase for NOR Flash; 2) greater use of NAND Flash; 3) new forms of dielectric storage memory; 4) spread of multi-level-cell (MLC) capability; 5) emergence of bit-to-bit interactions; and 6) increased use of knowledge-based, application-specific qualification methods. Data retention is no longer dominated by defect hopping ( $E_A=0.6\text{eV}$ ) but rather by SILC ( $E_A\sim 0$ ) and charge detrapping ( $\sim 1.1\text{eV}$ ). The standard  $150^\circ\text{C}$  bake is no longer appropriate and is being replaced. Bit-to-bit interactions and MLC make simple all-zeroes or checkerboard patterns equally questionable, and the revisions recommend more complex data patterns. New learning has uncovered the importance of the endurance cycling rate, and the revisions provide guidelines. Finally, as memory densities have increased it has become impractical to cycle every block to the endurance specification, and the JEDEC revisions provide guidelines for partial-array cycling. The presentation finishes with a summary of the current status of the JEDEC revisions and the relevance to the AEC.

## **Session 5: Semiconductor Testing (Part 2)**

**Wednesday, May 10  
10:30 am – 11:45 am**

### **5A.1 Prognostics for Automotive Electronics**

*Michael G. Pecht, CALCE Electronic Products & Systems Center*

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Prognostics is a method that permits the reliability of a system to be assessed in its actual application conditions. It is employed by integrating sensor data with models that enable in-situ assessment of the extent of deviation or degradation of a product from an expected normal operating condition (i.e., the system's "health") and also predict the future state of reliability based on current and historic conditions. The objective of prognostics is to: (1) provide advance warning of failures; (2) minimize unscheduled maintenance, extending maintenance cycles, and maintaining effectiveness through timely repair actions; (3) reduce the life-cycle cost of equipment by decreasing inspection costs, downtime, and inventory; and (4) improve qualification and assisting in the design and logistical support of fielded and future systems.

The presentation will provide various approaches for conducting prognostics of electronics. Sensors and models required for implementation will be discussed. A case study of prognostics of an electronic board in an automotive under-hood environment will be presented. Temperature and vibrations were measured in-situ on the board in the application environment. The measured data was reduced and processed to extract features, where were then used with stress and damage models to estimate the remaining life of the board. The presentation will provide a vision and plan for developing future automotive prognostic systems, that integrate sensor, on-board algorithms, telemetry systems, and global positioning system (GPS). The vehicles would be tracked using the unique 17-digit vehicle identification number and interrogated randomly from a remote location to acquire sensor data and assess the on-going reliability.

### **5A.2 An Industrialization Program for DPPM Improvement**

*Greg LaBonte, Test Advantage, Inc. & Frederic Artuphel, STMicroelectronics*

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STMicroelectronics and Test Advantage will jointly present the integration and demonstrated performance of a post wafer sort, test data analysis system for reduced DPPM. This discussion will outline the complete solution of all the key elements coming together as a fully automated manufacturing process referred at the semiconductor supplier level as the Automotive Grade Program. This program comprehends reduction of intrinsic defects at design using techniques that define solutions for robustness validation during new products development,

and embodies techniques for identifying extrinsic defects through the application of advanced outlier detection screening methods to eliminate parts that pose a quality risk.

The presentation will focus on the advanced outlier detection implementation and explore how both companies framed the project using core competencies from within both organizations. The semiconductor supplier has provided the integration platform, functional requirements and the overall program management support and leadership. The solution provider has delivered a state of the art capability for data analysis, utilizing an adaptive algorithms selection methodology based upon test data distribution shapes. This effort also involved the delivery of support during tool integration at the wafer-sort test facilities involving both training and consultancy. Executive commitment from both companies was evident throughout the project with the active role of an executive council and a technical committee targeting the achievement of program objectives without production interruption. Direct and lateral benefits of the program are examined identifying related risks along with solutions to control these risks.

**Session 6: Zero Defects**  
**Wednesday, May 10**  
**1:15 pm – 5:10 pm**

### **6A.1 Delphi's Zero Defects Approach for Semiconductors**

*Tom Siegel, Delphi Electronics & Safety*

Abstract not available at time of publication

### **6A.2 Importance of Multi-Temp Testing in Automotive Qualification and Zero Defects Program**

*Zhichun Wang, Philips Semiconductors*

For automotive qualification of Integrated circuits (ICs), multi-temp testing is required by AEC-Q100. In this presentation, we will demonstrate the importance and necessity of this multi-temp testing in automotive qualification of ICs and zero defects program by an example. High Temperature Operating Life (HTOL) and Early Life Failure Rate (ELFR) are important accelerate lifetime tests to simulate the degradation of ICs during application. During the qualification of one of our new products, we found that all stressed samples could pass electrical testing at room temperature but a few of them failed at hot temperature. Failure analysis tools like

OBIRCH and PEM were applied to investigate the failed samples. One transistor in the circuit was found to have abnormal large leakage current when it was at OFF state. However, the leakage current of the transistor was so low at room temperature that no malfunction could be detected. After HTOL/ELFR test, this transistor degraded further, but the leakage current was still so low that no malfunction can be detected by electrical testing at room temperature. Only when this leakage current was enormously increased during electrical testing at hot temperature, the fail was detected. Root cause was identified that a high gate source voltage was applied on the transistor during pre-testing because of a design error. Design error is corrected in the new version of the product, no failures are observed anymore. Our example demonstrates that some defects might escape in automotive qualification and production testing without multi-temp testing. Therefore multi-temp testing is important for zero defects program.

### **6A.3 Qualification Strategies in the Age of Zero Defect**

*Werner Kanert, Infineon Technologies AG*

Quality and reliability requirements for semiconductor components have considerably increased in recent years. In automotive areas, electronic components have found their way into many harsh applications like engine management, transmission and electronic power steering. In parallel, semiconductor technologies – both chips and packages - have continuously advanced on their way to smaller scale feature sizes, increased functionality and power densities. New materials have been introduced and will continue to be introduced in the future. At the same time a conspicuous increase in quality and reliability has been achieved, manifested in significantly decreased failure rates.

With all the progress, the way to qualify semiconductor products has essentially remained unchanged over the time. Today the AEC Q100 and Q101 are the de facto standards for product qualification of integrated circuits and discrettes, respectively, for automotive applications. However, the demand for Zero Defect poses new challenges to the industry. In view of this scenario it seems well justified to ask, if adaptation and improvement of our (i.e., the semiconductor industry) way of qualifying our components is called for.

Today's standard procedure of product qualification is based on a stress-test-driven approach, as is described in JEDEC JESD47. The same approach is also the basis for the AEC Q100. Alternative approaches such as "Application Specific Qualification", "Knowledge-Based Qualification", "Physics-of-Failure Approach", or "Failure-Mechanism-Driven Qualification" have been described in a number of papers and standards, but are rarely used today for product qualification. Silicon wafer technology qualification has traditionally been based on a failure-mechanism-driven approach. Successful examples are time-dependent dielectric breakdown (TDDB) of gate oxides, electromigration, hot carrier effects (HCE), and the negative bias temperature instability (NBTI), which has received considerable attention recently. On the package

and product side, this approach has not found that much recognition and acceptance. Though to some extent this may be due to a lack of knowledge, it is also true that applying the principles of this approach to these areas meets with some difficulties. Such a failure-mechanism-driven approach is being discussed today as an alternative to qualification for semiconductor components.

The paper wants to point at some drawbacks of the current qualification procedure and compare this to a failure-mechanism-driven approach. Although this failure-mechanism-driven approach is appealing because of its being founded on physical principles, it is not free from deficiencies. Such deficiencies are also discussed. The paper does neither claim nor intend to provide ready-made solutions. Instead, it wants to provide a look at some aspects of different qualification strategies to further discussion on ways to strengthen the AEC Q100/Q101 for future needs.

#### **6A.4 Zero Defects Quality for Automotive Bare Die Products**

*Masamichi Murase, NEC Electronics - Japan*

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Automotive electronics, especially automotive microcomputers, require Zero Defect Quality. Generally, the zero defect quality goal is targeted for packaged parts. However, it can be attempted for bare die products as well. In this paper, we discuss how NEC has applied Zero Defects Quality measures to its microcomputer bare die product. Bare die products are usually difficult to test and screen. Therefore KGD (Known Good Die) Quality level (< 10 ppm failure rate) has been hard to achieve. However, NEC has tried Zero Defects Quality level for its 0.35um microcomputer bare die products. Novel wafer test methods and innovative wafer screening methods have been devised to achieve zero defects goal. NEC has also adopted zero defects product line in which other products have been produced by continuous KAIZEN performance. Furthermore, advanced Failure Analysis technologies and stringent design reviews have been helpful to realize zero defect quality. NEC has also been regularly renewing its Zero Defects tools. Because of all the carefully planned steps, currently the field failure rate is 2 ppm, which is the same level as KGD. Additionally NEC has established bare die technology with the same quality level as KGD.

#### **6B.1 Zero Defects Plans for Power Semiconductor Modules**

*Ralf Schlörke, Infineon Technologies AG*

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Compared to discrete Power Semiconductors, Power Modules consist of a lot of more components, which makes them more complex and the production process more complicated. This complexity leads to a higher failure rate concerning delivery quality and lifetime of the components. While Discretes are currently running with a failure rate << 1 ppm, the compared figures of Power Semiconductor Modules have been in the range of some hundreds ppms only a few years ago. This paper shows by an example, how it is possible to achieve a failure rate

close to zero for Power Modules. This contains a long term evolution starting from the module design for manufacturing, as well as continuous improvement of the assembly process and a kind of final testing, which not only considers the data sheet, but is also very close to the application. With continuous improvement on all fields it was possible to manufacture and deliver zero defects over a significant period of time.

#### **6B.2 To Bayes or Not To Bayes: ELFR (or how to sharpen those limits)**

*Tim Haifley, Altera Corporation*

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This presentation introduces Bayes methods to augment zero defect sample plans traditionally employed in reliability tests. The zero defect sampling requirements of AEC-Q100 are based upon sampling (frequency) theory. This says that we estimate a fixed but unknown failure rate (PPM failure for ELFR or FIT rate in LFR) and that we sample from a very large population distribution. If we observe zero defects, then we rely upon confidence limits to estimate that failure rate. This presentation introduces the concept that the failure rate being estimated may, in fact, be a random variable rather than a fixed but unknown value. Issues of traditional sampling theory estimation and the improvement of those estimates using Bayes probability limits are discussed.

#### **6B.3 ASIC Quality Improvement through Dynamic Part Average Testing**

*Joeri Klutsch, AMI Semiconductor*

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Dynamic Part Average Testing (DPAT) is evaluated as a technique to improve the quality of a variety of semiconductor ASICs (application specific integrated circuits). The DPAT technique has been applied on both digital and mixed-signal ASICs covering a range of small to very large Si areas. The paper describes the criteria for defining appropriate parameters for DPAT. Typical examples for both mixed-signal and digital are presented. Also examples are shown of unjustified yield loss as a result of DPAT. Besides the immediate quality improvement through the removal of maverick devices, it was demonstrated that a systematic detailed evaluation of DPAT yield loss could be used as a tool to generate continuous manufacturing improvement. Also, a relationship was observed between the DPAT yield loss and the area of the chip. Finally it is demonstrated that the introduction of DPAT has resulted in a significant reduction of the number of field failures.

#### **6B.4 Product/Process Change Control in a "Zero Defects" Environment**

*Ruby Clark, Freescale Semiconductor*

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"Zero Defects" has become an integral part of manufacturing organizations providing parts for the automotive industry. Defect reduction/prevention and preventing the reoccurrence of defects have been an integral part of a "Zero Defects" approach to

manufacturing. With this focus of defect reduction/prevention, product/process changes are a 'necessary evil'. Success is achieved only when the product/process change control meets the requirements of a "Zero Defects" environment. In this presentation I will describe how the Manufacturing Organization of Freescale Semiconductor's ATMC (Austin Technology and Manufacturing Center) facility has integrated a "Zero Defects" approach in product/process change control. I will go through the process used to ensure the product/process change is controlled to maintain/ensure "Zero Defects". Throughout the presentation I will discuss the specific requirements in our product/process change control that help ensure success in the "Zero Defects" environment. The presentation will cover the steps that each product/process change must complete and the approval process prior to any change being made permanent. At the end of the presentation, attendees will have the basic understanding of product/ process change control in a semiconductor manufacturing operation.

## Session 7: Packaging Issues

Thursday, May 11

8:00 am – 10:05 am

### 7A.1 Reliability of COC Technology for Automotive Application

*Masakazu Yamana, NEC Electronics - Japan & Michael Wieberneit, NEC Electronics GmbH*

The increasing complexity of microelectronic devices for automotive applications requires integrating of various technologies towards a system solution. One approach to integrate different technologies to a system solution is the so-called COC (Chip-on-Chip) technology. In this paper we discuss the COC interconnection reliability with respect to the thermal stress requirements for automotive applications. The COC interconnection consists of an Au/Au connection based on a thermal-compression bump process. First results show an intermittent open failure of some COC connections depending on the thermal load. Special analysis technique has been used to confirm cracks at the connection interface. Cross section analysis and electrical test at high temperature has been applied to confirm the COC reliability after stress. New underfill materials and COC bonding parameters has been investigated to improve the COC reliability. The new conditions have been assessed after reflow stress, thermal shock stress and autoclave stress. As a result the best reliability performance requires an optimized match between the underfill material and the bonding conditions. Finally one combination could be determined which passed not only AEC-Q100 requirements but also extended temperature cycling stress. Today NEC Electronics is using the new COC process conditions in mass production for automotive applications.

### 7A.2 Impact of Warpage on BGA Quality

*Mike Varnau, Delphi Electronics & Safety*

BGA (Ball Grid Array) packages generally have outstanding assembly yield. However, as the BGA packages become larger, pitches and corresponding ball sizes decrease, a new assembly failure mechanism has developed. The inherent asymmetry of the BGA package makes the package susceptible to warpage if the CTE (Coefficient of Thermal Expansion) of the molding compound is not well matched to that of the BGA substrate. The CTE's must be reasonably well matched across the entire solder reflow temperature excursion. Otherwise, a part that is flat at room temperature will not be flat when the solder is liquid during the reflow process. Recent industry experience has seen this warpage effect cause both opens and shorts due to this phenomenon. This paper details the experience of identifying the problem, resultant process characterization, and solution to the problem.

### 7A.3 An Advanced Electronic Prognostic for FPGA Solder Joint Networks

*Russell Graves, Ridgetop Group, Inc.*

Ridgetop Group is developing innovative prototype electronic prognostic cells to detect damage to solder-joint networks of fully operational Field Programmable Gate Arrays (FPGAs) in a ball-grid array (BGA) packages such as the XILINX FG1156. FPGAs are used in all manner and kinds of Electronic Controllers in automotive an avionics systems and subsystems. Solder-joint damage is accumulative and results in increased crack growth rate and in increased frequency of high-resistance spikes. These faults typically manifest themselves as intermittent, hard-to-diagnose faults in which incorrect FPGA output signals occur. These intermittent faults increase in frequency, last longer and longer and lead to persistent failure.

The relative high density of the solder balls (also referred to as solder bumps) of BGA packages is a major challenge. If a solder bump in the interior of the package were to crack, there is no practical method of detecting the crack with or without an optical or other aid. The top of the package shields that bump from direct inspection, and because there is less than 1 mm spacing between the PWB and the bottom of the package, there is no practical method for inspecting interior bumps from the side. Even techniques such as X-ray examination are becoming more ineffective because the surfaces of the crack are typically parallel to the viewing plane. Active, real-time prognostics that work on fully-operational FPGAs, as opposed to dummy-chain chip packages, will result in earlier warning and provide high-confidence signal indications of fault occurrence, and the location of the damaged solder bumps.

## 7A.4 The Brittle Fracture of BGA Solder Joint during High Temperature Storage A Comparative Study of High Speed Shear/Pull and – A Comparison between SnPb and Pb-free Alloys

*Min Ding, Freescale Semiconductor*

The high temperature storage reliability of the solder joint has always been a major concern for automotive applications. Previous studies have shown that eutectic SnPb spheres yield a failure mode in solder ball shear test that transfers from the ductile bulk failure to the brittle interfacial intermetallic compound (IMC) failure. The phenomenon occurs after extended aging at elevated temperatures resulting from extensive growth of intermetallic compound. With Pb-free alloys, the IMC composition and growth kinetics at solder/pad interface is considerably different. In this present work, BGA packages with eutectic SnPb and SnAgCu Pb-free spheres on various pad finishes (electrolytic and electroless Ni/Au, solder on Cu) are studied. The SnPb and Pb Free alloys package components were stressed at 150 and 175°C for up to 1008 hours. The solder ball shear and pull at various speed ( $10^2$ ~ $10^6$  um/sec) were performed. The correlation between brittle failure rate and the stressing and test conditions are discussed. In the mean time, the evolution of intermetallic compound is examined using scanning electron microscope (SEM) and energy dispersive X-ray (EDX). The driving force and kinetics of the evolution as well as the correlation between the microstructure and mechanical strength is discussed.

## 7A.5 Surface Mount Technology in the Pb-free Era

*Pascal Oberndorff, Philips Semiconductors*

Pb-free technology is becoming more and more important, also in the automotive industry. Not only because many component suppliers will convert to Pb-free components due to the legislation, also Pb-free board assembly studies could become important for future applications. An important fact to consider is that the process window for Pb-free technology is smaller, hence the transition to Pb-free board assembly cannot be considered as a drop in replacement. It should also be considered that leadfree components are compatible with the standard solder processes but not always as drop in replacement.

Therefore, it is recommended to reconsider the SMT process. In this paper we would like to give some tips and tricks on how to deal with the transition based on the experience gained in other parts of the electronic industry. It is our opinion that sharing this knowledge will make it easier to obtain a smooth transition for both supplier as well as end-customer. Furthermore, we will deal with the obvious concern of the raised temperature, the impact on both the solder joint as well as the component. Other aspects that will be covered include board level reliability, component damage and the different appearance of Pb-free solder joints. Also some common failure modes will be illustrated with examples.

## Session 8: New Technologies

Thursday, May 11

10:30 am – 11:45 am

## 8A.1 Wire Bonding Divergence at the 65nm Node

*Glenn Tessmer, Texas Instruments*

90 nm node wire bonding to automotive standards is achieved through robust bond pad and bonding process design. It is also compatible with commercial die designs. This is demonstrated with bonded ball size versus failure mode study. The 65 and 45 nm node die shrinks present both wire bonding process and reliability challenges. A bonding process capability review indicates a divergence from baseline node processing. The divergence is driven by the differences between commercial and automotive quality requirements. The diffusion physics and product qualification specifications are constant forces being applied to smaller and smaller ball bonds. At some point this system will break. Extrapolation of the AEC Q100 ball shear specification indicates that the 45nm node is incompatible with current automotive reliability standards. A solution for low pin out designs is to simply enable larger bonds. However bond pad pitch limited designs challenge the size, performance and cost availability for automotive markets.

## 8A.2 Managing Power and Noise on 90nm FPGA and Beyond

*Bertrand Leigh, Lattice Semiconductor*

As the process technologies migrates towards 90nm and beyond for the Field Programmable Gate Array (FPGA) devices, the system designers must deal with the benefits and challenges that comes with these technologies. With these advance technologies, increased FPGA operating speed is the benefit. On the challenge side, the users must deal with the increased leakage current that translates to the power consumption of the device and switching noise associated with high-speed signal transitions.

Dealing with the power:

- Discuss the factors that contribute to power - Static & Dynamic Current
- What is the dependency for Static Current - Temperature, Package, & System Environment
- What is the dependency for Dynamic Current - Frequency & Activity Factor
- What tools are available from FPGA vendors to practically estimate these factors

Dealing with switching noise:

- SSO (Simultaneous Switching Outputs) Noise Considerations - I/O standards & pin placement
- How each I/O standards affects SSO Noise
- Trade-offs between signal integrity & SSO noise
- FPGA vendor tools to assist pin placement

### 8A.3 Transistor Reliability and Its Effect on Circuit Characteristics in 90nm LSI's

*Tomoya Omata, NEC Electronics - Japan*

As 90nm LSI's are being used in automotive electronics, it is getting more important to assess appropriate built-in reliability in the whole process of LSI development, such as from circuit design to mass production. We have extensively evaluated time evolution of transistor degradation process experimentally and determined its effectiveness on circuit characteristics. Propagation delay caused from drivability degradation of FET can be quantitatively evaluated by means of SPICE simulation considering transistor characteristics degradation. We elucidated transistor degradation owing to hot carrier injection and NBTI (negative bias temperature instability) mode, and estimated the change in propagation delay in some representative circuit used in conventional CMOS LSI's. As an example, we analyze the influence of hot carrier injection phenomena in PMOSFET, on propagation delay characteristics in CMOS circuits. The analysis result shows that hot carrier injection effect on PMOSFET can be efficiently prevented by appropriate circuit design restriction, taking into consideration realistic circuit operation conditions. We concluded that assessment from the viewpoint of both circuit design and physical device degradation model is indispensable in order to achieve automotive level reliability for under 90nm LSI's.

## Session 9: Failure Analysis & System Issues

Thursday, May 11  
1:15 pm – 2:55 pm

### 9A.1 Failure Modes, Mechanisms, and Effects Analysis for Automotive Electronics

*Diganta Das, CALCE Electronic Products & Systems Center*

Failure mechanisms are the processes by which physical, electrical, chemical and mechanical stresses induce failure. Knowledge of the failure mechanisms that cause product failure is essential to design and qualify reliable products. The standard Failure Modes and Effects Analysis (FMEA) and Failure Modes, Effects and Criticality Analysis (FMECA) procedures do not identify the product failure mechanisms and models. This paper describes a methodology, Failure Modes, Mechanisms and Effects Analysis (FMMEA), which enhances the value of FMEA and FMECA by identifying high priority failure mechanisms and failure models. FMMEA can be used to aid several design and development steps considered to be best practices, such as virtual qualification, root cause analysis, accelerated test programs, and remaining life assessment. High priority failure mechanisms indicate the operational stresses, and the environmental and operational parameters that need to be controlled. Models for the failure mechanisms help in the design and development of the product. The FMMEA methodology is applied to an

electronic circuit board assembly mounted in an automotive underhood environment.

### 9A.2 Fault Localization and Verification Techniques for Semiconductor Devices

*Eric Bedes & Will Frizzell, NEC Electronics America, Inc.*

Both non-destructive and destructive failure analysis techniques are essential to fault localization in semiconductor devices. When only a single sample is available, it is absolutely critical that the fault is accurately located before any destructive analysis is attempted. With semiconductor devices becoming more complex, non-destructive techniques such as Emission and IR-OBIRCH can reveal multiple suspect fault locations. The challenge of reducing these multiple locations to one common fault can be difficult without combining additional analysis techniques. Interfacing to an LSI Tester, GDS Cad Overlay, and FIB circuit modification can all be used to help localize the fault. Once the fault is localized destructive analysis techniques are employed for verification. Choosing the best technique for imaging the fault is extremely important and the nature of the fault will determine which technique will give the best results. To accomplish this there are a number of options available using the FIB, SEM, and TEM electron microscopes. In cases where the fault location is well defined the micro sampling lift-out technique is typically the best method. When the area surrounding the fault may also provide important data, FIB cross-section or layer by layer etch back may be better choices to ensure sample preservation.

### 9A.3 Intermittent Failures in High Pin Count Packaging

*Cleston Messick, Northrop Grumman*

With present day high pin count packaging, intermittent problems can be a function of the system design, software, testing and manufacturing techniques making the determination of the root cause of intermittent failures extremely difficult. Typically, design engineers may spend weeks trying to solve intermittent problems relating to a design when, in actuality, it may be just a function of the parts used in the system development. High pin count devices passing normal accelerated reliability testing exhibited intermittent failures when monitored during temperature changes. Failure analysis by Focused Ion Beam, Auger and SEM showed an inadequate bonding process. Further analysis found a process controlled by high CPK values rather than standard statistical control methodologies. The root cause of the intermittent failures most likely originated with the die manufacturer. Evidence of bonding process variations, probably in response to a fabrication limitation, indicates some lack of communication between various manufacturing entities. Another analysis shows several statistically significant differences between parts with the same date code. With a process not in statistical control, normal sampling techniques may be insufficient.

## **9A.4 A New Failure Mode - Surface ESD**

*Zhongning Liang, Philips Semiconductors*

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In the context of Zero Defects, some failure modes could be seen as new failure modes to which we need to pay attention. "Surface ESD" is recognized a new failure mode, also called ESD From Outside to Surface (ESDFOS). Surface ESD is not comparable with common ESD behaviors, such as HBM, MM, CDM, and TLP (transmission line pulse). Electrostatic pulses discharge directly onto the chip surface and not pass through pad protection structures. This means that normal ESD protection circuitry does not work for this Surface ESD mechanism! Without proper prevention and consideration in equipment design, this event usually occurs in post-wafer processing, leading to significant final test yield loss. Furthermore, the surface ESD damage can be latent, leading to reliability risk! In this presentation, we will show Surface ESD evidence, how to install effective measure and monitoring, and eventually how to prevent it from happening. The results are also shown.